DLPA100 电源管理和电机驱动器

1 特性

- 3.3V 开关稳压器 - 逻辑电源
- 具有使能功能的 5V 开关稳压器 - 模拟电路电源
- 1.0V 至 3.3V 可调节开关稳压器 - 内核电源
- 具有使能功能的可调节线性稳压器 - 锁相环 (PLL) 电源
- 具有使能功能的可调节线性稳压器控制 - 模拟电源
- 2.5V 开关稳压器数字电源
- 电源序列控制
- 电源监控电路
- 适用于高侧驱动的集成电荷泵
- 三个风扇驱动器
- 热关断电路
- 串行通信接口
- 三相反电动势 (BEMF) 电动机驱动器/控制器
- 电机电源开关稳压器

2 应用

- 4K 超高清 (UHD) 显示屏
- 激光电视 (TV)
- 数字标牌
- 投影映射

3 说明

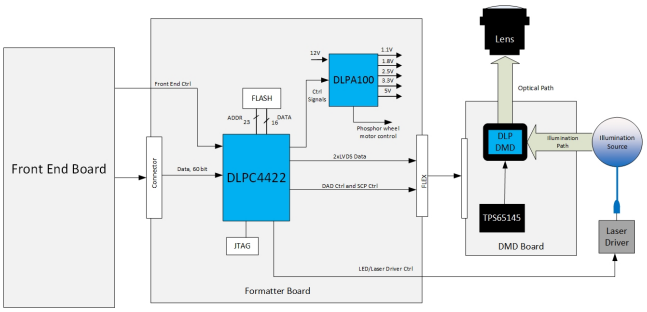
DLPA100 是一款专用电源管理和电机控制驱动器，适用于 DLP®4K UHD TRP 显示芯片组。DLPA100 与 DLP660TE 数字微镜器件和 DLPC4422 显示控制器共同构成芯片组。这款解决方案非常适合需要高分辨率、高亮度和系统简易性的显示系统。为了确保操作可靠性，DLP660TE DMD 和 DLPC4422 显示控制器必须始终与 DLPA100 电源管理和电机驱动器件搭配使用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLPA100	PT (48)	0.276mm x 0.276mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

图 1. 典型应用图



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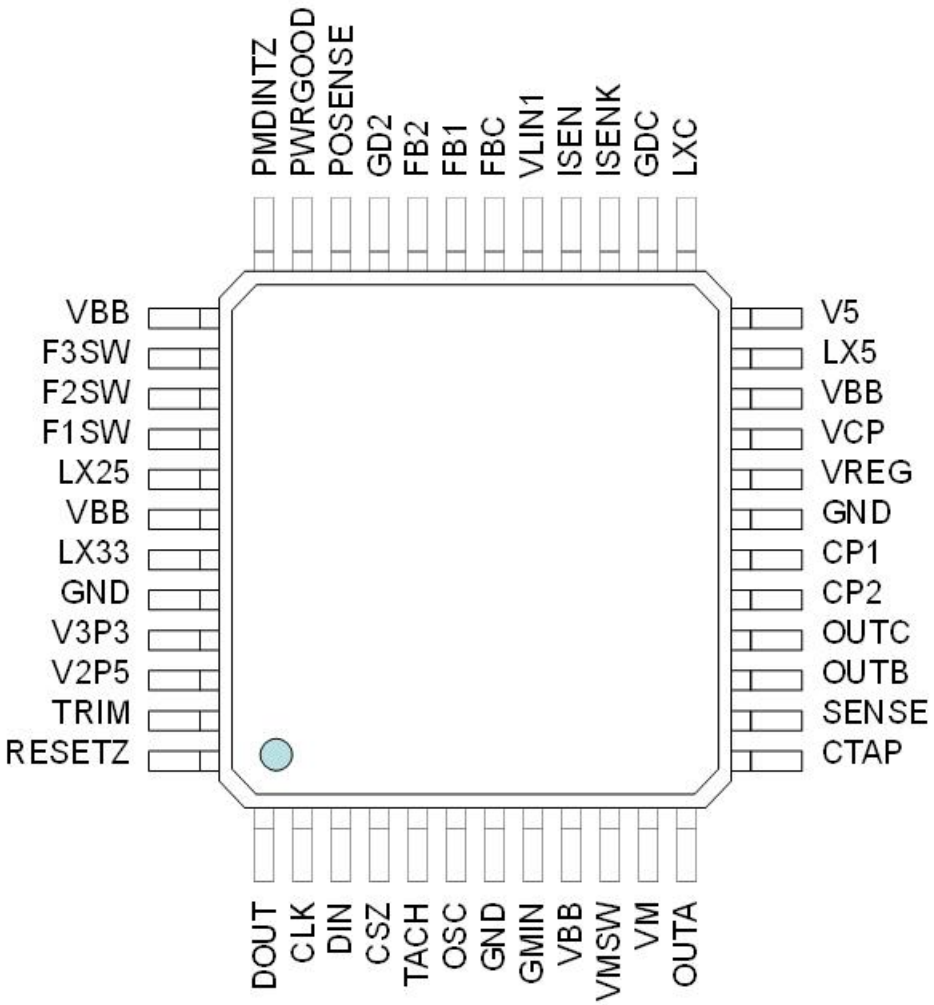
4 修订历史记录

日期	修订版本	注释
	*	首次发布。

5 Pin Configuration and Functions

(PT package)
(48 pin QFP)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DOUT	1	Output	Data Out for Serial Port
CLK	2	Input	Clock for Serial Port
DIN	3	Input	Data In for Serial Port
CSZ	4	Input	Chip Select for Serial Port
TACH	5	Output	Motor Speed Indication
OSC	6	Input	Master Osc for Digital Timing – 2 MHz typical
GND	7	Ground	Ground
GMIN	8	Input	Motor Gm Input
VBB	9	Power	VBB Load Supply
VMSW	10	Output	Motor Supply Switching Node
VM	11	Input	Motor Supply INPUT/FB
OUTA	12	Output	Motor Phase A
CTAP	13	Input/Output	Motor Centertap
SENSE	14	Input	Motor Current Sensing
OUTB	15	Output	Motor Phase B
OUTC	16	Output	Motor Phase C
CP2	17	Power	Charge Pump
CP1	18	Power	Charge Pump
GND	19	Ground	Ground
VREG	20	Power	Internal Bias Regulator Terminal
VCP	21	Power	Charge Pump Reservoir Capacitor Terminal
VBB	22	Power	VBB Load Supply
LX5	23	Output	5V Regulator Switching Node
V5	24	Power Input	5V Feedback and Logic Supply Input
LXC	25	Power Output	Adjustable Core Regulator Switching Node
GDC	26	Power Output	Gate Drive for Core Regulator
ISENK	27	Input	Kelvin Sense for Core Regulator
ISEN	28	Input	Current Sense for Core Regulator
VLIN1	29	Power Output	VLIN1 Linear Regulator Output
FBC	30	Power Input	Adjustable Core Switching Regulator Feedback Node
FB1	31	Power Input	VLIN1 Adjustable Feedback Node
FB2	32	Power Input	VLIN2 Adjustable Feedback Node
GD2	33	Power Output	VLIN2 Linear Gate Drive Output
POSENSE	34	Output	Power On Reset Output
PWRGOOD	35	Output	Power Good Output
PMDINTZ	36	Output	Interrupt Flag
VBB	37	Power	Motor Supply Terminal
F3SW	38	Output	Fan 3 Switching Node Output
F2SW	39	Output	Fan 2 Switching Node Output
F1SW	40	Output	Fan 1 Switching Node Output
LX25	41	Power Output	2.5V Regulator Switching Node
VBB	42	Power	VBB Load Supply
LX33	43	Power Output	3.3V Regulator Switching Node
GND	44	Ground	Ground
V3P3	45	Power Input	3.3V Feedback
V2P5	46	Power Input	2.5V Feedback

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TRIM	47	Power	Trim Pin (must be tied to VREG)
RESETZ	48	Input	Forced Reset

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
VBB	Load Supply Voltage		15	V
t_{ramp}	Time to ramp from 0V to VBB	200		µs
Vx	LX33, LXC, LX5, OUTA, OUTB, OUTC	-1		V
Vin	Logic Inputs (RESETZ, CLK, DIN, CSZ, OSC)	-0.3	7	V
Vout	Open Drain Logic Outputs (PWRGOOD, DOUT, POSENSE, PMDINTZ, TACH)		7	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Storage Conditions

		MIN	MAX	UNIT
T_{stg}	Storage temperature	-55	150	°C

6.3 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VBB	Load supply voltage			15	V
T_a	Operational ambient temperature	0		75	°C
T_j	Maximum Operational junction temperature			150	°C

6.5 Thermal Information

THERMAL METRIC(1)		DLPA100 LQFP 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BB1}	Supply Current	Motors and fans off			26	mA
I_{BB2}	Supply Current	All Regulators Operating, I_load= 0 mA			36	mA
I_{BB3}	Supply Current	x3 fans = 100% mode @ 200 mA load, VM = 100% mode @ 200 mA		2.7		A
CONTROL LOGIC						
V_{IL}	Logic Input Voltage (RESETZ, CLK, DIN, CSZ, OSC)				0.8	V
V_{IH}			2.0			V
I_{IL}	Logic Input Current	V_{IN} = 5	-20	<1.0	20	µA
I_{IH}		V_{IN} = 0	-20	<-1.0	20	µA
Vlow	Open Drain Logic Outputs (PWRGOOD, DOUT, POSENSE,PMDINTZ, TACH)	I = 4 mA			0.4	V
Iout	Logic Output Leakage Current	V = 3.3 V			1	µA
CHARGE PUMP						
V_{CP}	Output Voltage	Relative to VBB		7.25		V
VCP_{uvlo}	VCP Undervoltage			5.5		V
SWITCHING REGULATORS						
V_5	Output Voltage V5	Average Voltage, I_out = 0 mA to 1.6 A	4.75	5	5.25	V
Rds5	Buck Switch Rdson	T_j = 25°C		150		mΩ
Icl5	Buck Switch Current Limit		2.8	3.4	4.0	A
Fsw	Switching Frequency		450	500	525	kHz
tss	Soft Start		3	5	7	ms
V_{33}	Output Voltage V3P3	Average Voltage, I_out = 0 mA to 1.6 A	3.168	3.3	3.432	V
Rds33	Buck Switch Rdson	T_j = 25°C		300		mΩ
Icl33	Buck Switch Current Limit		2.4	2.8	3.4	A
Fsw	Switching Frequency		450	500	525	kHz
tss	Soft Start		3	5	7	ms
V_{core}	Output Voltage VCORE Range		1.0		3.3	V
V_{c1}	Output Voltage VCORE	Average Voltage, I_out = 200 mA to 3.7 A, using 0.5% tolerance feedback resistors	-4.0		4.0	V
V_{c2}	Output Voltage VCORE	Average Voltage, I_out = 0 mA to 200 mA, using 0.5% tolerance feedback resistors	-4.0		6.0	V
Iclc	Buck Switch Current Limit	Isense Resistor = 100 mΩ	4.8	5.5	6.5	A
T_{RISE}	Gate Drive Rise Time	Cl = 500 pF, Vgs = 7 V (10% to 90%)		40		ns
T_{FALL}	Gate Drive Fall Time	Cl = 500 pF, Vgs = 0 V (90% to 10%)		40		ns
Fsw	Switching Frequency		450	500	525	kHz
tss	Soft Start		3	5	7	ms
V_{25}	Output Voltage V2P5	Average Voltage, I_out = 0 mA to 1.2 A	2.4	2.5	2.6	V
Rds5	Buck Switch Rdson	T_j = 25°C		300		mΩ
Icl5	Buck Switch Current Limit		1.7	2.1	2.5	A

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Fsw	Switching Frequency		450	500	525	kHz
tss	Soft Start		3	5	7	ms
LINEAR REGULATORS						
Output Voltage VLIN1 Range			1.0		3.3	V
Vout	Output Voltage VLIN1	Average voltage relative to target, I_load =2 mA to 75 mA, using 0.5% tolerance feedback resistors	-3%		3%	
I_{LIM}	VLIN1 Current Limit		100	150		mA
RR	Ripple rejection	f = 120 Hz, Cout = 10 µF	60			dB
I_{FB}	Feedback Input Bias Current		-400	-100	100	nA
tss	Soft Start		3	5	7	ms
VLIN2 External FET Supply Voltage			1.7		5.5	V
Output Voltage VLIN2 Range			1.0		3.3	V
Vout	Output Voltage VLIN1	Average voltage relative to target, I_load = 10 mA to 1.2 mA, using 0.5% tolerance feedback resistors	-3%		3%	
RR	Ripple rejection	f = 120 Hz, Cout = 10 µF	60			dB
I_{FB}	Feedback Input Bias Current		-400	-100	100	nA
tss	Soft Start		3	5	7	ms
FAN CONTROLLERS						
F_{pwm}	PWM switching frequency	Controlled by DLPC4422 Software		100		kHz
F_{pwm}	PWM switching frequency	Controlled by DLPC4422 Software		24		Hz
Duty Cycle LSB					500	ns
Rds	Rdson Buck Switch	I = 200 mA		1		Ω
Current Limit			550		875	mA
Current Limit Blanking		Controlled by DLPC4422 Software		20		µs
COLOR WHEEL SWITCHING REGULATOR SUPPLY						
VM	Output Voltage	Average Voltage, I_out = 0 mA to maximum programmed load current. Buck inductor = 33 µH	-5%		5%	
Rds	Buck Switch Rdson	T_j = 25°C		500		mΩ
Icl	Buck Switch Current Limit	relative to target programmed value	-20%	0%	20%	
T_{off}	Fixed off-time	VM >6 V		1.33		µs
T_{off}	Fixed off-time	2.6 V < VM <4.0 V		4.7		µs
T_{off}	Fixed off-time	VM < 1.5 V		17		µs
tss	Soft Start					
COLOR WHEEL MOTOR DRIVER						
Pdm	Power Dissipation				1.0	W
Rdson	Source Driver Rdson	I = 1 A		400	600	mΩ
Rdson	Sink Driver	I = 1 A		500	700	mΩ
Im	Drive Current				1.4	A
Ib	Brake Current				2.5	A

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

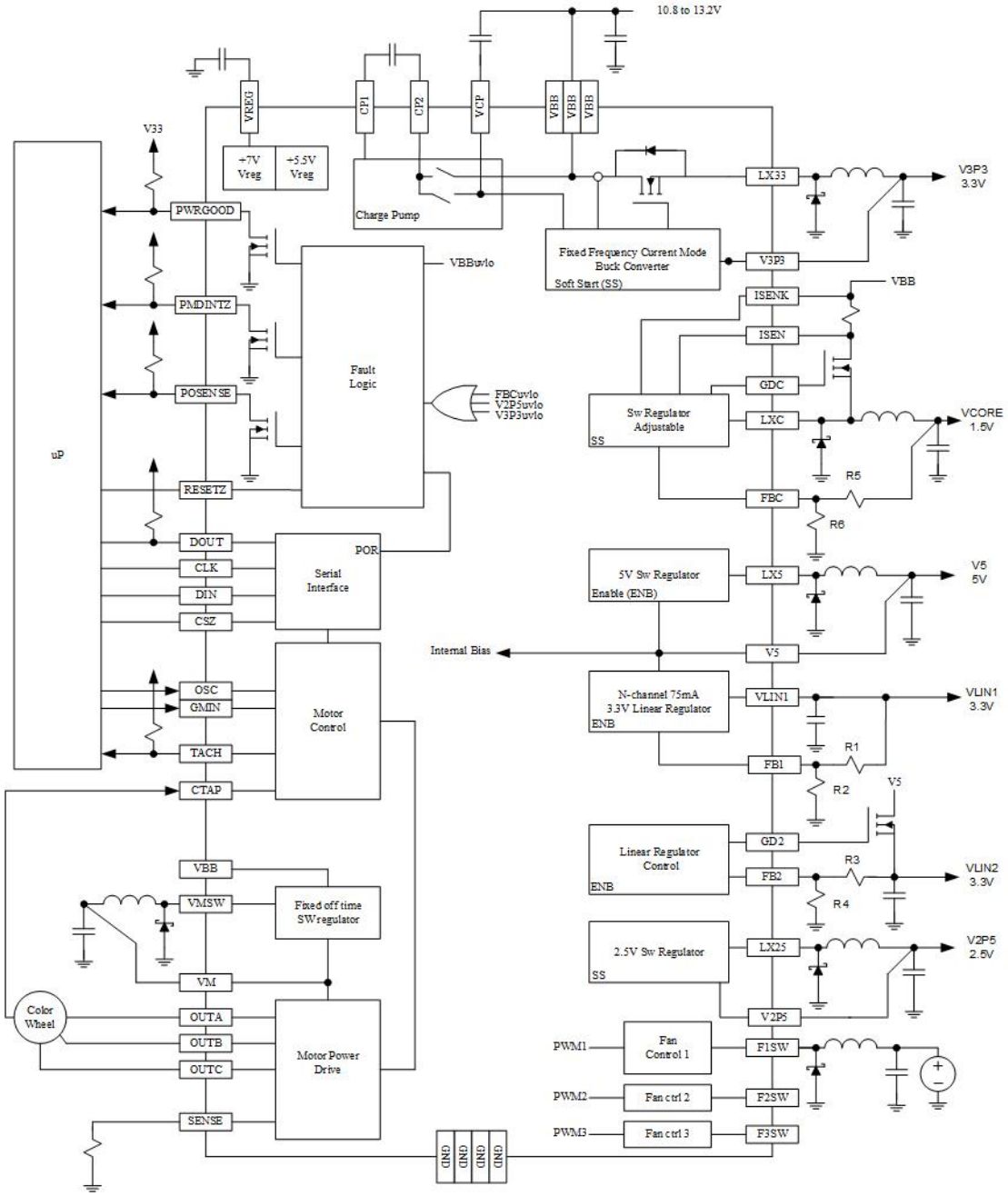
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Tb	Brake Period	For brake current to change from maximum value (2.5 A) to the maximum drive current (1.4 A)			800	ms
Kgm	Gm Constant	Controlled by DLPC4422 Software		125		
		Controlled by DLPC4422 Software		250		
Vos	Offset			0.5		V
	Bemf Comp Hysteresis	Vctap = 1.5 V to 6 V	5	20	35	mV
Fosc	OSC (Motor Oscillator)				5	MHz
Th	OSC High Period		100			ns
Tl	OSC Low Period		100			ns
MOTOR CHARACTERISTICS						
Rload	Load Resistance	Phase to Phase	1.5		15	Ω
#	Poles		4	12	16	Poles
	Speed	Poles = 12 or 16	2880	7200	11160	rpm
		Poles = 4 or 8	2880	7200	14880	rpm
	Commutation Period - (60/[Speed(rpm) × 3 × #Poles])	4-Pole at 2880 rpm			1736	µs
		16-Pole at 11160 rpm	112			µs
L/R	Time Constant - Phase to Phase inductance divided by Phase-to-Phase resistance	4-Pole at 14880 rpm			112	µs
		8-Pole at 14880 rpm			56	µs
		12-Pole at 11160 rpm			50	µs
		16-Pole at 11160 rpm			37	µs

7 Detailed Description

7.1 Overview

The DLPA100 is a power management and motor driver IC optimized for DLP video and data display systems and meant for use in either embedded or accessory projector applications. DLPA100 is part of the chipset comprising of the DLP660TE DMD and DLPC4422 controller.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Up Sequencing

Once the VBB voltage reaches the VBB_{uvsd} threshold (specification defined in *Shutdown*), the VCORE channel soft-starts within a period of 5 ms typical (tss). Once this period is completed and the $VCORE_{uvlo}$ has been reached, the V3P3 and V2P5 rails soft-start, ramping up ratiometrically. Once each of the three rails are above their respective undervoltage lockout levels ($VCORE_{uvlo}$, $V3P3_{uvlo}$, $V2P5_{uvlo}$), the POSENSE flag will go high after a period of 150 ms typical (T_{por}) and also, the VLIN1, VLIN2, V5 and VM rails soft-start, ramping up ratiometrically. Note that VLIN1, VLIN2, V5 and VM can be individually disabled via the serial port, although VLIN1 and VLIN2 require V5 to be present.

The PWRGOOD flag will go high once the POSENSE is high and the VBB voltage is above the undervoltage lockout threshold VBB_{uvlo}.

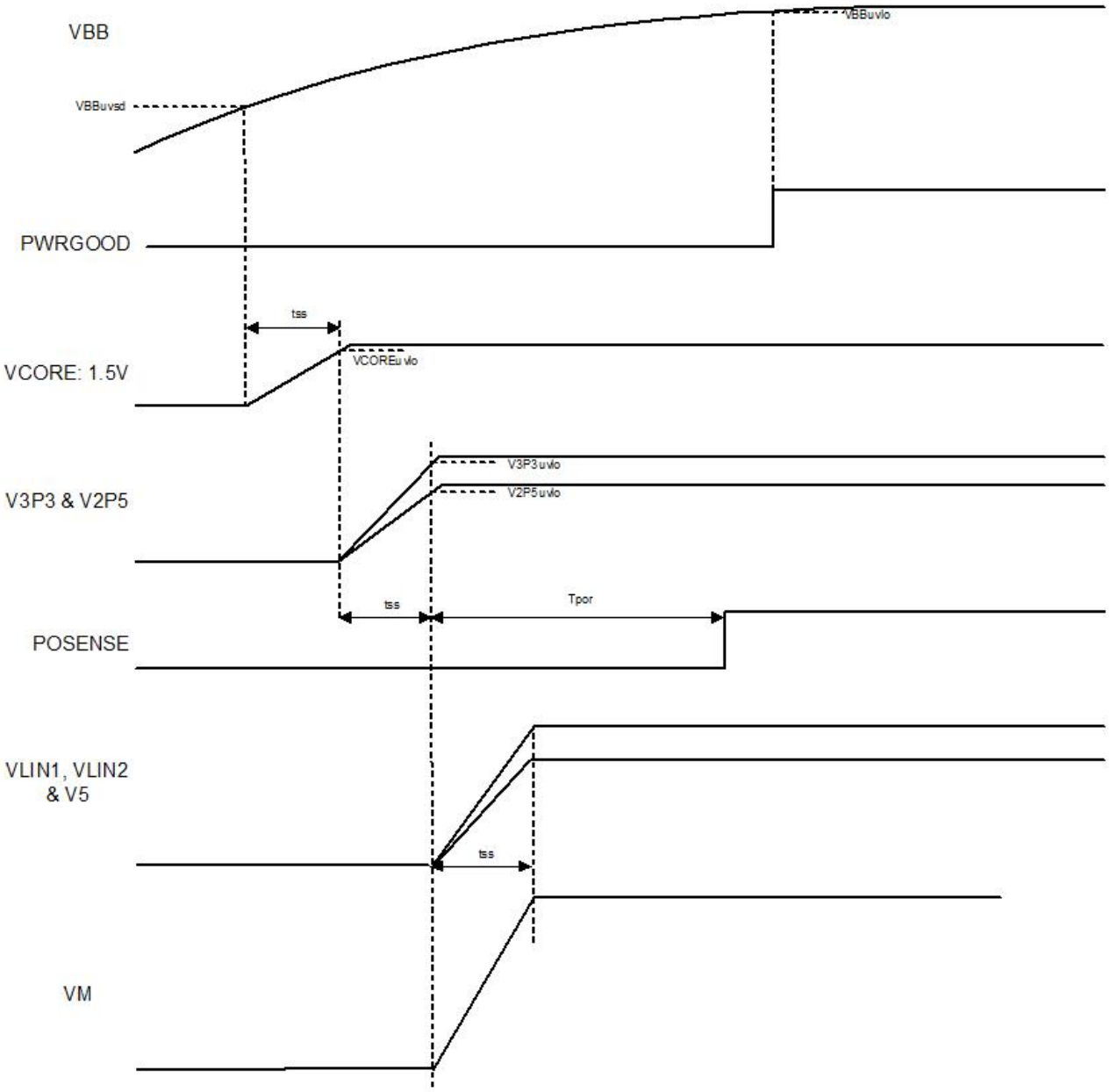


Figure 2. Power Up Sequencing Timing Diagram

Feature Description (continued)

7.3.2 Power Down Sequencing

If VBB drops below the undervoltage level (VBB_{uvlo}), the PWRGOOD will flag. If VBB drops below the undervoltage level (VBB_{uvsd}), all the switcher and linear channels will turn off and the output rails will be supplied by the output filter capacitors. The duration between VBB_{uvlo} and VBB_{uvsd} allows sufficient 'hold up' time to 'park' the DMD mirrors. Although the regulators can supply rated current down to VBB_{uvsd}, they can only provide this power for a maximum of 0.5 ms.

If either of the rails: VCORE or V3P3 or V2P5 drop below their respective undervoltage levels, the POSENSE and PWRGOOD will flag immediately.

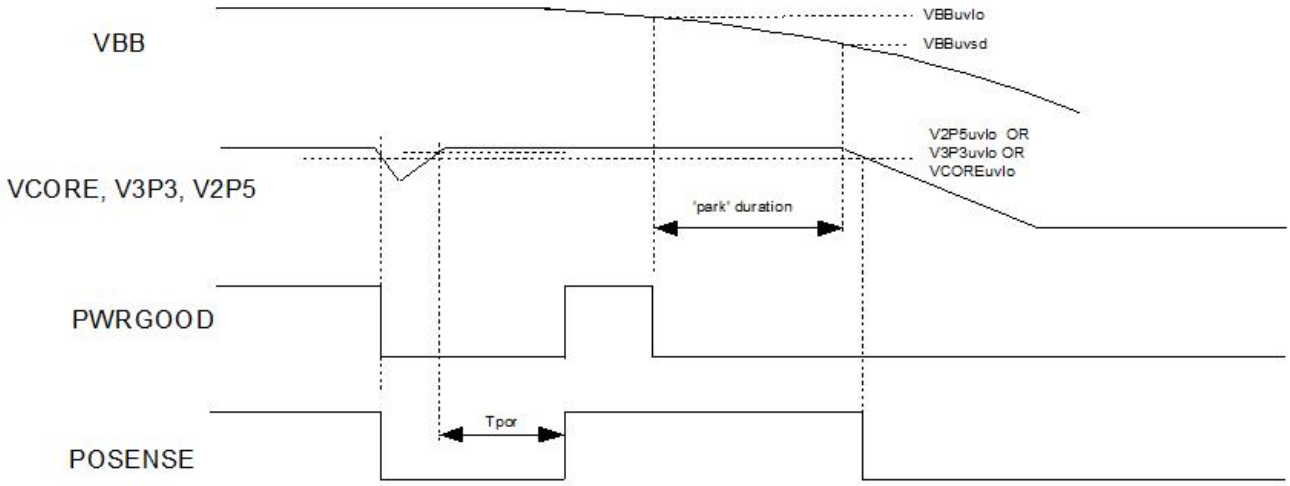


Figure 3. Power Down Sequencing Timing Diagram

7.3.3 Shutdown

In the event of a fault either due to excessive junction temperature, or low voltage on VCP, or low voltage on VREG, or low VBB voltage, each switcher and linear channel is disabled.

A low VBB voltage, VBB_{uvsd} in this case, shuts down the DLPA100, protecting it from excessive power dissipation. An undervoltage power monitoring flag, PWRGOOD is also provided, to indicate when the VBB voltage is operating in and out of normal operating range.

7.3.3.1 Thermal

An overtemperature monitor provides a warning when the junction temperature reaches 130°C. The DLPA100 is protected from excessive temperatures by an internal circuit that will shut the device down immediately the junction temperature reaches 165°C. As soon as the temperature drops below the hysteresis level, the regulators will start-up again under soft-start control, assuming all other conditions are met (VCP, VBB etc.).

7.3.4 System Reset

The DLPA100 device can be reset by using the RESETZ input. This feature can be used during start-up conditions to reset the serial port registers to a known set of states. It can also be used during power-down conditions to disable certain features before complete shutdown occurs. The DLPC4422 display controller software controls which functions are reset to the power on reset (POR) state when RESETZ is initiated.

- MSKFAN: Masks the reset of the 3 fan drivers (POR state = disabled, PWM=0%).
- MSKREG: Masks the reset of linear regulators VLIN1 & VLIN2, and 5V switcher (POR state = enabled).
- MSKMOT: Masks the reset of the motor controller configuration registers (POR state = 0).
- MSKMOTE: Masks the reset of the motor controller output enable bit (POR state = disabled).

Feature Description (continued)

7.3.5 Interrupt Logic

PMDINTZ is an active low open drain output that will be asserted if the DLPA100 goes into thermal shutdown at 165°C. The open drain output is held low by using the DLPA100 internal regulator even though the rest of the DLPA100 device is shut down. This internal regulator only depends on 12 V being operational to allow retention of the data in the latched status registers if any of the supplies are lost. PMDINTZ is primarily used as an interrupt to the DLP controller but can also be used to drive an LED overtemp indicator on the projector.

The thermal warning signal (TWARN) can also trigger an interrupt if enabled. Over-current events for the three DLP controller supplies can also cause PMDINTZ to go low. The DLP controller processor can clear or set PMDINTZ by writing to the latches that capture the interrupts. The DLP controller can also mask any of the interrupts (except TSD) via the enable interrupt register.

The raw status register can be read back in real time to monitor the fault condition. If the faults are present for a valid time, they will be latched into the latched status register.

7.3.6 Serial Communications Port

The Serial communications port (SCP) is a full duplex, synchronous, character-oriented byte port that allows exchange of data between the DLP controller (master) and the DLPA100.

Table 1. Serial Communications Port Signal Definitions

SIGNAL	I/O	FROM/TO	TYPE	DESCRIPTION
SCPK	I	SCP bus master to slave	LVTTL compatible	SCP bus serial transfer clock. The host processor (master) generates this clock.
SCPENZ	I	SCP bus master to slave	LVTTL compatible	SCP bus access enable (low true). When high, slave will reset to idle state, and SCPDO output will tri-state. Pulling SCPENZ low initiates a read or write access. SCPENZ must remain low for an entire read/write access, and must be pulled high after the last data cycle. To abort a read or write cycle, pull SCPENZ high at any point.
SCPDI	I	SCP bus master to slave	LVTTL compatible	SCP bus serial data input. Data bits are valid and must be clocked in on the falling edge of SCPCK.
SCPDO	O	SCP bus slave to master	LVTTL open drain w/tri-state	SCP bus serial data output. Data bits must clocked out on the rising edge of SCPCK.

Table 2. Serial Interface Timing Requirements

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	NOM	MAX	UNIT
A	Setup CSZ low to CLK	Reference to rising edge of CLK	360			ns
B	Byte to Byte Delay	Nominally 1 CLK cycle rising edge to rising edge	1.9			µs
C	Setup DIN to CSZ High	Last byte to slave disable	360			ns
	CLK Frequency		0		526	kHz
D	CLK Period		1.9	2		µs
E	CLK High or Low Time		300			ns
F	DIN Set-Up Time	Reference to falling edge of CLK	300			ns
G	DIN Hold Time	Reference from falling edge of CLK	300			ns
H	DOUT Propogation Delay	Reference from rising edge of CLK			300	ns
	CLK Filter (pulse reject)		200			ns

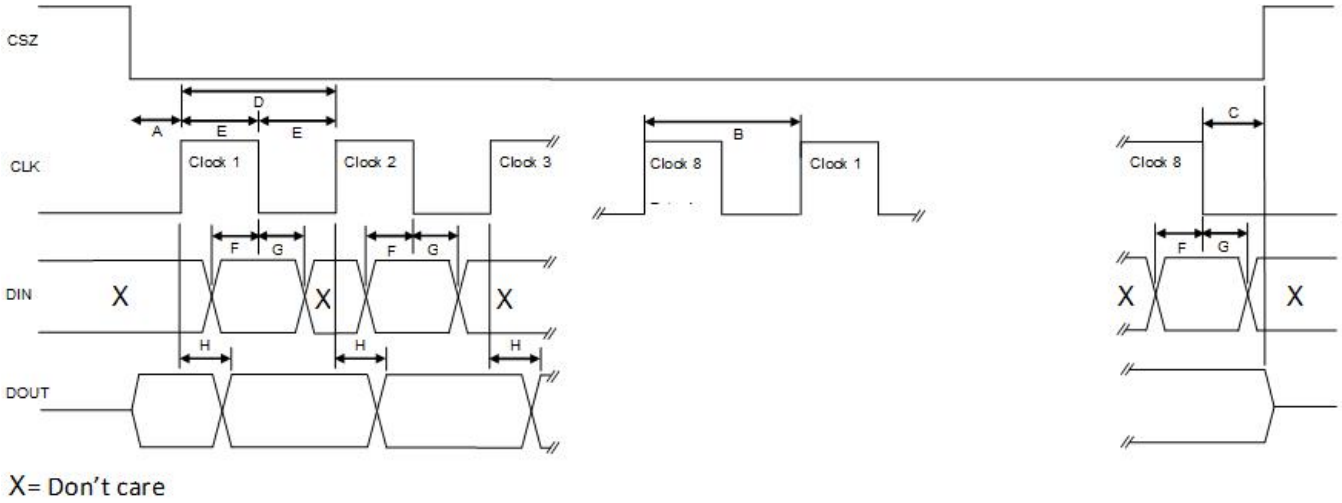


Figure 4. Serial Communications Port Timing Diagram

7.3.7 Switching Regulators

The DLPA100 has four fixed frequency current mode control buck regulators that are used to provide power to integrated circuits in the system. The V5 regulator is used to power control functions in the DLPA100, as well as power the VLIN1 and VLIN2 linear regulators.

The regulators require external fly back diodes, inductors and filter capacitors. Due to the high currents in the VCORE regulator, an external FET and sense resistor are required. The regulators will operate in both continuous and discontinuous mode. An internal blanking circuit will be used to filter out transients due to the reverse recovery of the external clamp diode.

7.3.7.1 Output Voltage - VOUT

All of the switchers apart from VCORE are regulated with respect to a 1.2 V reference (V_{FB}). As the Core Regulator (VCORE) output voltage is adjustable from 1.0 V to 3.3 V the internal reference for this output is 0.8 V.

$$Vout = V_{FB} \times (1 + R1/R2) \quad (1)$$

7.3.7.2 Adjustable Linear Regulator - VLIN1

This low dropout type regulator features current limit for a shorted load. It includes an integrated n-channel pass element and can work with either ceramic or electrolytic output capacitors. The output can range between 1.0 V and 3.3 V. The output voltage of the adjustable regulator is set by:

$$VLIN1 = V_{FB} \times (1+R1/R2) + (I_{FB} \times R2)$$

where

- V_{FB}= 0.8 V (2)

7.3.7.3 Adjustable Linear Regulator Control - VLIN2

An additional linear regulator is implemented with external n-channel pass element. The output can range between 1.0 V and 3.3 V. The output voltage of the adjustable regulator is set by:

$$VLIN2 = V_{FB} \times (1+R3/R4) + (I_{FB} \times R4)$$

where

- V_{FB}= 0.8 V (3)

7.3.8 Fan Controllers

The DLPA100 has three outputs available to be used as the switching node for either voltage mode step down switcher or ‘direct drive’ schemes. The output voltage is determined by a PWM value programmed using the DLPC4422 display controller software. The switching frequency for each output can be programmed using the DLPC4422 display controller software for either 100 kHz for applications requiring a step-down switcher, or 24 Hz in applications that can utilize a direct drive scheme. The drivers in the ‘direct drive’ scheme are connected to the corresponding fans via a series resistor.

The default condition at start-up will be separate control of each fan control channel and 100kHz switching frequency.

7.3.9 Color Wheel Motor Driver

The driver system is a three phase BEMF sensing motor controller and driver. Commutation is controlled by a proprietary BEMF sensing technique. It eliminates many external passive components and provides flexibility by allowing various timing parameters to be programmed via the serial port.

7.3.9.1 Color Wheel Motor Driver Power Dissipation

The maximum allowable power dissipation on motor driver is specified in the color wheel motor driver table. Motor driver power dissipation can be calculated as follows:

$$Pdm = [VM – (KE \times Sm) – Ispd \times Rpp] \times Ispd \quad (4)$$

where

- Pdm = Power dissipation of motor driver
- VM = Programmed output voltage of the motor supply
- KE = Motor voltage constant in Volts/(rad/sec)
- Sm = Motor speed in rad/sec
- Ispd = Motor current at Sm speed
- Rpp = Phase-to-phase motor resistance

7.3.10 Color Wheel Switching Regulator Supply

A fixed off time switching regulator is included to manage power dissipation for driving color wheels. For highly resistive motors requiring a low running current, Irun < 75 mA, using this regulator may not be required, in which case VM should be connected directly to VBB and the external inductor, capacitor & Schottky diode do not need to be fitted.

7.4 Device Functional Modes

DLPA100 device functional modes are controlled by the DLPC4422 display controller. See the DLPC4422 display controller datasheet or contact a TI applications engineer.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). DMDs vary in resolution and size and can contain over 8 million micromirrors. Each micromirror of a DMD can represent either one or more pixels on the display and is independently controlled, synchronized with color sequential illumination, to create stunning images on any surface. DLP technology enables a wide variety of display products worldwide, from tiny projection modules embedded in smartphones to high powered digital cinema projectors, and emerging display products such as digital signage and laser TV.

In display applications using the DLP660TE DMD the DLPA100 provides all needed analog functions including the analog power supplies and the color wheel motor driver to provide a robust and efficient display solution.

8.2 Typical Application

When the DLPA100 power management device is combined with two display controllers (DLPC4422), an FPGA, and other electrical, optical and mechanical components the chipset enables bright, affordable, full 4K UHD display solutions. The DLPA100 power management and motor driver provides power supply sequencing and controls the color wheel motors, laser and LED currents as required by the application. A typical 4K UHD system application is shown in Figure 5.

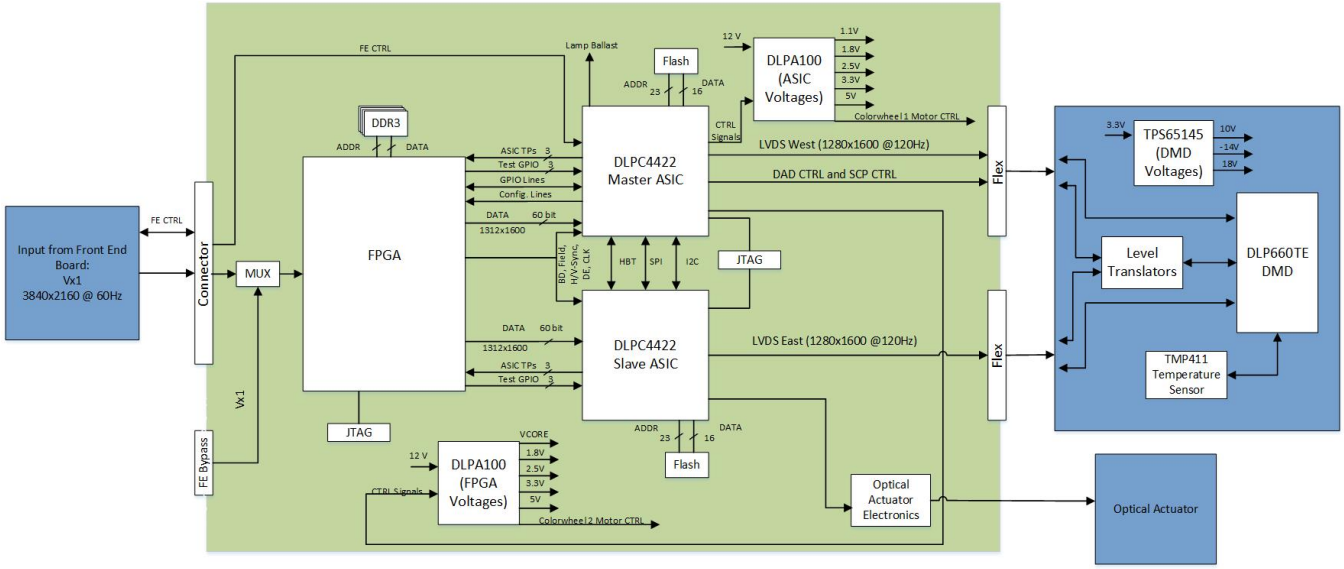


Figure 5. Typical 4K UHD Projector Application

8.2.1 Design Requirements

At the high level, DLP660TE DMD systems will include an illumination source, a light engine, electronic components, and software. The designer must first choose an illumination source and design the optical engine taking into consideration the relationship between the optics and the illumination source. The designer must then understand the electronic components of a DLP660TE DMD system. A display projector is created by using a DLP chipset comprised of DLP660TE DMD, DLPC4422 controller and DLPA100 power and motor driver. The DLPC4422 does the digital image processing, the DLPA100 provides the needed analog functions for the projector, and the DMD is the display device for producing the projected image.

Typical Application (continued)

8.2.2 Detailed Design Procedure

For connecting together the DLPC4422 digital display controller, the DLP660TE DMD, and the DLPA100, see the reference design schematic. Layout guidelines should be followed to achieve a reliable projector. To complete the DLP system an optical module or light engine is required that contains the DLP660TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

8.2.3 Application Curves

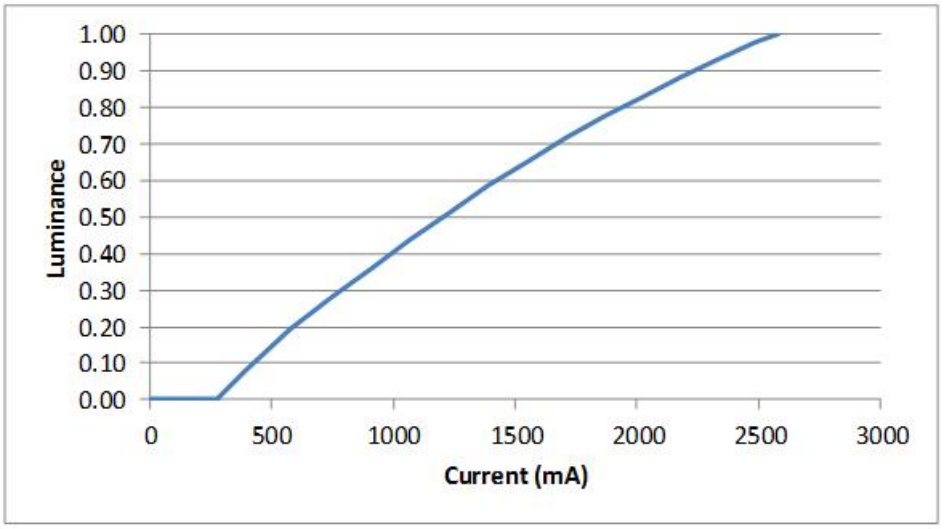


Figure 6. Luminance vs. Current

9 Power Supply Recommendations

The DLPA100 is designed to operate from a 12-V input voltage supply or battery. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminal, or supply peak current limitations, additional bulk capacitance may be required. If ringing occurs an electrolytic or tantalum type capacitor may be needed for damping. The amount of bulk capacitance required should be evaluated such that the input voltage can remain in specification long enough for a proper fast shutdown to occur as shown in Figure 3. The shutdown begins when the input voltage drops below the programmable UVLO threshold, such as when the external power supply or battery supply is suddenly removed from the system.

10 Layout

10.1 Layout Guidelines

The 12-V supply, VBB, should be provided on a separate plane, or portion of a shared power distribution plane. Each ceramic filter capacitor should be placed as close as possible to each VBB terminal: pins 9, 22, 37 and 42. The additional reservoir capacitor should also be placed as close as possible to the VBB terminals. The ground for VBB should be routed directly to the DLPA100 thermal pad connection.

The PWB traces used on the switching regulators should be as short and wide as possible. The electrical loops formed between the VBB filter capacitors, input switch (LX pins), inductor, output capacitor and the diode should be as small as possible.

An adjacent layer ground region covering the entire switching node should be provided for the pins: LXC (pin 25), LX5 (pin 23), LX33 (pin 43), LX25 (pin 41), and VMSW (pin10). Each of the switching nodes and all associated components should be located as near the DLPA100 device as possible.

Avoid routing any noise sensitive signals near the DLPA100 device switching nodes and associated ground regions. The sensitive pins on the DLPA100 device consist of pins 1, 2, 3, 4, 5, 6, 8, and 48. If sensitive signals must be routed across the switching loops, use subdivided planes and/or multiple ground planes to avoid interference. Use of shielded inductors on the switching regulator circuits will minimize the possibility of crosstalk and interference.

High current paths should have an adequate number of vias to minimize resistance and inductance. Placement and routing priority should be given to the higher current circuits. For example, the VCORE supply should take precedence over a fan PWM output. The following is the order of precedence from highest to lowest:

1. VCORE
2. V5
3. V3P3
4. V2P5
5. VM
6. VLIN2
7. VLIN1
8. FAN1, FAN2, FAN3

Suitable kelvin connections should be provided for the regulator feedback pins: FBC (pin 30), V2P5 (pin 46), V3P3 (pin 45), V5 (pin 24), FB1 (pin 31) & FB2 (pin 32) and for sense pins: SENSE (pin 14), ISEN (pin 28) & ISENK (pin 27). Also note that the external feedback networks used for the VCORE and VLIN1 regulators should also deploy kelvin connections. The feedback pin traces FBC, FB1, FB2 are most prone to interference and should be located near the DLPA100 device.

10.2 Grounding Guidelines

Ground pin 19 is isolated internally to the DLPA100 from pins 7 and 44. All three ground pins should be tied together on the PWB at the DLPA100 thermal pad connection. Depending on the application there are three grounding approaches for board layout:

1. Completely isolated ground regions for the DLPA100 subcircuits.
2. Single isolated ground region for the collective DLPA100 circuit.
3. Non-isolated common ground region for the entire board.

   The most favorable approach should be carefully considered for the specific application.

Grounding Guidelines (continued)

10.2.1 Completely Isolated Ground Regions

In this case, the PWB has an isolated ground layer around the DLPA100 circuit which serves as a “noisy” ground for the motor driver, switchers, and linear regulators. This plane can be subdivided into isolated sections around each switcher, linear regulator and motor block to minimize the possibility of noise crosstalk between the regulator circuits. See Figure 7. Each isolated section should be connected in a “star” configuration at the DLPA100 thermal pad position. An additional “quiet” solid ground plane should be provided on a separate layer for reference to the sensitive blocks of the DLPA100 device and other sensitive external circuitry. The sensitive pins on the DLPA100 device are pins 1, 2, 3, 4, 5, 6, 8, and 48. The quiet ground plane should connect to the DLPA100 device with the array of thermal vias.

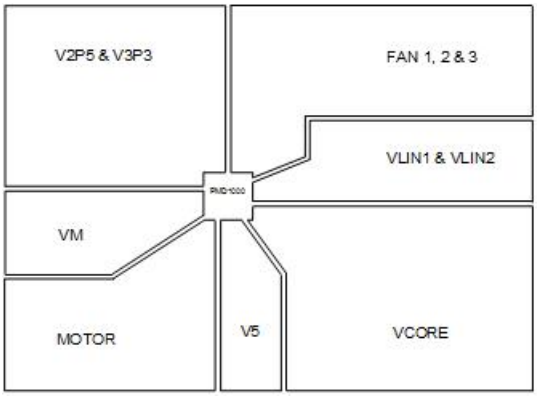


Figure 7. Noisy Ground Layer

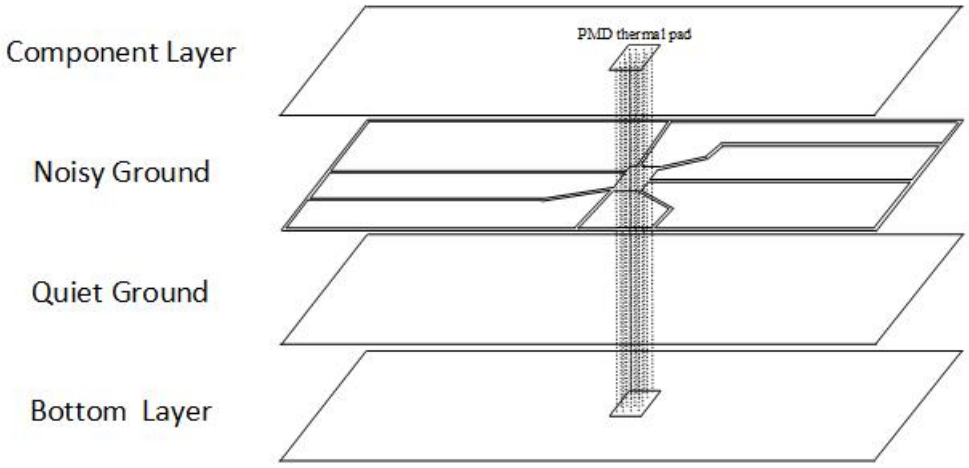


Figure 8. PWB Planes

10.2.2 Single Isolated Ground Region

In this case, the PWB has a single isolated ground layer around the DLPA100 circuit. This ground layer serves as a “noisy” ground for the switchers, linear regulators, and motor driver. An additional “quiet” solid ground plane should be provided on a separate layer for reference to the sensitive blocks of the DLPA100 and other sensitive external circuitry. Connect the “quiet” and “noisy” ground planes at the DLPA100 thermal pad array of vias.

10.2.3 Non-isolated Common Ground Region

In this case, the PWB has a solid non-isolated common ground layer for the entire board. In this configuration, use particular care during component placement and separate the noisy portions of the DLPA100 circuit from other sensitive signals on the board. The ground plane should connect to the DLPA100 with the array of thermal vias.

10.3 Thermal Guidelines

The PWB should have a thermal pad underneath the DLPA100 on both the top and bottom layers. The thermal pad on the top layer should extend to the edge of the terminal pads and include a 4x4 array of thermal vias. These thermal pads should connect to the internal ground planes via the thermal vias. It is recommended that the internal ground plane should extend for at least 20 square inches.

Careful consideration should be taken in providing an adequate amount of copper traces around the discrete Schottky diodes and MOSFET terminals used in the switching and linear converters to ensure proper thermal management. The thermal impedance (T_{j-a}) of each component should be calculated to determine the corresponding amount of copper required. If using an internal plane, it is important to use an array of thermal vias underneath the device tab or terminal to assist in the transfer of the heat.

10.4 Motor Control Guidelines

The DLPA100 motor control terminals should be filtered with voltage transient suppressing devices for improved startup reliability and noise immunity. Schottky diodes should be placed cathode to anode between VBB to motor terminals OUTA (pin 12), OUTB (pin 15), OUTC (pin 16) and CTAP (pin 13). Schottky diodes should also be placed cathode to anode between motor terminals OUTA (pin 12), OUTB (pin 15), OUTC (pin 16) and CTAP (pin 13) to ground. Series RC snubbers consisting of a capacitor (0.001 μF) in series with a resistor (150 Ω) should be placed between the motor terminals OUTA (pin12), OUTB (pin 15), and OUTC (pin 16) to CTAP (pin 13).

The value of the motor current sensing resistor on SENSE (pin 14) should be thoroughly evaluated for the application. Careful consideration should be taken in the amount of current draw during motor startup and braking with respect to the speed range and speed change timing requirements. It is recommended that the SENSE (pin 14) voltage does not exceed 450 mV. Most motors from today's modern technology have relatively low operating currents but higher start-up currents which make it very difficult to achieve good signal to noise ratio during operating range and meet the 450 mV maximum on SENSE (pin 14). Most motors have demonstrated success well below 100 mV steady-state SENSE (pin 14) voltage. As long as good layout and component selection practices are followed, acceptable signal to noise ratios can be achieved at such low operating SENSE (pin 14) voltages. The typical SENSE resistor value ranges from 0.47 Ω to 2.2 Ω. A 1.0-Ω SENSE resistor value is suggested as a good starting point. Typically the steady-state SENSE (pin 14) voltage with a 1.0-Ω resistor will be near 100 mV.

10.5 Layout Example

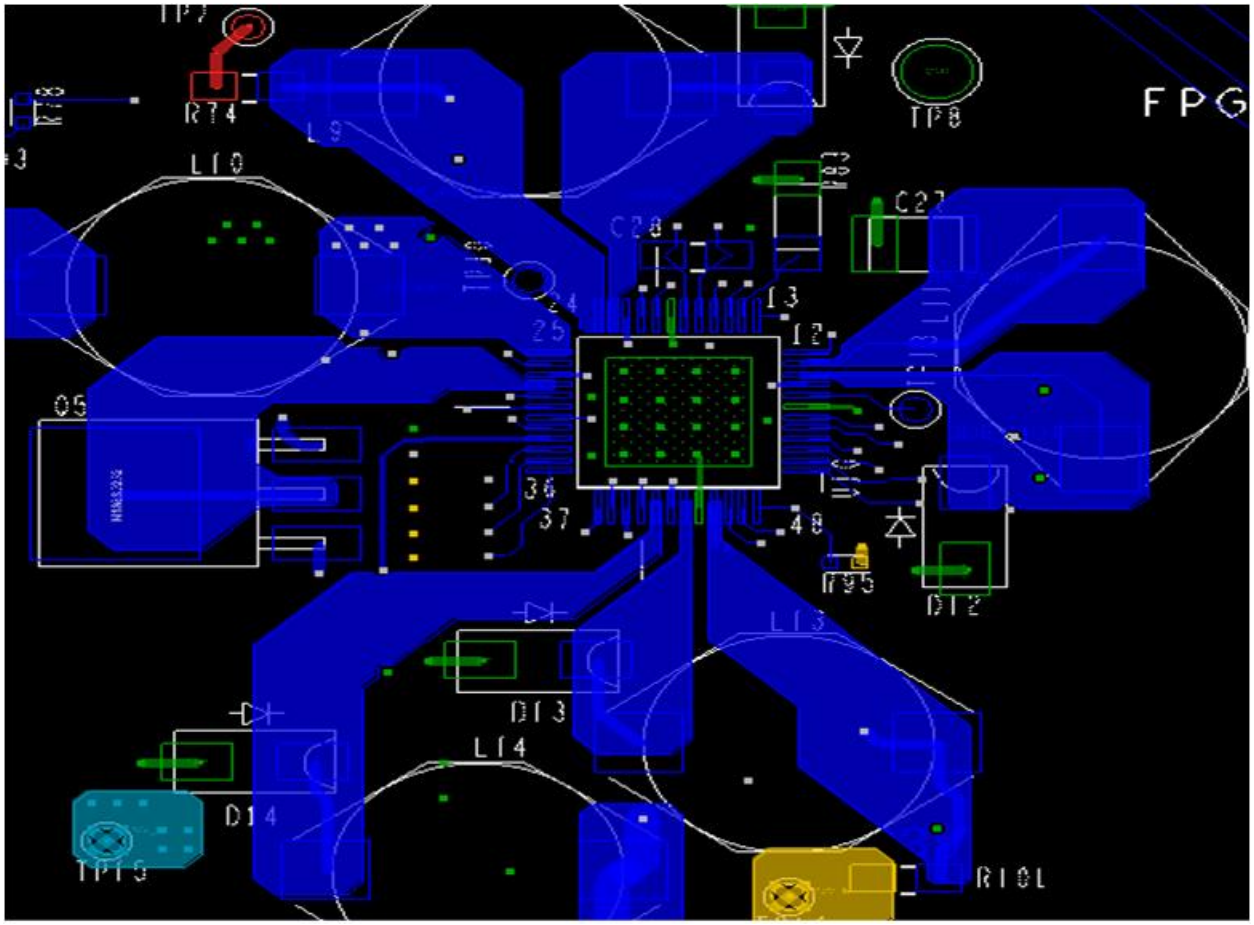


Figure 9. Top Layer

11 器件和文档支持

11.1 器件标记

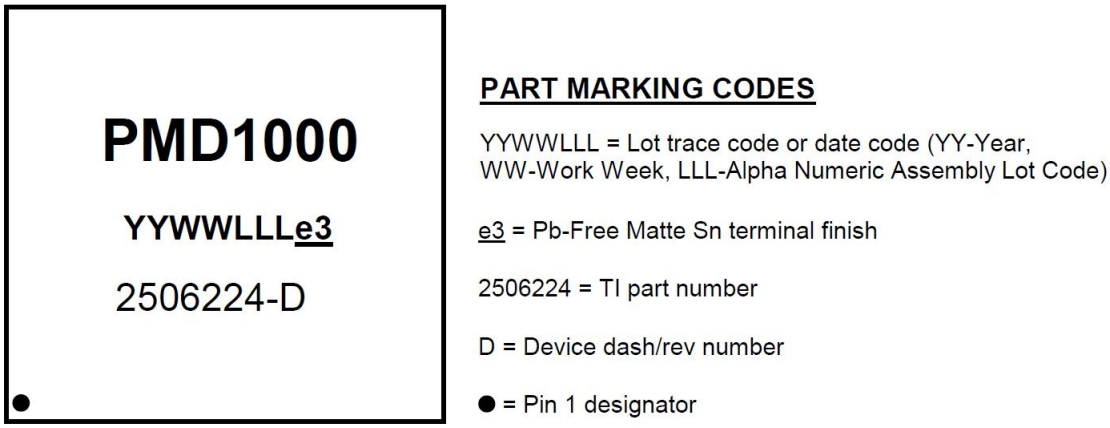


图 **10.** 器件标记

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- 《DLPC4422 显示控制器数据表》
- 《DLP660TE DMD 数据表》

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPA100PT	ACTIVE			48	260	TBD	Call TI	Call TI	0 to 75		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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