DLP9000 Family of 0.9 WQXGA Type A DMDs

1 Features

- High Resolution 2560×1600 (WQXGA) Array
  - > 4 Million Micromirrors
  - 7.56-µm Micromirror Pitch
  - 0.9-Inch Micromirror Array Diagonal
  - ±12° Micromirror Tilt Angle (Relative to Flat State)
  - Designed for Corner Illumination
  - Integrated Micromirror Driver Circuitry
  - Two High Speed Options
- DLP9000X With a Single DLPC910 Digital Controller
  - 480 MHz Input Data Clock Rate
  - Up to 61 Giga-Bits Per Second (with Continuous Streaming Input Data)
  - Up to 14989 Hz (1-Bit Binary Patterns)
  - Up to 1873 Hz (8-Bit Gray Patterns With Illumination Modulation)
- DLP9000 with Dual DLPC900 Digital Controllers
  - 400 MHz Input Data Clock Rate
  - Up to 38 Giga-Bits per Second (With Up to 400 Pre-Stored Binary Patterns)
  - Up to 9523 Hz (1-Bit Binary Patterns)
  - Up to 1031 Hz (8-Bit Gray Patterns Pre-Loaded With Illumination Modulation), External Input Up to 360 Hz
- Designed for Use With Broad Wavelength Range
  - 400 nm to 700 nm
  - Window Transmission 95% (Single Pass, Through Two Window Surfaces)
  - Micromirror Reflectivity 88%
  - Array Diffraction Efficiency 86%
  - Array Fill Factor 92%

2 Applications

- Industrial
  - Machine Vision and Quality Control
  - 3D Printing
  - Direct Imaging Lithography
  - Laser Marking and Repair
- Medical
  - Ophthalmology
  - 3D Scanners for Limb and Skin Measurement
  - Hyper-Spectral Imaging
  - Hyper-Spectral Scanning
- Displays
  - 3D Imaging Microscopes
  - Intelligent and Adaptive Lighting

3 Description

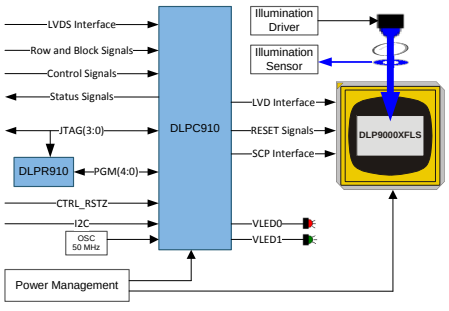
Featuring over 4 million micromirrors, the high resolution DLP9000 and DLP9000X digital micromirror devices (DMDs) are spatial light modulators (SLMs) that modulate the amplitude, direction, and/or phase of incoming light. This advanced light control technology has numerous applications in the industrial, medical, and consumer markets. The streaming nature of the DLP9000X and its DLPC910 controller enable very high speed continuous data streaming for lithographic applications. Both DMDs enable large build sizes and fine resolution for 3D printing applications. The high resolution provides the direct benefit of scanning larger objects for 3D machine vision applications.

Device Information(1)

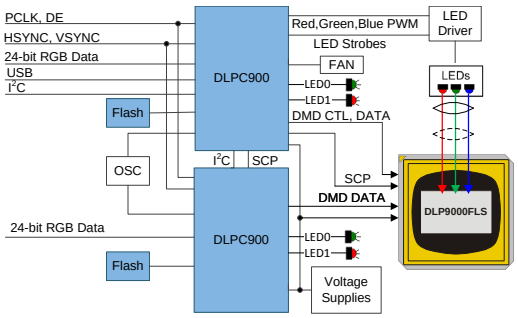
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP9000	CLGA (355)	42.20 mm x 42.20 mm x 7.00 mm
DLP9000X		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical DLP9000X Application



Typical DLP9000 Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2015) to Revision B **Page**

- Separated TCASE into TARRAY and TWINDOW. Changed TGRADIENT to TDELTA. Reduce DCLK_A,B,C,D for DLP9000 in *Absolute Maximum Ratings*. ... 11
- Separated Tstg into Tdmd and RH in *Storage Conditions*. ... 12
- Changed TDMD to TARRAY and TGRADIENT to TDELTA, added short term operational, and updated temperature values in *Recommended Operating Conditions*. ... 13
- Added the four modes of operation. ... 21
- Removed the column showing the pixel data rate and added the pattern mode pattern rates ... 21
- Updated CL2w constant in *Micromirror Array Temperature Calculation*. ... 33
- Added recommended idle mode operation for maximizing mirror useful life. ... 34
- Updated Micromirror Derating Curve ... 34
- Added mirror park sequence requirements. ... 41
- Updated device nomenclature and markings. ... 51

Changes from Original (September 2014) to Revision A **Page**

- Updated title ... 1
- Updated *Features*, *Description*, and *Device Information* to include DLP9000XFLS DMD. ... 1
- Added DLP9000XFLS application diagram. ... 1

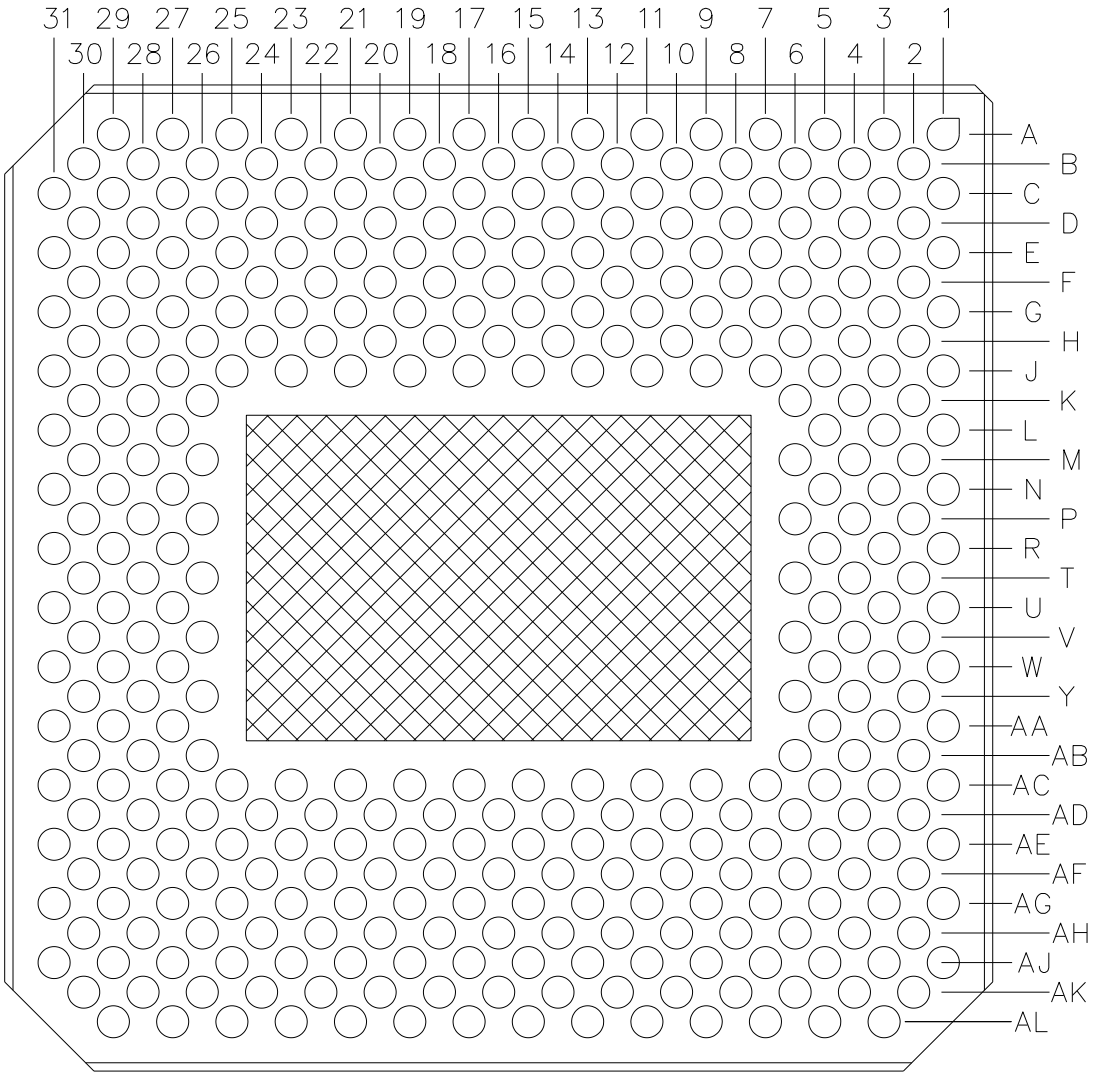
- Updated *Absolute Maximum Ratings* to include DLP9000XFLS absolute maximum ratings. 11
- Updated *Recommended Operating Conditions* to include DLP9000XFLS recommended operating conditions. 12
- Updated *Electrical Characteristics* to include DLP9000XFLS electrical characteristics. 14
- Updated *Electrical Characteristics* to include DLP9000XFLS electrical characteristics. 15
- Updated *Timing Requirements* to include DLP9000XFLS timing requirements 16
- Updated *Typical Characteristics* tables to have pixel data rates and patttern rates for both the DLP9000FLS and the DLP9000XFLS. 21
- Updated *Device Functional Modes* section to include DLP9000X functional description. 32
- Updated *Application and Implementations* section to include typical application for the DLP9000XFLS. 37

5 Description (continued)

Reliable function and operation of the DLP9000 family requires that each DMD be used in conjunction with its specific digital controller. The DLP9000X must be driven by a single DLPC910 Controller and the DLP9000 must be driven by two DLPC900 Controllers. These dedicated chipsets provide robust, high resolution, high speed system solutions.

6 Pin Configuration and Functions

FLS Package Connector Terminals
355-Pin CLGA
Bottom View



Pin Functions

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	DESCRIPTION	TRACE (mils) (4)
NAME	NO.						
DATA BUS A							
D_AN(0)	H10	Input	LVDS	DDR	Differential	Data, Negative	737
D_AN(1)	G3	Input	LVDS	DDR	Differential	Data, Negative	737
D_AN(2)	G9	Input	LVDS	DDR	Differential	Data, Negative	737
D_AN(3)	F4	Input	LVDS	DDR	Differential	Data, Negative	738
D_AN(4)	F10	Input	LVDS	DDR	Differential	Data, Negative	739
D_AN(5)	E3	Input	LVDS	DDR	Differential	Data, Negative	739
D_AN(6)	E9	Input	LVDS	DDR	Differential	Data, Negative	737
D_AN(7)	D2	Input	LVDS	DDR	Differential	Data, Negative	737
D_AN(8)	J5	Input	LVDS	DDR	Differential	Data, Negative	739
D_AN(9)	C9	Input	LVDS	DDR	Differential	Data, Negative	736
D_AN(10)	F14	Input	LVDS	DDR	Differential	Data, Negative	743
D_AN(11)	B8	Input	LVDS	DDR	Differential	Data, Negative	737
D_AN(12)	G15	Input	LVDS	DDR	Differential	Data, Negative	739
D_AN(13)	B14	Input	LVDS	DDR	Differential	Data, Negative	740
D_AN(14)	H16	Input	LVDS	DDR	Differential	Data, Negative	737
D_AN(15)	D16	Input	LVDS	DDR	Differential	Data, Negative	737
D_AP(0)	H8	Input	LVDS	DDR	Differential	Data, Positive	737
D_AP(1)	G5	Input	LVDS	DDR	Differential	Data, Positive	738
D_AP(2)	G11	Input	LVDS	DDR	Differential	Data, Positive	737
D_AP(3)	F2	Input	LVDS	DDR	Differential	Data, Positive	736
D_AP(4)	F8	Input	LVDS	DDR	Differential	Data, Positive	739
D_AP(5)	E5	Input	LVDS	DDR	Differential	Data, Positive	738
D_AP(6)	E11	Input	LVDS	DDR	Differential	Data, Positive	737
D_AP(7)	D4	Input	LVDS	DDR	Differential	Data, Positive	737
D_AP(8)	J3	Input	LVDS	DDR	Differential	Data, Positive	739
D_AP(9)	C11	Input	LVDS	DDR	Differential	Data, Positive	737
D_AP(10)	F16	Input	LVDS	DDR	Differential	Data, Positive	741
D_AP(11)	B10	Input	LVDS	DDR	Differential	Data, Positive	737
D_AP(12)	H14	Input	LVDS	DDR	Differential	Data, Positive	739
D_AP(13)	B16	Input	LVDS	DDR	Differential	Data, Positive	739
D_AP(14)	G17	Input	LVDS	DDR	Differential	Data, Positive	737
D_AP(15)	D14	Input	LVDS	DDR	Differential	Data, Positive	737
DATA BUS B							
D_BN(0)	AD8	Input	LVDS	DDR	Differential	Data, Negative	739
D_BN(1)	AE3	Input	LVDS	DDR	Differential	Data, Negative	737
D_BN(2)	AF8	Input	LVDS	DDR	Differential	Data, Negative	736
D_BN(3)	AF2	Input	LVDS	DDR	Differential	Data, Negative	739
D_BN(4)	AG5	Input	LVDS	DDR	Differential	Data, Negative	737
D_BN(5)	AH8	Input	LVDS	DDR	Differential	Data, Negative	737
D_BN(6)	AG9	Input	LVDS	DDR	Differential	Data, Negative	737
D_BN(7)	AH2	Input	LVDS	DDR	Differential	Data, Negative	739

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.
(2) DDR = Double Data Rate.
SDR = Single Data Rate.
Refer to the *Timing Requirements* regarding specifications and relationships.
(3) Internal term = CMOS level internal termination. Refer to *Recommended Operating Conditions* regarding differential termination specification.
(4) Dielectric Constant for the DMD Type A ceramic package is approximately 9.6.
For the package trace lengths shown:
Propagation Speed = 11.8 / sqrt(9.6) = 3.808 in/ns.
Propagation Delay = 0.262 ns/in = 262 ps/in = 10.315 ps/mm.

Pin Functions (continued)

PIN [1]		TYPE (I/O/P)	SIGNAL	DATA RATE [2]	INTERNAL TERM [3]	DESCRIPTION	TRACE (mils) [4]
NAME	NO.						
D_BN(8)	AL9	Input	LVDS	DDR	Differential	Data, Negative	737
D_BN(9)	AJ11	Input	LVDS	DDR	Differential	Data, Negative	738
D_BN(10)	AF14	Input	LVDS	DDR	Differential	Data, Negative	736
D_BN(11)	AE11	Input	LVDS	DDR	Differential	Data, Negative	737
D_BN(12)	AH16	Input	LVDS	DDR	Differential	Data, Negative	740
D_BN(13)	AD14	Input	LVDS	DDR	Differential	Data, Negative	737
D_BN(14)	AG17	Input	LVDS	DDR	Differential	Data, Negative	738
D_BN(15)	AD16	Input	LVDS	DDR	Differential	Data, Negative	738
D_BP(0)	AD10	Input	LVDS	DDR	Differential	Data, Positive	738
D_BP(1)	AE5	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(2)	AF10	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(3)	AF4	Input	LVDS	DDR	Differential	Data, Positive	738
D_BP(4)	AG3	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(5)	AH10	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(6)	AG11	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(7)	AH4	Input	LVDS	DDR	Differential	Data, Positive	740
D_BP(8)	AL11	Input	LVDS	DDR	Differential	Data, Positive	736
D_BP(9)	AJ9	Input	LVDS	DDR	Differential	Data, Positive	739
D_BP(10)	AF16	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(11)	AE9	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(12)	AH14	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(13)	AE15	Input	LVDS	DDR	Differential	Data, Positive	737
D_BP(14)	AG15	Input	LVDS	DDR	Differential	Data, Positive	740
D_BP(15)	AE17	Input	LVDS	DDR	Differential	Data, Positive	739
DATA BUS C							
D_CN(0)	C15	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(1)	E15	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(2)	A17	Input	LVDS	DDR	Differential	Data, Negative	736
D_CN(3)	F20	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(4)	B20	Input	LVDS	DDR	Differential	Data, Negative	738
D_CN(5)	G21	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(6)	D22	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(7)	E23	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(8)	B26	Input	LVDS	DDR	Differential	Data, Negative	739
D_CN(9)	F28	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(10)	C27	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(11)	J29	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(12)	D26	Input	LVDS	DDR	Differential	Data, Negative	737
D_CN(13)	H26	Input	LVDS	DDR	Differential	Data, Negative	739
D_CN(14)	E29	Input	LVDS	DDR	Differential	Data, Negative	736
D_CN(15)	G29	Input	LVDS	DDR	Differential	Data, Negative	737
D_CP(0)	C17	Input	LVDS	DDR	Differential	Data, Positive	738
D_CP(1)	E17	Input	LVDS	DDR	Differential	Data, Positive	737
D_CP(2)	A15	Input	LVDS	DDR	Differential	Data, Positive	735
D_CP(3)	F22	Input	LVDS	DDR	Differential	Data, Positive	737
D_CP(4)	B22	Input	LVDS	DDR	Differential	Data, Positive	737
D_CP(5)	H20	Input	LVDS	DDR	Differential	Data, Positive	737
D_CP(6)	D20	Input	LVDS	DDR	Differential	Data, Positive	737
D_CP(7)	E21	Input	LVDS	DDR	Differential	Data, Positive	737
D_CP(8)	B28	Input	LVDS	DDR	Differential	Data, Positive	739

Pin Functions (continued)

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	DESCRIPTION	TRACE (mils) (4)
NAME	NO.						
D_CP(9)	F26	Input	LVDS	DDR	Differential	Data, Positive	735
D_CP(10)	C29	Input	LVDS	DDR	Differential	Data, Positive	737
D_CP(11)	J27	Input	LVDS	DDR	Differential	Data, Positive	737
D_CP(12)	D28	Input	LVDS	DDR	Differential	Data, Positive	736
D_CP(13)	H28	Input	LVDS	DDR	Differential	Data, Positive	739
D_CP(14)	E27	Input	LVDS	DDR	Differential	Data, Positive	736
D_CP(15)	G27	Input	LVDS	DDR	Differential	Data, Positive	737
DATA BUS D							
D_DN(0)	AJ15	Input	LVDS	DDR	Differential	Data, Negative	737
D_DN(1)	AC27	Input	LVDS	DDR	Differential	Data, Negative	737
D_DN(2)	AK16	Input	LVDS	DDR	Differential	Data, Negative	738
D_DN(3)	AE29	Input	LVDS	DDR	Differential	Data, Negative	738
D_DN(4)	AE21	Input	LVDS	DDR	Differential	Data, Negative	737
D_DN(5)	AF20	Input	LVDS	DDR	Differential	Data, Negative	738
D_DN(6)	AL15	Input	LVDS	DDR	Differential	Data, Negative	737
D_DN(7)	AG29	Input	LVDS	DDR	Differential	Data, Negative	738
D_DN(8)	AD22	Input	LVDS	DDR	Differential	Data, Negative	739
D_DN(9)	AG21	Input	LVDS	DDR	Differential	Data, Negative	738
D_DN(10)	AJ23	Input	LVDS	DDR	Differential	Data, Negative	736
D_DN(11)	AJ29	Input	LVDS	DDR	Differential	Data, Negative	737
D_DN(12)	AF28	Input	LVDS	DDR	Differential	Data, Negative	737
D_DN(13)	AK22	Input	LVDS	DDR	Differential	Data, Negative	741
D_DN(14)	AD28	Input	LVDS	DDR	Differential	Data, Negative	739
D_DN(15)	AK28	Input	LVDS	DDR	Differential	Data, Negative	739
D_DP(0)	AJ17	Input	LVDS	DDR	Differential	Data, Positive	737
D_DP(1)	AC29	Input	LVDS	DDR	Differential	Data, Positive	737
D_DP(2)	AK14	Input	LVDS	DDR	Differential	Data, Positive	738
D_DP(3)	AE27	Input	LVDS	DDR	Differential	Data, Positive	737
D_DP(4)	AD20	Input	LVDS	DDR	Differential	Data, Positive	737
D_DP(5)	AF22	Input	LVDS	DDR	Differential	Data, Positive	738
D_DP(6)	AL17	Input	LVDS	DDR	Differential	Data, Positive	737
D_DP(7)	AG27	Input	LVDS	DDR	Differential	Data, Positive	738
D_DP(8)	AE23	Input	LVDS	DDR	Differential	Data, Positive	739
D_DP(9)	AG23	Input	LVDS	DDR	Differential	Data, Positive	738
D_DP(10)	AJ21	Input	LVDS	DDR	Differential	Data, Positive	736
D_DP(11)	AJ27	Input	LVDS	DDR	Differential	Data, Positive	737
D_DP(12)	AF26	Input	LVDS	DDR	Differential	Data, Positive	737
D_DP(13)	AK20	Input	LVDS	DDR	Differential	Data, Positive	740
D_DP(14)	AD26	Input	LVDS	DDR	Differential	Data, Positive	739
D_DP(15)	AK26	Input	LVDS	DDR	Differential	Data, Positive	739
SERIAL CONTROL							
SCTRL_AN	D8	Input	LVDS	DDR	Differential	Serial Control, Negative	736
SCTRL_BN	AK8	Input	LVDS	DDR	Differential	Serial Control, Negative	739
SCTRL_CN	G23	Input	LVDS	DDR	Differential	Serial Control, Negative	737
SCTRL_DN	AH28	Input	LVDS	DDR	Differential	Serial Control, Negative	739
SCTRL_AP	D10	Input	LVDS	DDR	Differential	Serial Control, Positive	736
SCTRL_BP	AK10	Input	LVDS	DDR	Differential	Serial Control, Positive	739
SCTRL_CP	H22	Input	LVDS	DDR	Differential	Serial Control, Positive	739
SCTRL_DP	AH26	Input	LVDS	DDR	Differential	Serial Control, Positive	739

Pin Functions (continued)

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	DESCRIPTION	TRACE (mils) (4)
NAME	NO.						
CLOCKS							
DCLK_AN	H2	Input	LVDS		Differential	Clock, Negative	740
DCLK_BN	AJ5	Input	LVDS		Differential	Clock, Negative	740
DCLK_CN	C23	Input	LVDS		Differential	Clock, Negative	736
DCLK_DN	AH22	Input	LVDS		Differential	Clock, Negative	736
DCLK_AP	H4	Input	LVDS		Differential	Clock, Positive	740
DCLK_BP	AJ3	Input	LVDS		Differential	Clock, Positive	740
DCLK_CP	C21	Input	LVDS		Differential	Clock, Positive	736
DCLK_DP	AH20	Input	LVDS		Differential	Clock, Positive	738
SERIAL COMMUNICATIONS PORT (SCP)							
SCP_DO	AC3	Output	LVCMOS	SDR		Serial Communications Port Output	
SCP_DI	AD2	Input	LVCMOS	SDR	Pull-Down	Serial Communications Port Data Input	
SCP_CLK	AE1	Input	LVCMOS		Pull-Down	Serial Communications Port Clock	
SCP_ENZ	AD4	Input	LVCMOS		Pull-Down	Active-low Serial Communications Port Enable	
MICROMIRROR RESET CONTROL							
RESET_ADDR(0)	H12	Input	LVCMOS		Pull-Down	Reset Driver Address Select	
RESET_ADDR(1)	C5	Input	LVCMOS		Pull-Down	Reset Driver Address Select	
RESET_ADDR(2)	B6	Input	LVCMOS		Pull-Down	Reset Driver Address Select	
RESET_ADDR(3)	A19	Input	LVCMOS		Pull-Down	Reset Driver Address Select	
RESET_MODE(0)	J1	Input	LVCMOS		Pull-Down	Reset Driver Mode Select	
RESET_MODE(1)	G1	Input	LVCMOS		Pull-Down	Reset Driver Mode Select	
RESET_SEL(0)	AK4	Input	LVCMOS		Pull-Down	Reset Driver Level Select	
RESET_SEL(1)	AL13	Input	LVCMOS		Pull-Down	Reset Driver Level Select	
RESET_STROBE	H6	Input	LVCMOS		Pull-Down	Reset Address, Mode, & Level latched on rising-edge	
ENABLES AND INTERRUPTS							
PWRDNZ	B4	Input	LVCMOS			Active-low Device Reset	
RESET_OEZ	AK24	Input	LVCMOS		Pull-Down	Active-low output enable for DMD reset driver circuits	
RESETZ	AL19	Input	LVCMOS		Pull-Down	Active-low sets Reset circuits in known VOFFSET state	
RESET_IRQZ	C3	Output	LVCMOS			Active-low, output interrupt to ASIC	
VOLTAGE REGULATOR MONITORING							
PG_BIAS	J19	Input	LVCMOS		Pull-Up	Active-low fault from external VBIAS regulator	
PG_OFFSET	A13	Input	LVCMOS		Pull-Up	Active-low fault from external VOFFSET regulator	
PG_RESET	AC19	Input	LVCMOS		Pull-Up	Active-low fault from external VRESET regulator	
EN_BIAS	J15	Output	LVCMOS			Active-high enable for external VBIAS regulator	
EN_OFFSET	H30	Output	LVCMOS			Active-high enable for external VOFFSET regulator	
EN_RESET	J17	Output	LVCMOS			Active-high enable for external VRESET regulator	
LEAVE PIN UNCONNECTED							
MBRST(0)	L5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(1)	M28	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(2)	P4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(3)	P30	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(4)	L3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(5)	P28	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(6)	P2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	

Pin Functions (continued)

PIN [1]		TYPE (I/O/P)	SIGNAL	DATA RATE [2]	INTERNAL TERM [3]	DESCRIPTION	TRACE (mils) [4]
NAME	NO.						
MBRST(7)	T28	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(8)	M4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(9)	L29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(10)	T4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(11)	N29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(12)	N3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(13)	L27	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(14)	R3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(15)	V28	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(16)	V4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(17)	R29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(18)	Y4	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(19)	AA27	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(20)	W3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(21)	W27	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(22)	AA3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(23)	W29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(24)	U5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(25)	U29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(26)	Y2	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(27)	AA29	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(28)	U3	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(29)	Y30	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(30)	AA5	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(31)	R27	Output	Analog		Pull-Down	For proper DMD operation, do not connect	
LEAVE PIN UNCONNECTED							
RESERVED_PFE	J11	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_TM	AC7	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_XI0	AC25	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_XI1	AC23	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_XI2	J23	Input	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_TP0	AC9	Input	Analog			For proper DMD operation, do not connect	
RESERVED_TP1	AC11	Input	Analog			For proper DMD operation, do not connect	
RESERVED_TP2	AC13	Input	Analog			For proper DMD operation, do not connect	
LEAVE PIN UNCONNECTED							
RESERVED_BA	AC15	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_BB	J13	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_BC	AC21	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_BD	J21	Output	LVCMOS			For proper DMD operation, do not connect	
RESERVED_TS	AC17	Output	LVCMOS			For proper DMD operation, do not connect	
LEAVE PIN UNCONNECTED							
NO CONNECT	J7					For proper DMD operation, do not connect	
NO CONNECT	J9					For proper DMD operation, do not connect	
NO CONNECT	J25					For proper DMD operation, do not connect	

Pin Functions

PIN		TYPE (I/O/P)	SIGNAL	DESCRIPTION
NAME (1)	NO.			
VBIAS	A3, A9, A5, A11, A7, B2	Power	Analog	Supply voltage for positive Bias level of Micromirror reset signal.
VOFFSET	L1, N1, R1	Power	Analog	Supply voltage for HVCMOS logic.
	U1, W1	Power	Analog	Supply voltage for stepped high voltage at Micromirror address electrodes.
	AC1, AA1	Power	Analog	Supply voltage for Offset level of MBRST(31:0).
VRESET	L31, N31, R31, U31, W31, AA31	Power	Analog	Supply voltage for negative Reset level of Micromirror reset signal.
VCC	A21, A23, A25, A27, A29, C1, C31, E31, G31, J31, K2, AC31, AE31, AG1, AG31, AJ31, AK2, AK30, AL3, AL5, AL7, AL21, AL23, AL25, AL27	Power	Analog	Supply voltage for LVCMOS core logic. Supply voltage for normal high level at Micromirror address electrodes.
VCCI	H18, H24, M6, M26, P6, P26, T6, T26, V6, V26, Y6, Y26, AD6, AD12, AD18, AD24	Power	Analog	Supply voltage for LVDS receivers.
VSS	A1, B12, B18, B24, B30, C7, C13, C19, C25, D6, D12, D18, D24, D30, E1, E7, E13, E19, E25, F6, F12, F18, F24, F30, G7, G13, G19, G25, K4, K6, K26, K28, K30, M2, M30, N5, N27, R5, T2, T30, U27, V2, V30, W5, Y28, AB2, AB4, AB6, AB26, AB28, AB30, AC5, AD30, AE7, AE13, AE19, AE25, AF6, AF12, AF18, AF24, AF30, AG7, AG13, AG19, AG25, AH6, AH12, AH18, AH24, AH30, AJ1, AJ7, AJ13, AJ19, AJ25, AK6, AK12, AK18, AL29	Power	Analog	Device Ground. Common return for all power.

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
SUPPLY VOLTAGES					
VCC	Supply voltage for LVCMOS core logic (2)		–0.5	4	V
VCCI	Supply voltage for LVDS receivers (2)		–0.5	4	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode (2) (3)		–0.5	9	V
VBIAS	Supply voltage for micromirror electrode (2)		–0.5	17	V
VRESET	Supply voltage for micromirror electrode (2)		–11	0.5	V
| VCC – VCCI |	Supply voltage delta (absolute value) (4)			0.3	V
| VBIAS – VOFFSET |	Supply voltage delta (absolute value) (5)			8.75	V
INPUT VOLTAGES					
	Input voltage for all other LVCMOS input pins (2)		–0.5	VCC + 0.3	V
	Input voltage for all other LVDS input pins (2) (6)		–0.5	VCCI + 0.3	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value) (7)			700	mV
I_{ID}	Input differential current (7)			7	mA
CLOCKS					
f_{clock}	DLP9000	Clock frequency for LVDS interface, DCLK_A		440	MHz
		Clock frequency for LVDS interface, DCLK_B		440	
		Clock frequency for LVDS interface, DCLK_C		440	
		Clock frequency for LVDS interface, DCLK_D		440	
	DLP9000X	Clock frequency for LVDS interface, DCLK_A		500	
		Clock frequency for LVDS interface, DCLK_B		500	
		Clock frequency for LVDS interface, DCLK_C		500	
		Clock frequency for LVDS interface, DCLK_D		500	
ENVIRONMENTAL					
T_{ARRAY}	Array temperature: operational (8) (9)		0	90	ºC
	Array temperature: non–operational (9)		-40	90	
T_{WINDOW}	Window temperature: operational		0	70	ºC
	Window temperature: non–operational		-40	90	
$\lvert T_{DELTA} \rvert$	Absolute termperature delta between the window test points and the ceramic test point TP1 (10)			10	ºC
RH	Relative Humidity, operating and non–operating			95%	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(3) VOFFSET supply transients must fall within specified voltages.
(4) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. Refer to *Power Supply Requirements* for additional information.
(6) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(7) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) Exposure of the DMD simultaneously to any combination of the maximum operating conditions for case temperature, differential temperature, or illumination power density may affect device reliability.
(9) The highest temperature of the active array as calculated by the *Micromirror Array Temperature Calculation* using ceramic test point 1 (TP1) in Figure 15.
(10) Temperature delta is the highest difference between the ceramic test point TP1 and window test points TP2 and TP3 in Figure 15.

7.2 Storage Conditions

applicable before the DMD is installed in the final product

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	-40	80	°C
RH	Relative Humidity, (non-condensing)		95%	

7.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES (1) (2)						
VCC	DLP9000	Supply voltage for LVCMOS core logic	3.0	3.3	3.6	V
	DLP9000X	Supply voltage for LVCMOS core logic	3.3	3.45	3.6	
VCCI	DLP9000	Supply voltage for LVDS receivers	3.0	3.3	3.6	V
	DLP9000X	Supply voltage for LVDS receivers	3.3	3.45	3.6	
VOFFSET	Supply voltage for HVCMOS and micromirror electrodes (3)		8.25	8.5	8.75	V
VBIAS	Supply voltage for micromirror electrodes		15.5	16	16.5	V
VRESET			–9.5	–10	–10.5	V
|VCCI–VCC|	Supply voltage delta (absolute value) (4)				0.3	V
|VBIAS–VOFFSET|	Supply voltage delta (absolute value) (5)				8.75	V
LVCMOS PINS						
V_{IH}	High level Input voltage (6)		1.7	2.5	VCC + 0.3	V
V_{IL}	Low level Input voltage (6)		– 0.3		0.7	V
I_{OH}	High level output current at V_{OH} = 2.4 V				–20	mA
I_{OL}	Low level output current at V_{OL} = 0.4 V				15	mA
T_{PWRDNZ}	PWRDNZ pulse width (7)		10			ns
SCP INTERFACE						
f_{clock}	SCP clock frequency (8)				500	kHz
t_{SCP_SKEW}	Time between valid SCPDI and rising edge of SCPCLK (9)		–800		800	ns
t_{SCP_DELAY}	Time between valid SCPDO and rising edge of SCPCLK (9)				700	ns
$t_{SCP\_BYTE\_INTERVAL}$	Time between consecutive bytes		1			µs
$t_{SCP\_NEG\_ENZ}$	Time between falling edge of SCPENZ and the first rising edge of SCPCLK		30			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)		1			µs
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state)				1.5	ns
f_{clock}	SCP circuit clock oscillator frequency (10)		9.6		11.1	MHz

(1) Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) All voltages are referenced to common ground VSS.
(3) VOFFSET supply transients must fall within specified max voltages.
(4) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. Refer to *Power Supply Requirements* for additional information.
(6) Tester Conditions for V_{IH} and V_{IL}:
Frequency = 60 MHz. Maximum Rise Time = 2.5 ns at (20% to 80%)
Frequency = 60 MHz. Maximum Fall Time = 2.5 ns at (80% to 20%)
(7) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
(8) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(9) Refer to Figure 1.
(10) SCP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
LVDS INTERFACE						
f_{clock}	DLP9000	Clock frequency DCLK			400	MHz
	DLP9000X	Clock frequency DCLK (11)	400		480	
$\|V_{ID}\|$	Input differential voltage (absolute value) (12)		100	400	600	mV
V_{CM}	Common mode (12)			1200		mV
V_{LVDS}	LVDS voltage (12)		0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ				10	ns
Z_{IN}	Internal differential termination resistance		95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)		90	100	110	Ω
ENVIRONMENTAL (13) For Illumination Source Between 420 nm and 700 nm						
T_{ARRAY}	DLP9000	Array temperature, Long–term operational (14) (15)(16)	10		40 to 65 (17)	°C
		Array temperature, Short–term operational (14) (15)(18)	0		10	
	DLP9000X	Array temperature, Long–term operational (14) (15)(16)	10		40 (19)	
		Array temperature, Short–term operational (14) (15)(18)	0		10	
T_{WINDOW}	DLP9000	Window Temperature test points TP2 and TP3, Long-term operational(16)	10		70	°C
	DLP9000X	Window Temperature test points TP2 and TP3, Long-term operational(16)	10		40	
$\|T_{DELTA}\|$	Absolute Temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1(20)				10	°C
ILL_{VIS}	Illumination				Thermally Limited (21)	mW/cm^2
RH	Relative Humidity (non-condensing)				95%	
ENVIRONMENTAL (13) For Illumination Source Between 400 nm and 420 nm						
T_{ARRAY}	Array temperature, Long–term operational (14) (15)(16)		20		30	°C
	Array temperature, Short–term operational (14) (15)(18)		0		20	
T_{WINDOW}	Window Temperature test points TP2 and TP3, Long-term operational(16)				30	°C
$\|T_{DELTA}\|$	Absolute Temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1(20)				10	°C
ILL_{VIS}	Illumination				10	W/cm^2
RH	Relative Humidity (non-condensing)				95%	
ENVIRONMENTAL (13) For Illumination Source <400 nm and >700 nm						
T_{ARRAY}	DLP9000	Array temperature, Long–term operational (14) (15)(16)	10		40 to 65 (17)	°C
		Array temperature, Short–term operational (14) (15)(18)	0		10	
	DLP9000X	Array temperature, Long–term operational (14) (15)(16)	10		40 (19)	
		Array temperature, Short–term operational (14) (15)(18)	0		10	

(11) The DLP9000X, coupled with the DLPC910, is designed for operation at 2 specific DCLK frequencies only - 400 MHz or 480 MHz. 480 MHz operation is only allowed at the specific environmental operating conditions as shown in this table.
(12) Refer to Figure 2, Figure 3, and Figure 4.
(13) Optimal, long-term performance and optical efficiency of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(14) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 15 and the package thermal resistance in *Thermal Information* using *Micromirror Array Temperature Calculation*.
(15) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(16) Long-term is defined as the usable life of the device.
(17) Per Figure 16, the maximum operational case temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(18) Array and Window temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(19) For the DLP9000X, Figure 16 does not apply and the maximum temperature is as specified in table.
(20) Temperature delta is the highest difference between the ceramic test point (TP1) and window test points (TP2) and (TP3) in Figure 15.
(21) Refer to *Thermal Information* and *Micromirror Array Temperature Calculation*.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_{WINDOW}	DLP9000	Window Temperature test points TP2 and TP3, Long-term operational (16)	10		70	°C
	DLP9000X	Window Temperature test points TP2 and TP3, Long-term operational (16)	10		40	
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1 (20)				10	°C
ILL_{UV}	Illumination, wavelength < 400 nm				0.68	mW/cm^2
ILL_{IR}	Illumination, wavelength > 700 nm				10	mW/cm^2
RH	Relative Humidity (non-condensing)				95%	

7.5 Thermal Information

THERMAL METRIC (1)		DLP9000 FLS (CLGA) 355 PINS	UNIT
$R_{\theta JA}$	Thermal resistance, active area to test point 1 (TP1) (max)	0.5	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	VCC = 3 V, I_{OH} = –20 mA	2.4			V
V_{OL}	Low level output voltage	VCC = 3.6, I_{OL} = 15 mA			0.4	V
I_{IH}	High–level input current (2) (3)	VCC = 3.6 V, V_I = VCC			250	µA
IIL	Low level input current	VCC = 3.6 V, V_I = 0	–250			µA
I_{OZ}	High–impedance output current	VCC = 3.6 V			10	µA
CURRENT						
I_{CC}	Supply current (4)	DLP9000 VCC = 3.6 V, DCLK=400 MHz			1600	mA
		DLP9000X VCC = 3.6V, DCLK=480 MHz			1850	
I_{CCI}		DLP9000 VCCI = 3.6 V, DCLK=400 MHz			985	
		DLP9000X VCCI = 3.6, DCLK=480 MHz			1100	
I_{OFFSET}	Supply current (5)	VOFFSET = 8.75 V			25	mA
I_{BIAS}		VBIAS = 16.5 V			14	
I_{RESET}	Supply current	VRESET = –10.5 V			11	mA
I_{TOTAL}		DLP9000 Total Sum			2634	
		DLP9000X Total Sum			3000	
POWER						

(1) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) Applies to LVCMOS input pins only. Does not apply to LVDS pins and MBRST pins.
(3) LVCMOS input pins utilize an internal 18000 Ω passive resistor for pull-up and pull-down configurations. Refer to *Pin Configuration and Functions* to determine pull-up or pull-down configuration used.
(4) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
P_{CC}	Supply power dissipation	DLP9000 VCC = 3.6 V			5760	mW
		DLP9000X VCC = 3.6 V			6660	
P_{CCI}		DLP9000 VCCI = 3.6 V			3546	mW
		DLP9000X VCCI = 3.6 V			3960	
P_{OFFSET}		VOFFSET = 8.75 V			219	mW
P_{BIAS}		VBIAS = 16.5 V			231	mW
P_{RESET}		VRESET = –10.5 V			115	mW
P_{TOTAL}	Supply power dissipation (6)	DLP9000 Total Sum, DCLK = 400 MHz			9871	mW
		DLP9000X Total Sum, DCLK = 480 MHz			11185	
CAPACITANCE						
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Output capacitance	f = 1 MHz			10	pF
	Reset group capacitance MBRST(31:0)	f = 1 MHz; 2560 × 50 micromirrors	230		290	pF

(6) Total power on the active micromirror array is the sum of the electrical power dissipation and the absorbed power from the illumination source. See the *Micromirror Array Temperature Calculation*.

7.7 Timing Requirements

over *Recommended Operating Conditions* (unless otherwise noted) (1)

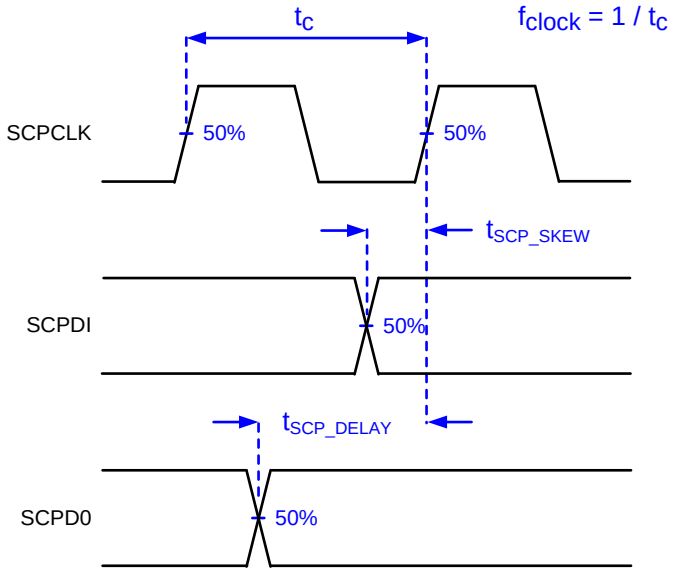
				MIN	NOM	MAX	UNIT
SCP INTERFACE (2)							
t_r	Rise time	20% to 80%				200	ns
t_f	Fall time	80% to 20%				200	ns
LVDS INTERFACE (2)							
t_r	Rise time	20% to 80%		100		400	ps
t_f	Fall time	80% to 20%		100		400	ps
LVDS CLOCKS (3)							
t_c	Cycle time	DLP9000	DCLK_A, 50% to 50%	2.5			ns
			DCLK_B, 50% to 50%	2.5			
			DCLK_C, 50% to 50%	2.5			
			DCLK_D, 50% to 50%	2.5			
		DLP9000X	DCLK_A, 50% to 50%	2.083			
			DCLK_B, 50% to 50%	2.083			
			DCLK_C, 50% to 50%	2.083			
			DCLK_D, 50% to 50%	2.083			
t_w	Pulse duration	DLP9000	DCLK_A, 50% to 50%	1.19	1.25		ns
			DCLK_B, 50% to 50%	1.19	1.25		
			DCLK_C, 50% to 50%	1.19	1.25		
			DCLK_D, 50% to 50%	1.19	1.25		
		DLP9000X	DCLK_A, 50% to 50%	1.031	1.042		
			DCLK_B, 50% to 50%	1.031	1.042		
			DCLK_C, 50% to 50%	1.031	1.042		
			DCLK_D, 50% to 50%	1.031	1.042		
LVDS INTERFACE (3)							
t_{su}	Setup time	D_A(15:0) before rising or falling edge of DCLK_A		0.2			ns
		D_B(15:0) before rising or falling edge of DCLK_B		0.2			
		D_C(15:0) before rising or falling edge of DCLK_C		0.2			
		D_D(15:0) before rising or falling edge of DCLK_D		0.2			
t_{su}	Setup time	SCTRL_A before rising or falling edge of DCLK_A		0.2			ns
		SCTRL_B before rising or falling edge of DCLK_B		0.2			
		SCTRL_C before rising or falling edge of DCLK_C		0.2			
		SCTRL_D before rising or falling edge of DCLK_D		0.2			
t_h	Hold time	DLP9000	D_A(15:0) after rising or falling edge of DCLK_A	0.5			ns
			D_B(15:0) after rising or falling edge of DCLK_B	0.5			
			D_C(15:0) after rising or falling edge of DCLK_C	0.5			
			D_D(15:0) after rising or falling edge of DCLK_D	0.5			
		DLP9000X	D_A(15:0) after rising or falling edge of DCLK_A	0.4			
			D_B(15:0) after rising or falling edge of DCLK_B	0.4			
			D_C(15:0) after rising or falling edge of DCLK_C	0.4			
			D_D(15:0) after rising or falling edge of DCLK_D	0.4			
t_h	Hold time	DLP9000	SCTRL_A after rising or falling edge of DCLK_A	0.5			ns
			SCTRL_B after rising or falling edge of DCLK_B	0.5			
			SCTRL_C after rising or falling edge of DCLK_C	0.5			
			SCTRL_D after rising or falling edge of DCLK_D	0.5			
		DLP9000X	SCTRL_A after rising or falling edge of DCLK_A	0.4			
			SCTRL_B after rising or falling edge of DCLK_B	0.4			
			SCTRL_C after rising or falling edge of DCLK_C	0.4			
			SCTRL_D after rising or falling edge of DCLK_D	0.4			

(1) Refer to *Pin Configuration and Functions* for pin details.
(2) Refer to Figure 5.
(3) Refer to Figure 6.

Timing Requirements (continued)

over *Recommended Operating Conditions* (unless otherwise noted) (1)

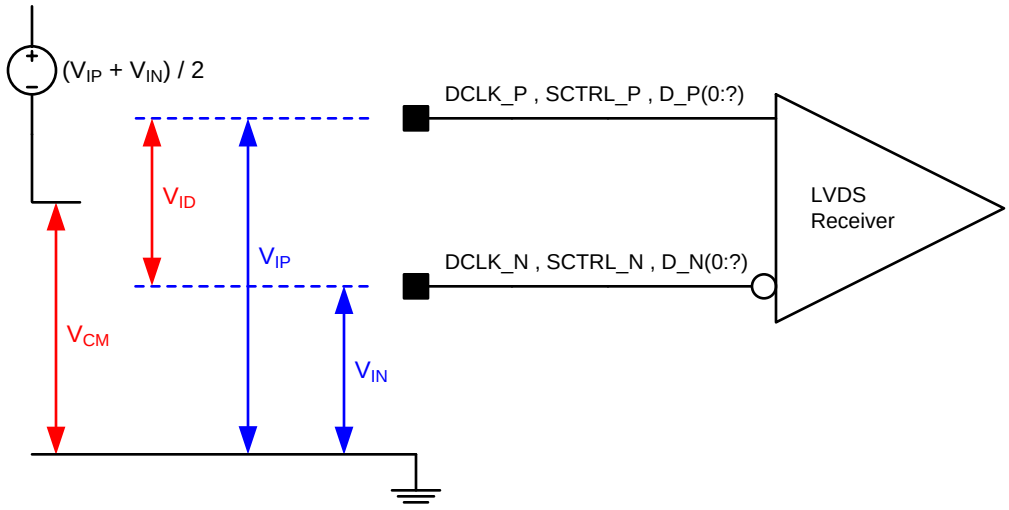
				MIN	NOM	MAX	UNIT
LVDS INTERFACE (3)							
t_{skew}	Skew time	Channel B relative to Channel A	DLP9000 Channel A includes the following LVDS pairs: DCLK_AP and DCLK_AN SCTRL_AP and SCTRL_AN D_AP(15:0) and D_AN(15:0)	–1.25		1.25	ns
			DLP9000 Channel B includes the following LVDS pairs: DCLK_BP and DCLK_BN SCTRL_BP and SCTRL_BN D_BP(15:0) and D_BN(15:0)				
			DLP9000X Channel A includes the following LVDS pairs: DCLK_AP and DCLK_AN SCTRL_AP and SCTRL_AN D_AP(15:0) and D_AN(15:0)	-1.04		1.04	ns
			DLP9000X Channel B includes the following LVDS pairs: DCLK_BP and DCLK_BN SCTRL_BP and SCTRL_BN D_BP(15:0) and D_BN(15:0)				
		Channel D relative to Channel C	DLP9000 Channel C includes the following LVDS pairs: DCLK_CP and DCLK_CN SCTRL_CP and SCTRL_CN D_CP(15:0) and D_CN(15:0)	–1.25		1.25	ns
			DLP9000 Channel D includes the following LVDS pairs: DCLK_DP and DCLK_DN SCTRL_DP and SCTRL_DN D_DP(15:0) and D_DN(15:0)				
			DLP9000X Channel C includes the following LVDS pairs: DCLK_CP and DCLK_CN SCTRL_CP and SCTRL_CN D_CP(15:0) and D_CN(15:0)	-1.04		1.04	ns
			DLP9000X Channel D includes the following LVDS pairs: DCLK_DP and DCLK_DN SCTRL_DP and SCTRL_DN D_DP(15:0) and D_DN(15:0)				



Not to scale.

Refer to SCP Interface section of the Recommended Operating Conditions table.

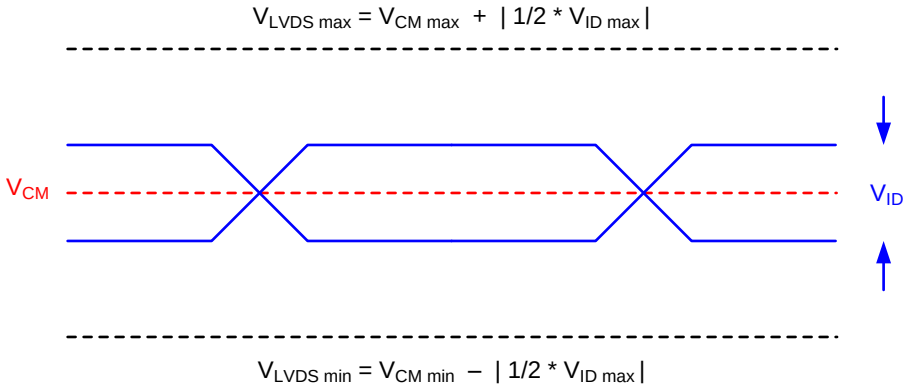
Figure 1. SCP Timing Parameters



Refer to LVDS Interface section of the Recommended Operating Conditions table.

Refer to Pin Configuration and Functions for list of LVDS pins.

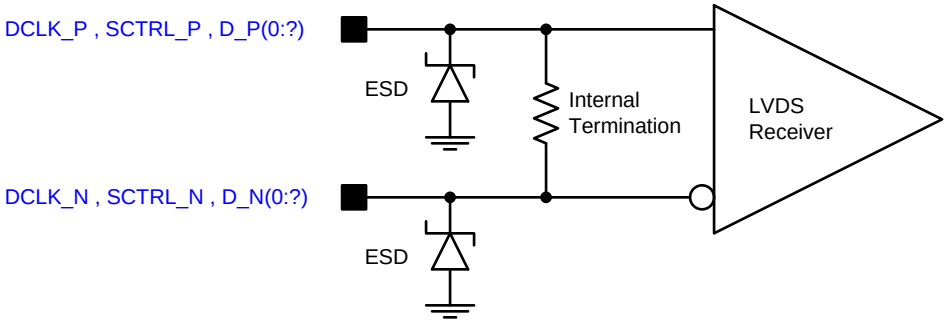
Figure 2. LVDS Voltage Definitions (References)



Not to scale.

Refer to LVDS Interface section of the Recommended Operating Conditions table.

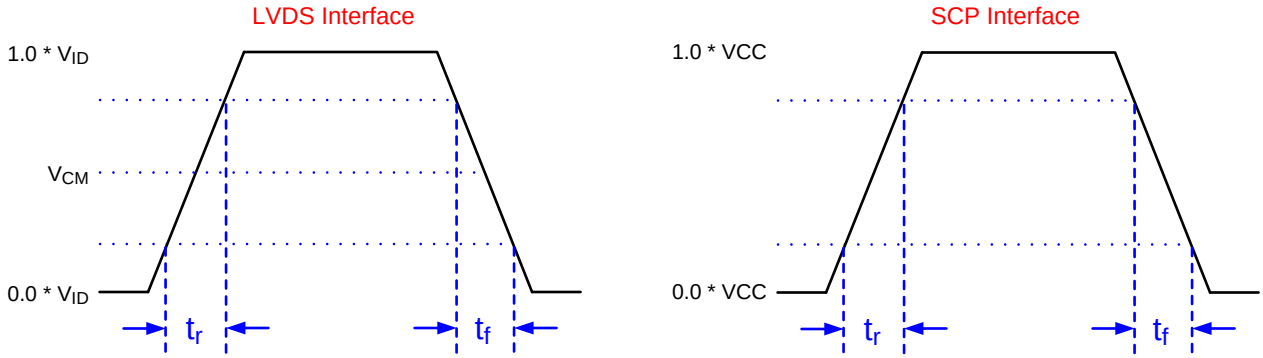
Figure 3. LVDS Voltage Parameters



Refer to LVDS Interface section of the Recommended Operating Conditions table.

Refer to Pin Configuration and Functions for list of LVDS pins.

Figure 4. LVDS Equivalent Input Circuit

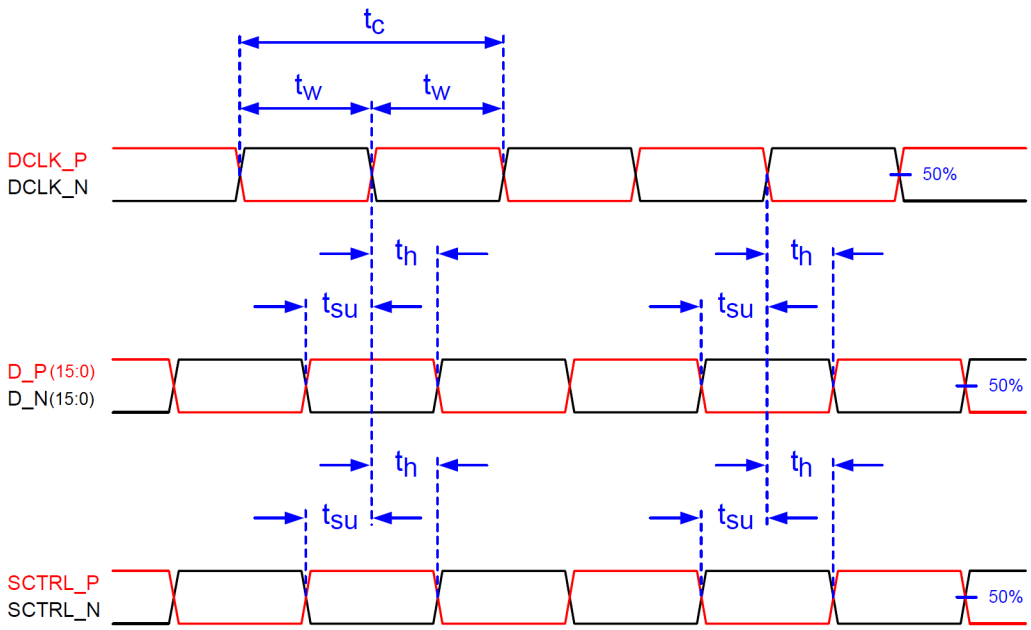


Not to scale.

Refer to the Timing Requirements table

Refer to Pin Configuration and Functions for a list of LVDS pins and SCP pins..

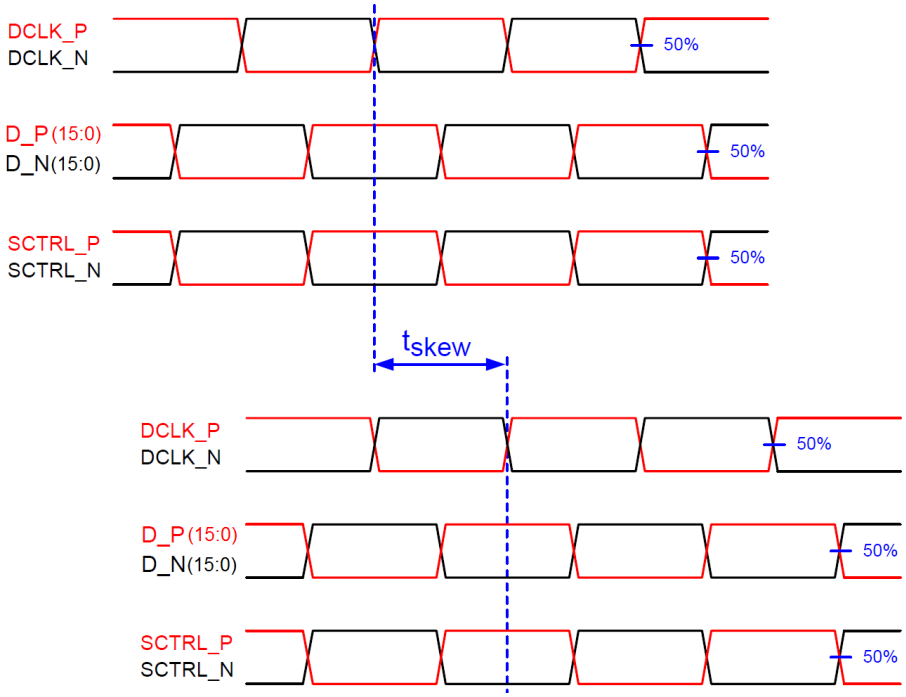
Figure 5. Rise Time and Fall Time



Not to scale.

Refer to LVDS INTERFACE section in the Timing Requirements table.

Figure 6. Timing Requirement Parameter Definitions



Not to scale.

Refer to LVDS INTERFACE section in the Timing Requirements table.

Figure 7. LVDS Interface Channel Skew Definition

7.8 Capacitance at Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_I	Input capacitance	f = 1 MHz		10	pF
C_O	Output capacitance	f = 1 MHz		10	pF
C_{IM}	MBRST(31:0) input capacitance	f = 1 MHz. All inputs interconnected.	230	290	pF

7.9 Typical Characteristics

When the DLP9000 DMD is controlled by two DLPC900 controllers, these digital controllers offer four modes of operation.

1. Video Mode
2. Video Pattern Mode
3. Pre-Stored Pattern Mode
4. Pattern On-The-Fly Mode

In video mode, the video source is displayed on the DMD at the rate of the incoming video source.

In modes 2, 3, and 4, the pattern rates depend on the bit depth as shown in Table 1.

When the DLP9000X DMD is controlled by the DLPC910 controller, the digital controller offers streaming 1-bit binary patterns to the DMD at speeds greater than 61 Gigabits per second (Gbps). The patterns are streamed from a customer designed applications processor into the DLPC910 input LVDS data interface. Table 2 shows the pattern rates for the different DMD Reset Modes.

Table 1. DLPC900 with DLP9000 Pattern Rate versus Bit Depth

BIT DEPTH	VIDEO PATTERN MODE (Hz)	PRE-STORED or PATTERN ON-THE-FLY MODE (Hz)
1	2880	9523
2	1440	3289
3	960	2638
4	720	1364
5	480	823
6	480	672
7	360	500
8	247	247

Table 2. DLPC910 with DLP9000X Pattern Rates versus Reset Mode

RESET MODE(1)	MAX PIXEL DATA RATE (Gbps)(2)	MAX PATTERN RATE (Hz) (3)
Global	53.42	13043(4)
Single	56.46	13783 (5)
Dual	59.89	14624 (5)
Quad	61.39	14989(5)

(1) Refer to the DLPC910 data sheet in *Related Documentation* for a description of the reset modes.
(2) Pixel data rates are based on continuous streaming.
(3) Increasing exposure periods may be necessary for a desired application but may decrease pattern rate.
(4) Global reset mode allows for continuous or pulsed illumination source.
(5) This reset mode typically requires pulsed illumination such as a laser or LED.

7.10 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Thermal interface area (See Figure 8)			35	lbs
	Electrical interface area			300	lbs
	Datum *A* interface area (1)			160	lbs

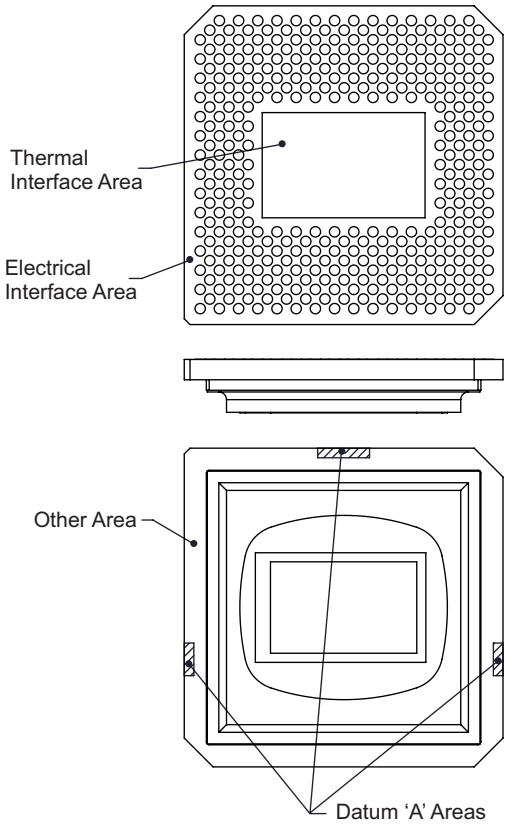
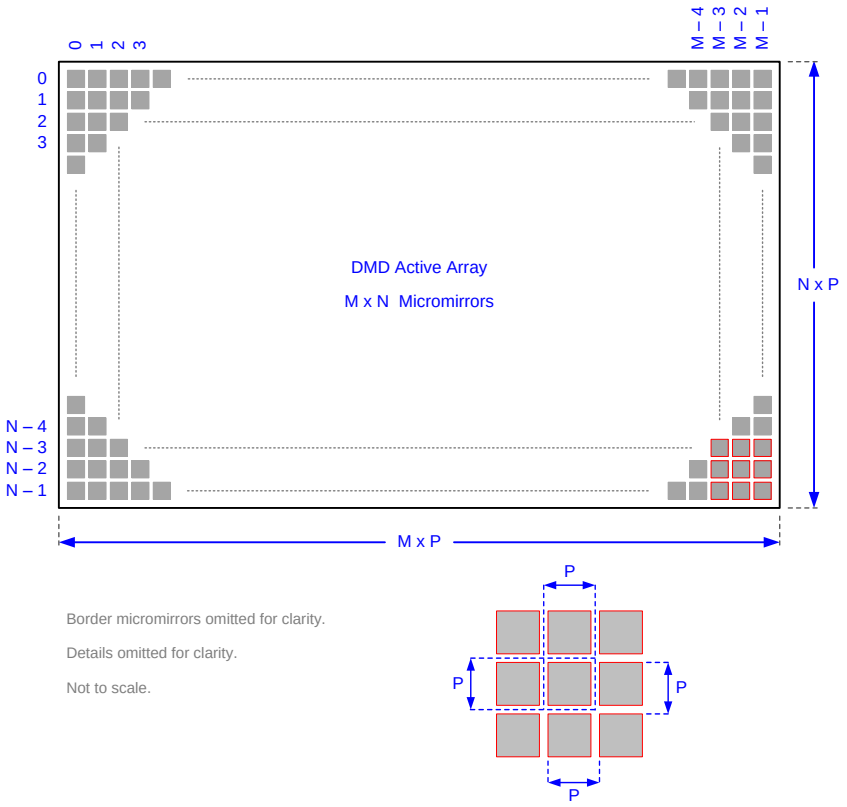


Figure 8. System Mounting Interface Loads

7.11 Micromirror Array Physical Characteristics

				VALUE	UNIT
M	Number of active columns		See Figure 9	2560	micromirrors
N	Number of active rows			1600	micromirrors
P	Micromirror (pixel) pitch			7.56	µm
	Micromirror active array width	M × P		19.3536	mm
	Micromirror active array height	N × P		12.096	mm
	Micromirror active border	Pond of micromirror (POM) (1)		14	micromirrors/ side
	Micromirror total area	P^2 x M x N (converted to cm)		2.341	cm^2

(1) Combined loads of the thermal and electrical interface areas in excess of Datum "A" load shall be evenly distributed outside the Datum *A* area (300 + 35 – Datum *A*).
(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 9. Micromirror Array Physical Characteristics

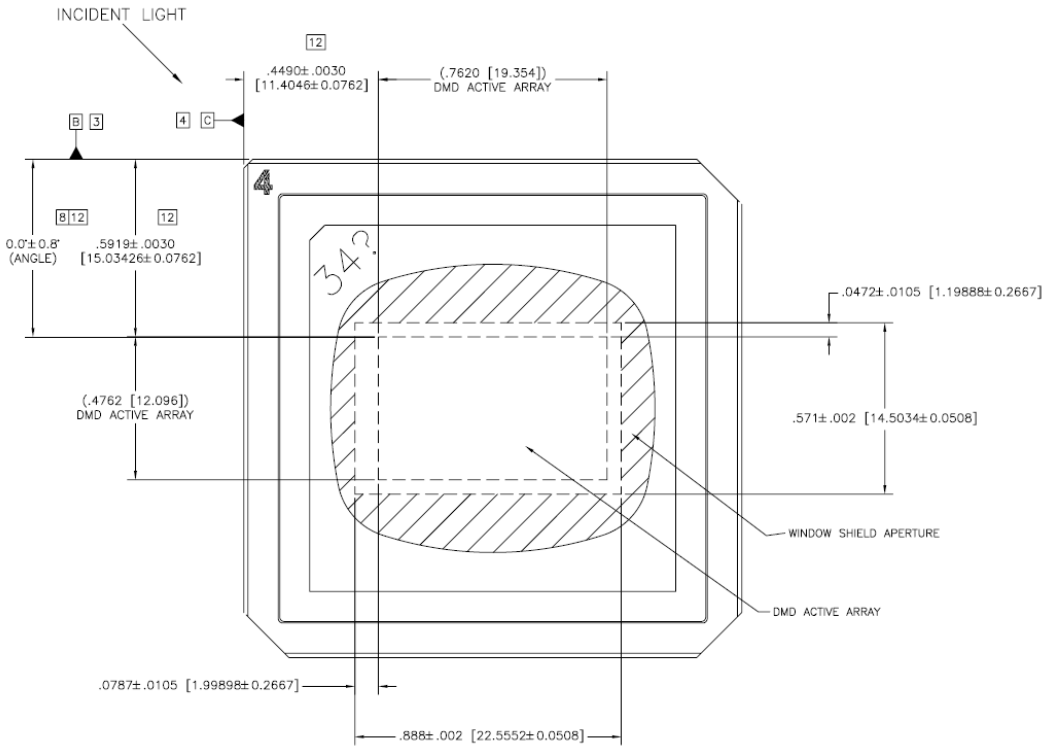


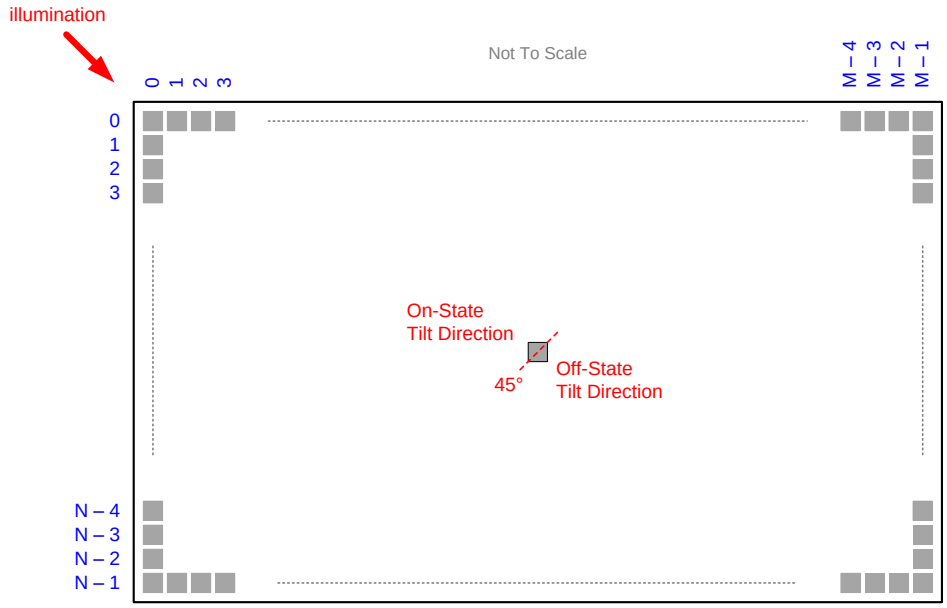
Figure 10. DMD Micromirror Active Area

7.12 Micromirror Array Optical Characteristics

Refer to *Optical Interface and System Image Quality* for important information.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD landed state (1)		12		°
β	Micromirror tilt angle tolerance (1) (2) (3) (4) (5)		–1		1	°
	Micromirror tilt direction (5) (6)	See Figure 11	44	45	46	°
	Number of out-of-specification micromirrors (7)	Adjacent micromirrors			0	micromirrors
		Non-adjacent micromirrors			10	
	Micromirror crossover time (8) (9)	Typical performance		2.5		µs
	DMD efficiency within the wavelength range 400 nm to 420 nm (10)			68%		
	DMD photopic efficiency within the wavelength range 420 nm to 700 nm (10)			66%		

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(7) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.
(8) Micromirror crossover time is primarily a function of the natural response time of the micromirrors.
(9) Performance as measured at the start of life.
(10) Efficiency numbers assume 24-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 11. Micromirror Landed Orientation and Tilt

7.13 Optical and System Image Quality

Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in a) through c) below:

a. Numerical Aperture and Stray Light Control. The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

b. Pupil Match. TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

c. Illumination Overfill. Overfill light illuminating the area outside the active array can create artifacts from the mechanical features that surround the active array and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere outside the active array more than 20 pixels from the edge of the active array on all sides. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the outside of the active array may still cause artifacts to still be visible.

NOTE

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED ABOVE.

7.14 Window Characteristics

PARAMETER (1)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Window material designation	Corning 7056				
Window refractive index	at wavelength 589 nm		1.487		
Window aperture	See (2)				
Illumination overfill	Refer to *Illumination Overfill*				
Window transmittance, single–pass through both surfaces and glass (3)	At wavelength 405 nm. Applies to 0° and 24° AOI only.	95%			
	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) Refer to *Window Characteristics and Optics* for more information.
(2) For details regarding the size and location of the window aperture, refer to the package mechanical characteristics listed in the Mechanical ICD in the Mechanical, Packaging, and Orderable Information section.
(3) Refer to the TI application report DLPA031, *Wavelength Transmittance Considerations for DMD Window*.

7.15 Chipset Component Usage Specification

The DMD is a component of one or more DLP® chipsets. Reliable function and operation of the DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DMD.

8 Parameter Measurement Information

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 12 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Refer to the *Application and Implementation* section.

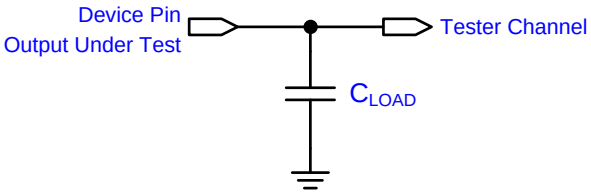


Figure 12. Test Load Circuit

9 Detailed Description

9.1 Overview

The DMD is a 0.9 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and square grid pixel arrangement are shown in Figure 9.

The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS), Double Data Rate (DDR).

The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of *M* memory cell columns by *N* memory cell rows. Refer to the *Functional Block Diagram*.

The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

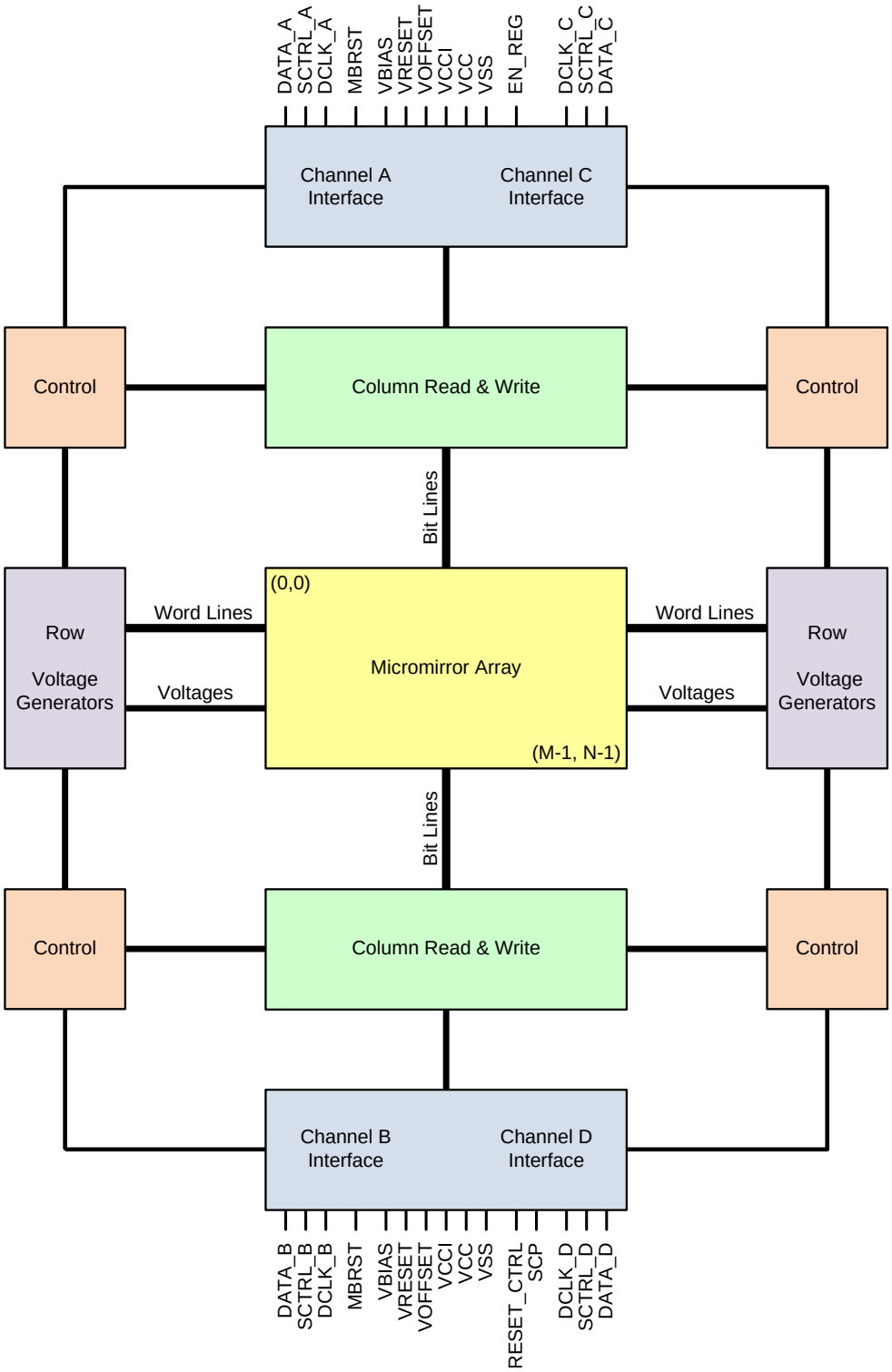
Each cell of the *M* × *N* memory array drives its true and complement ('Q' and 'QB') data to two electrodes underlying one micromirror, one electrode on each side of the diagonal axis of rotation. Refer to *Micromirror Array Optical Characteristics*. The micromirrors are electrically tied to the micromirror reset signals (MBRST) and the micromirror array is divided into reset groups.

Electrostatic potentials between a micromirror and its memory data electrodes cause the micromirror to tilt toward the illumination source in a DLP projection system or away from it, thus reflecting its incident light into or out of an optical collection aperture. The positive (+) tilt angle state corresponds to an 'on' pixel, and the negative (–) tilt angle state corresponds to an 'off' pixel.

Refer to *Micromirror Array Optical Characteristics* for the ± tilt angle specifications. Refer to *Pin Configuration and Functions* for more information on micromirror reset control.

9.2 Functional Block Diagram

Not to Scale. Details Omitted for Clarity. See Accompanying Notes in this Section.



For pin details on Channels A, B, C, and D, refer to *Pin Configuration and Functions* and LVDS Interface section of *Timing Requirements*.

9.3 Feature Description

The DMD consists of 4096000 highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional orthogonal pixel array. Refer to Figure 9 and Figure 13.

Each aluminum micromirror is switchable between two discrete angular positions, –α and +α. The angular positions are measured relative to the micromirror array plane, which is parallel to the silicon substrate. Refer to *Micromirror Array Optical Characteristics* and Figure 14.

The parked position of the micromirror is not a latched position and is therefore not necessarily perfectly parallel to the array plane. Individual micromirror flat state angular positions may vary. Tilt direction of the micromirror is perpendicular to the hinge-axis. The on-state landed position is directed toward the left-top edge of the package, as shown in Figure 13.

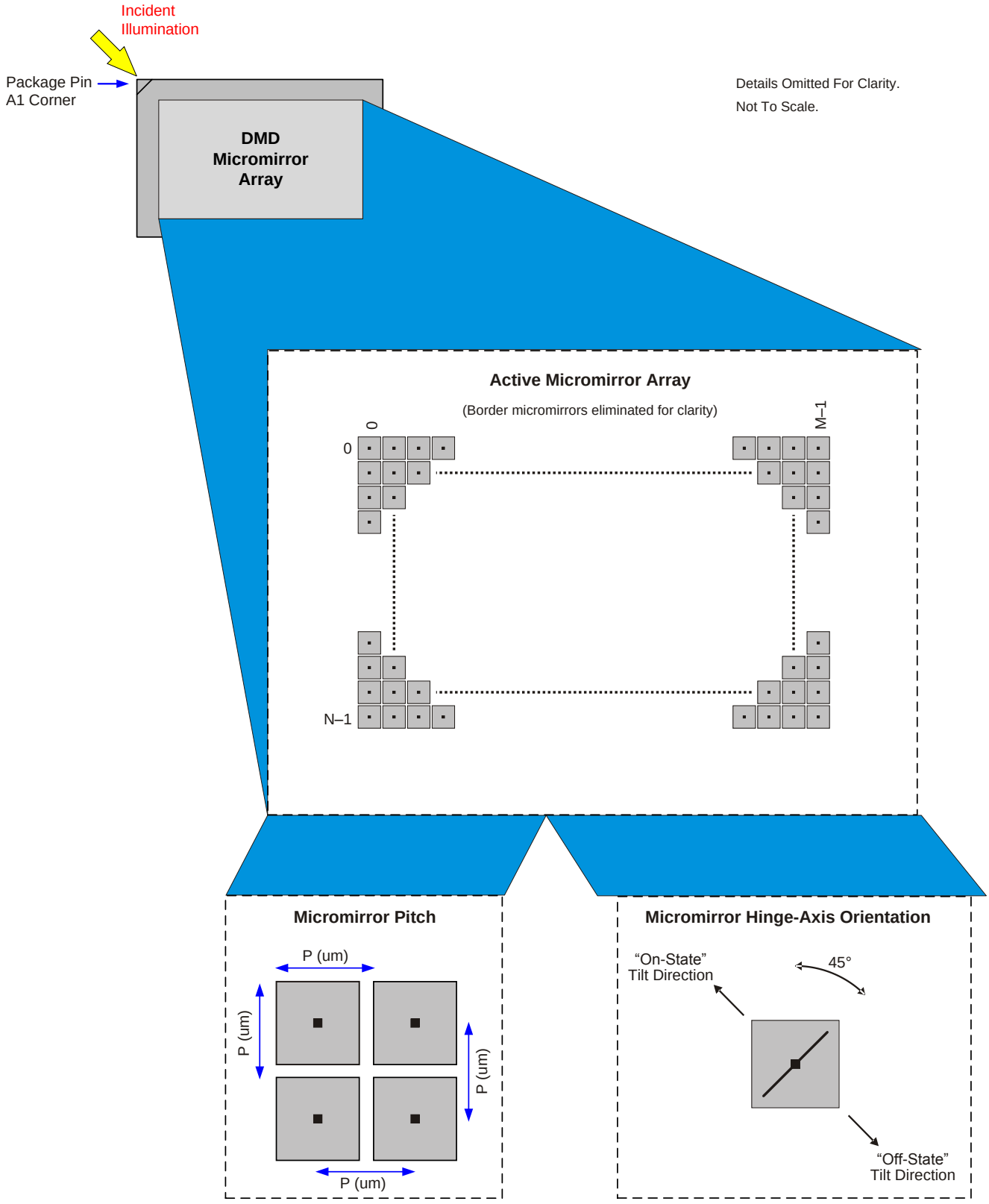
Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror clocking pulse is applied. The angular position (–α and +α) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update.

Writing logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a +α position. Writing logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a – α position.

Updating the angular position of the micromirror array consists of two steps. First, update the contents of the CMOS memory. Second, apply a micromirror reset (also referred as Mirror Clocking Pulse) to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror reset pulses are generated internally by the DMD, with application of the pulses being coordinated by the DLPC900 or the DLPC910 digital controller.

For more information, refer to the TI application report DLPA008, *DMD101: Introduction to Digital Micromirror Device (DMD) Technology*.

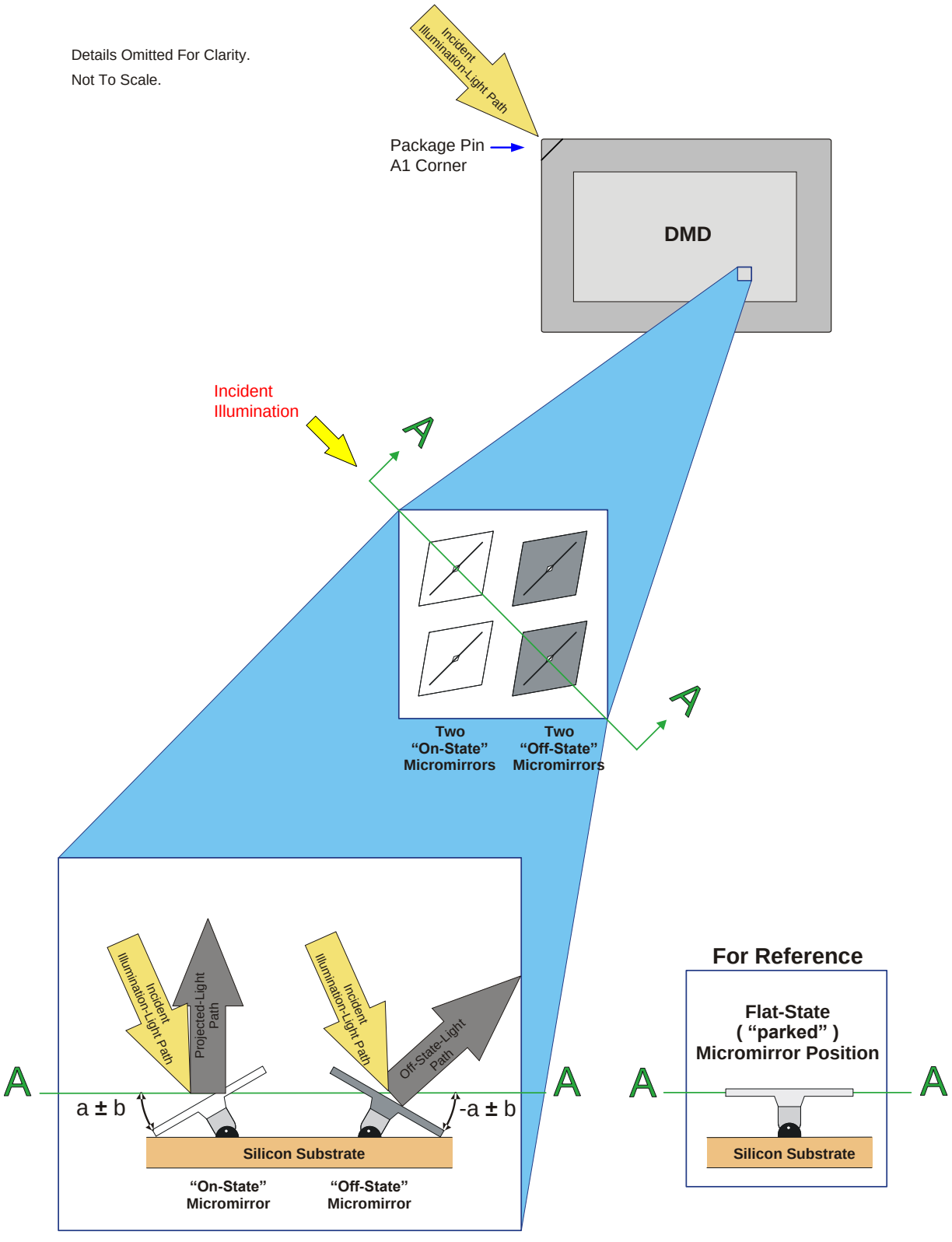
Feature Description (continued)



Refer to *Micromirror Array Physical Characteristics* , Figure 9, and Figure 11.

Figure 13. Micromirror Array, Pitch, Hinge Axis Orientation

Feature Description (continued)



Micromirror States: On, Off, Flat

Figure 14. Micromirror States: On, Off, Flat

9.4 Device Functional Modes

9.4.1 DLP9000

The DLP9000 DMD is controlled by two DLPC900 digital controllers. The digital controller operates in two different modes. The first is video mode where the video source is displayed on the DMD. The second is Pattern mode, where the patterns are downloaded over USB or pre-stored in flash memory, and then streamed to the DMD. The resulting DMD pattern rate depends on which mode and bit-depth is selected. For more information, refer to the DLPC900 data sheet listed under *Related Documentation*.

9.4.2 DLP9000X

The DLP9000X DMD is controlled by one DLPC910 digital controller. The digital controller offers high speed streaming mode where 1-bit binary patterns are accepted at the LVDS interface input, and then streamed to the DMD. To ensure reliable operation, the DLP9000X must always be used with the DLPC910. For more information, refer to the DLPC910 data sheet listed under *Related Documentation*.

9.5 Window Characteristics and Optics

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

9.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

9.5.2 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

9.5.3 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

9.5.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

9.6 Micromirror Array Temperature Calculation

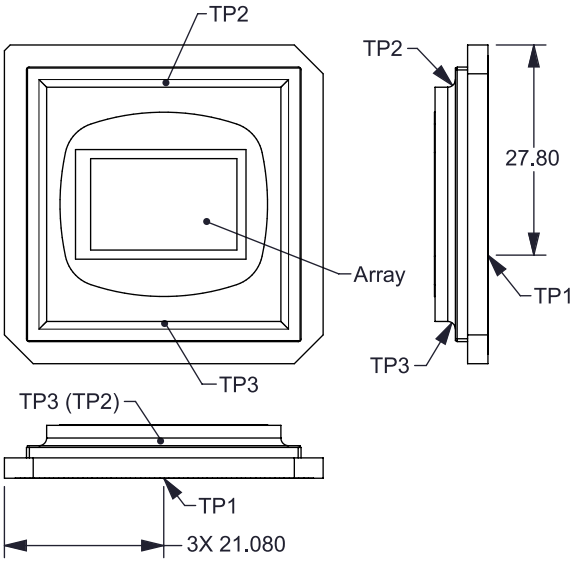


Figure 15. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL) \quad (3)$$

Where:

T_{ARRAY} = Computed micromirror array temperature (°C)
$T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in Figure 15
$R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from micromirror array to outside ceramic (°C/W) specified in *Thermal Information*
Q_{ARRAY} = Total DMD power; electrical, specified in *Electrical Characteristics*, plus absorbed (calculated) (W)
$Q_{ELECTRICAL}$ = DMD electrical power dissipation (W), specified in *Electrical Characteristics*
C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
SL = Measured ANSI screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above produce a total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00274 W/lm.

Sample Calculation for typical projection application:

$T_{CERAMIC}$ = 55°C, assumed system measurement; refer to *Recommended Operating Conditions* regarding specific limits.
SL = 2000 lm
$Q_{ELECTRICAL}$ = 9.87W for the DLP9000 (refer to the power specifications in *Electrical Characteristics*)
C_{L2W} = 0.00274 W/lm

Micromirror Array Temperature Calculation (continued)

Q_{ARRAY} = 9.87 W + (0.00274 W/lm × 2000 lm) = 15.35 W
T_{ARRAY} = 55°C + (15.35 W × 0.5 ºC/W) = 62.68°C

9.7 Micromirror Landed-On/Landed-Off Duty Cycle

9.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On–state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On-state 100% of the time (and in the Off-state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off-state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

9.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

Individual DMD mirror duty cycles vary by application as well as the mirror location on the DMD within any specific application. DMD mirror useful life are maximized when every individual mirror within a DMD approaches 50/50 (or 1/1) duty cycle. Therefore, for the DLPC900 and DLP9000 chipset, it is recommended that *DMD Idle Mode* be enabled as often as possible. Examples are whenever the system is idle, the illumination is disabled, between sequential pattern exposures (if possible), or when the exposure pattern sequence is stopped for any reason. This software mode provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the on and off states. Refer to the DLPC900 Programmer's Guide DLPU018 for a description of the *DMD Idle Mode* command. For the DLPC910 and DLP9000X chipset, it is recommended the controlling applications processor provide a 50/50 pattern sequence to the DLPC910 for display on the DLP9000X as often as possible, similar to the above examples stated for the DLPC900. The pattern provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the on and off states.

9.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 16. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a give long-term average Landed Duty Cycle.

Micromirror Landed-On/Landed-Off Duty Cycle (continued)

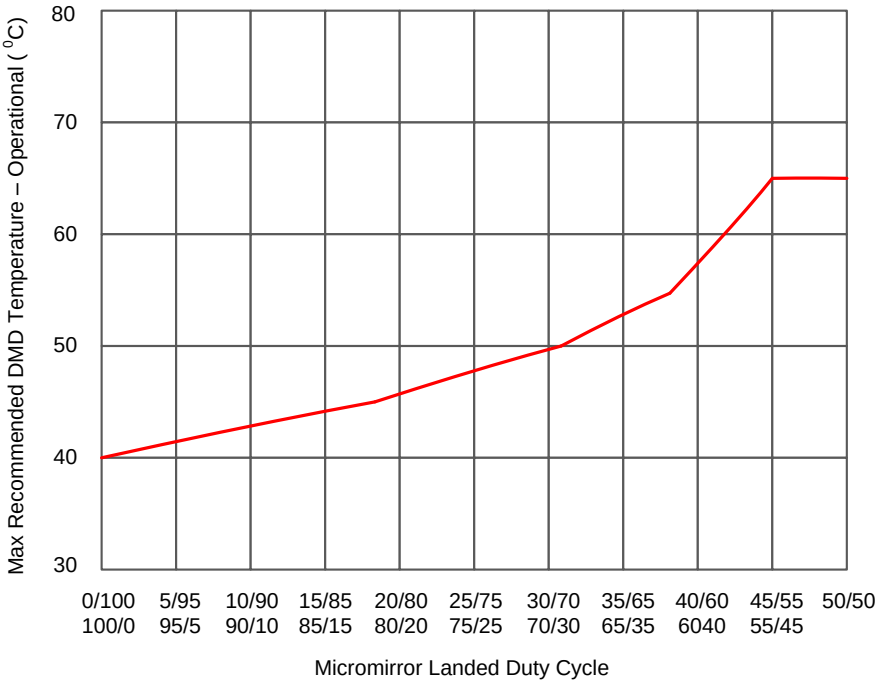


Figure 16. Max Recommended DMD Temperature – Derating Curve

9.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 3.

Table 3. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

Where:

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 4.

Table 4. Example Landed Duty Cycle for Full-Color

RED CYCLE PERCENTAGE 50%	GREEN CYCLE PERCENTAGE 20%	BLUE CYCLE PERCENTAGE 30%	LANDED DUTY CYCLE
RED SCALE VALUE	GREEN SCALE VALUE	BLUE SCALE VALUE	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DLP9000 DMD is controlled by two DLPC900 controllers. This chipset offers two modes of operation. The first is video mode where the video source is displayed on the DMD. The second is Pattern mode, where the patterns are pre-stored in flash memory and then streamed to the DMD. The allowed DMD pattern rate depends on which mode and bit-depth is selected.

The DLP9000X DMD is controlled by the DLPC910 controller, where the DLPC910 is configured by the program content in the DLPR910. This chipset offers streaming 1-bit binary patterns to the DMD at speeds greater than 61 Gigabits per second (Gbps). The patterns are streamed from an customer designed processor into the DLPC910 LVDS input data interface.

Both the DLP9000 and the DLP9000X provide solutions for many varied applications including structured light, 3-D printing, video projection, and high speed lithography. The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data being used.

10.2 Typical Applications

10.2.1 Typical Application using DLP9000

A typical embedded system application using two DLPC900 controllers and a DLP9000 DMD is shown in Figure 17. In this configuration, the DLPC900 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. The 24-bit parallel data must be split between a left half and a right half, each half between the two controllers. The external processor must format each half to consist of 1280x1600 plus any horizontal and vertical blanking at half the pixel clock rate. This system configuration supports still and motion video as well as sequential pattern modes. For more information, refer to the DLPC900 digital controller data sheet listed under *Related Documentation*.

Typical Applications (continued)

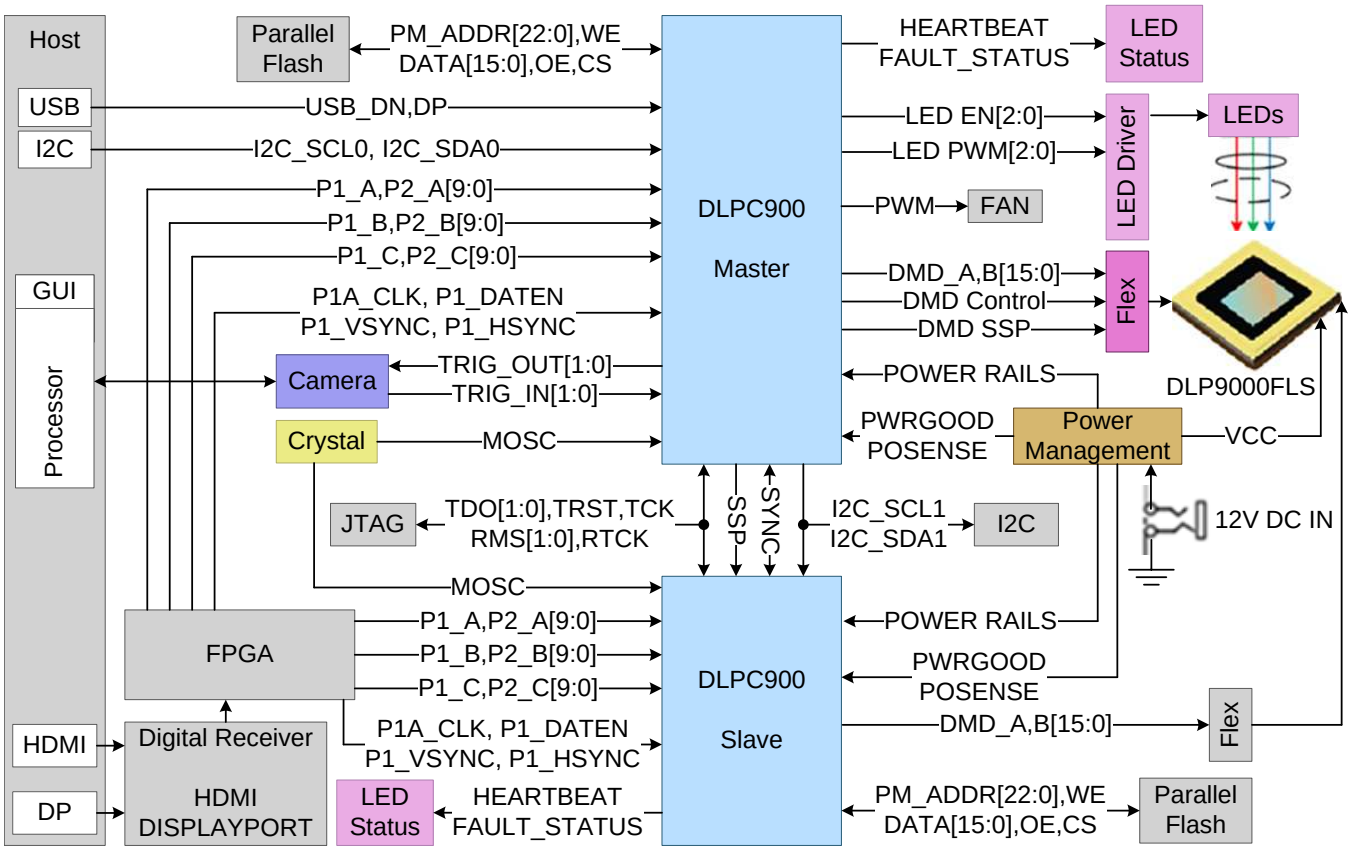


Figure 17. DLP9000 Typical Application Schematic

10.2.1.1 Design Requirements

Detailed design requirements are located in the DLPC900 or the DLPC910 digital controller data sheets. Refer to the data sheets listed under *Related Documentation*.

10.2.1.2 Detailed Design Procedure

Reference Design material exists for systems using either the DLP9000 or the DLP9000X DMD with their respective Controllers. This reference material includes reference board schematics, PCB layouts, and Bills of Materials. Layout guidelines for boards utilizing these controllers and DMDs can be found in the respective DLPC900 or DLPC910 Controller data sheets. For more information, please refer to the individual controller data sheets listed under *Related Documentation*.

10.2.2 Typical Application Using DLP9000X

Direct-write digital imaging is regularly used in high-end lithography printing. This mask-less technology offers a continuous run of printing by changing the digitally created patterns without stopping the imaging head. Figure 18 shows a system where a DLPC910 digital controller is coupled with the DLP9000X DMD. This system offers an ideal back-end imager that takes in digital images at 2560 x 1600 in resolution to achieve speeds of more than 61 Gbps. For more information, refer to the DLPC910 digital controller data sheet listed under *Related Documentation*.

Typical Applications (continued)

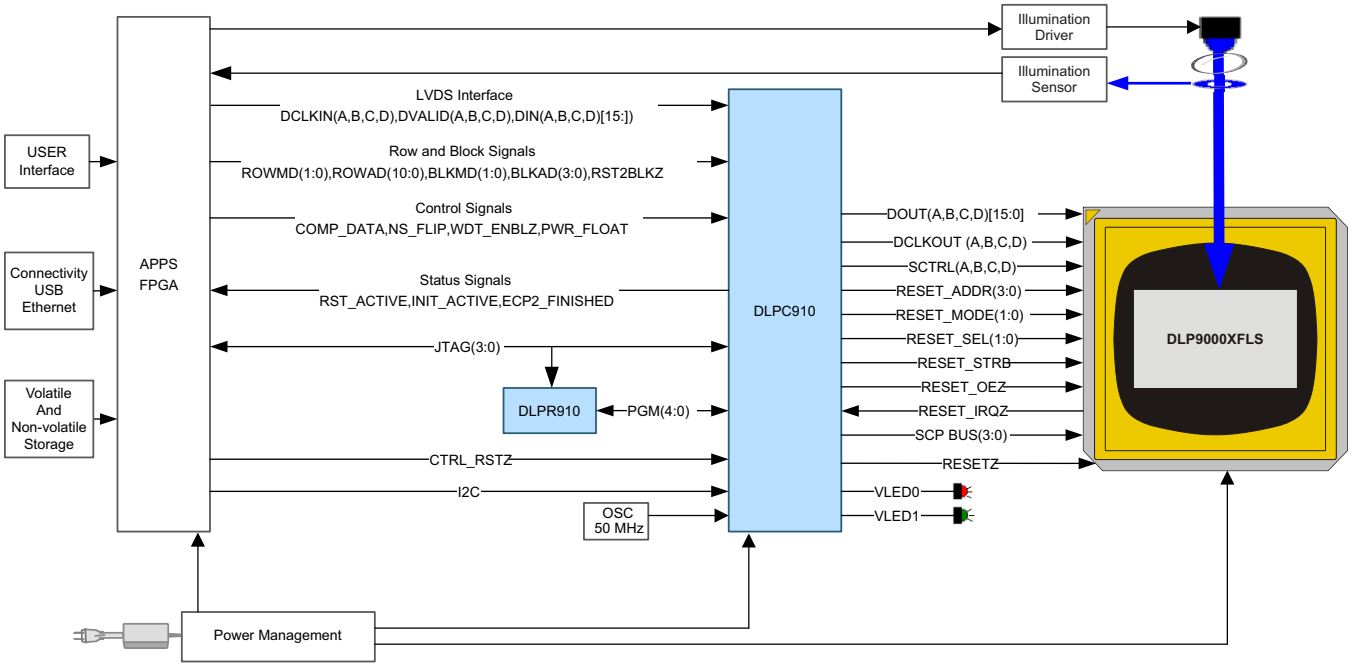


Figure 18. DLP9000X Typical Application Schematic

11 Power Supply Requirements

11.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC900 or DLPC910 Controllers within their associated reference designs.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VCC, VCCI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. VSS must also be connected. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 19.

11.2 DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions*. *During power-up, VBIAS does not have to start after VOFFSET.*
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates requirements during power-up are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Figure 19.
- During power-up, LVCMOS input pins shall not be driven high until after VCC and VCCI have settled at operating voltages listed in *Recommended Operating Conditions*.

11.3 DMD Mirror Park Sequence Requirements

11.3.1 DLP9000

For correct power down operation of the DLP9000 DMD, the following power down procedure must be executed.

Prior to an anticipated power removal, the controlling applications processor must command the DLPC900 to enter Standby mode by using the *Power Mode* command and then wait for a minimum of 20 ms to allow the DLPC900 to complete the power down procedure. This procedure will assure the mirrors are in a flat state. Following this procedure, the power can be safely removed.

In the event of an unanticipated power loss, the power management system must detect the input power loss, command the DLPC900 to enter Standby mode by using the *Power Mode* command, and then maintain all operating power levels of the DLPC900 and the DLP9000 DMD for a minimum of 20 ms to allow the DLPC900 to complete the power down procedure. Following this procedure, the power can be allowed to fall below safe operating levels. Refer to the DLPC900 datasheet for more details on power down requirements.

In both anticipated power down and unanticipated power loss, the DLPC900 is commanded over the USB/I2C interface, and then the DLPC900 loads the correct power down sequence to the DMD. Communicating over the USB/I2C and loading the power down sequence accounts for most of the 20 ms. Compared to the DLPC910, the controlling processor only needs to assert the PWR_FLOAT pin and wait for a minimum of 500 µs.

The controlling applications processor can resume normal operations by commanding the DLPC900 to enter Normal mode. See *Power Mode* command in the DLPC900 Programmer's Guide DLPU018 for a description of this command.

11.3.2 DLP9000X

For correct power down operation of the DLP9000X DMD, the following power down procedure must be executed.

Prior to an anticipated power removal, assert PWR_FLOAT to the DLPC910 for a minimum of 500 µs to allow the DLPC910 to complete the power down procedure. This procedure will assure the DMD mirrors are in a flat state. Following this procedure, the power can be safely removed.

In the event of an unanticipated power loss, the power management system must detect the input power loss, assert PWR_FLOAT to the DLPC910, and maintain all operating power levels of the DLPC910 and the DLP9000X DMD for a minimum of 500 µs to allow the DLPC910 to complete the power down procedure. Refer to the DLPC910 datasheet for more details on power down requirements.

To restart after assertion of PWR_FLOAT without removing power, the DLPC910 must be reset by setting CTRL_RSTZ low (logic 0) for 50 ms, and then back to high (logic 1), or power to the DLPC910 must be cycled.

11.4 DMD Power Supply Power-Down Procedure

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. Refer to Table 5.
- During power-down, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions*. During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in *Figure 19*.
- During power-down, LVCMOS input pins must be less than specified in *Recommended Operating Conditions.*

DMD Power Supply Power-Down Procedure (continued)

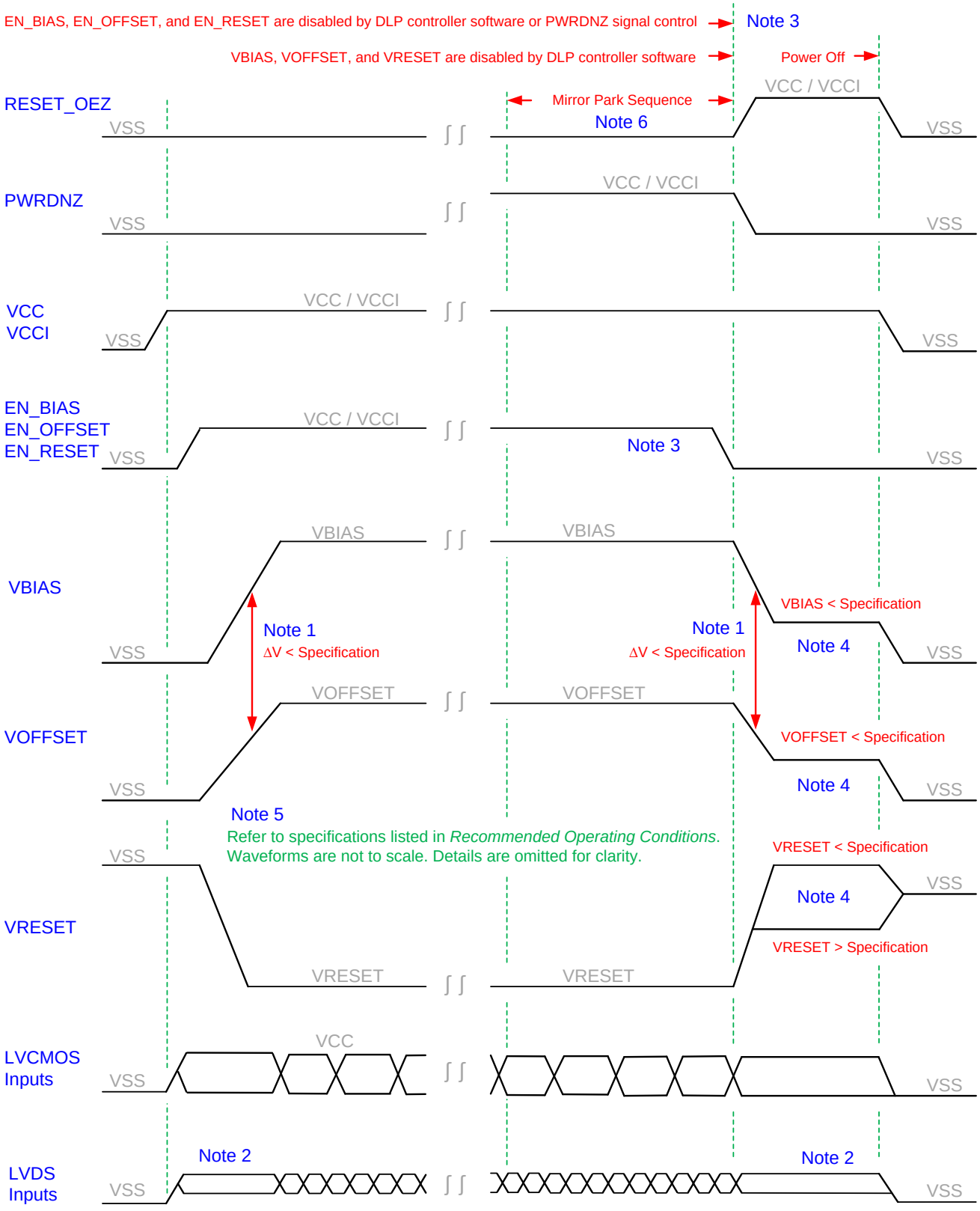


Figure 19. DMD Power Supply Sequencing Requirements

DMD Power Supply Power-Down Procedure (continued)

1. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in *Recommended Operating Conditions*. *OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down.*
2. During power-up, the LVDS signals are less than the input differential voltage (VID) maximum specified in *Recommended Operating Conditions*. During power-down, LVDS signals are less than the high level input voltage (VIH) maximum specified in *Recommended Operating Conditions*.
3. When system power is interrupted, the DLPC900 and the DLPC910 controllers initiate a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET after the micromirror park sequence. Software power-down disables VBIAS, VRESET, and VOFFSET after the micromirror park sequence through software control. For either case, enable signals EN_BIAS, EN_OFFSET, and EN_RESET are used to disable VBIAS, VOFFSET, and VRESET, respectively.
4. Refer to Table 5.
5. Figure not to scale. Details have been omitted for clarity. Refer to *Recommended Operating Conditions*.
6. Refer to *DMD Mirror Park Sequence Requirements* for details on powering down the DMD.

Table 5. DMD Power-Down Sequence Requirements

PARAMETER		MIN	MAX	UNIT
VBIAS	Supply voltage level during power–down sequence		4.0	V
VOFFSET			4.0	V
VRESET		–4.0	0.5	V

12 Layout

12.1 Layout Guidelines

Each chipset provides a solution for many applications including structured light and video projection. This section provides layout guidelines for the DMD.

12.1.1 General PCB Recommendations

The PCB shall be designed to IPC2221 and IPC2222, Class 2, Type Z, at level B producibility and built to IPC6011 and IPC6012, class 2. The PCB board thickness to be 0.062 inches ±10%, using a dielectric material with a low Loss-Tangent, for example: Hitachi 679gs or equivalent.

Two-ounce copper planes are recommended in the PCB design in order to achieve needed thermal connectivity. Refer to the digital controller data sheets listed under *Related Documentation* regarding DMD Interface Considerations.

High-speed interface waveform quality and timing on the digital controllers (that is, the LVDS DMD interface) is dependent on the following factors:

- Total length of the interconnect system
- Spacing between traces
- Characteristic impedance
- Etch losses
- How well matched the lengths are across the interface

Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

- Setup Margin = (controller output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)
- Hold-time Margin = (controller output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

The PCB SI degradation is the signal integrity degradation due to PCB affects which includes such things as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol-interference (ISI) noise.

Both the DLPC910 and the DLPC900 I/O timing parameters can be found in their respective data sheets. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not as easy to determine.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines provide a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Deviation from these recommendations should be confirmed with PCB signal integrity analysis or lab measurements.

12.1.2 Power Planes

Signal routing is NOT allowed on the power and ground planes. All device pin and via connections to this plane shall use a thermal relief with a minimum of four spokes. The power plane shall clear the edge of the PCB by 0.2".

Prior to routing, vias connecting all digital ground layers (GND) should be placed around the edge of the rigid PWB regions 0.025” from the board edges with a 0.100” spacing. It is also desirable to have all internal digital ground (GND) planes connected together in as many places as possible. If possible, all internal ground planes should be connected together with a minimum distance between connections of 0.5". Extra vias are not required if there are sufficient ground vias due to normal ground connections of devices. NOTE: All signal routing and signal vias should be inside the perimeter ring of ground vias.

Power and Ground pins of each component shall be connected to the power and ground planes with one via for each pin. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100”). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. Ground plane slots are NOT allowed.

Route VOFFSET, VBIAS, and VRESET as a wide trace >20 mils (wider if space allows) with 20 mils spacing.

Layout Guidelines (continued)

12.1.3 LVDS Signals

The LVDS signals shall be first. Each pair of differential signals must be routed together at a constant separation such that constant differential impedance (as in section *Board Stack and Impedance Requirements*) is maintained throughout the length. Avoid sharp turns and layer switching while keeping lengths to a minimum. The distance from one pair of differential signals to another shall be at least 2 times the distance within the pair.

12.1.4 Critical Signals

The critical signals on the board must be hand routed in the order specified below. In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long trace all around the PCB.

Table 6. Timing Critical Signals

GROUP	SIGNAL	CONSTRAINTS	ROUTING LAYERS
1	D_AP(0:15), D_AN(0:15), DCLK_AP, DCLK_AN, SCTRL_AN, SCTRL_AP, D_BP(0:15), D_BN(0:15), DCLK_BP, DCLK_BN, SCTRL_BN, SCTRL_BP, D_CP(0:15), D_CN(0:15), DCLK_CP, DCLK_CN, SCTRL_CN, SCTRL_CP, D_DP(0:15), D_DN(0:15), DCLK_DP, DCLK_DN, SCTRL_DN, SCTRL_DP.	Refer to Table 7 and Table 8	Internal signal layers. Avoid layer switching when routing these signals.
2	RESET_ADDR_(0:3), RESET_MODE_(0:1), RESET_OEZ, RESET_SEL_(0:1) RESET_STROBE, RESET_IRQZ.		Internal signal layers. Top and bottom as required.
3	SCP_CLK, SCP_DO, SCP_DI, SCP_DMD_CSZ.		Any
4	Others	No matching/length requirement	Any

12.1.5 Flex Connector Plating

Plate all the pad area on top layer of flex connection with a minimum of 35 and maximum 50 micro-inches of electrolytic hard gold over a minimum of 150 micro-inches of electrolytic nickel.

12.1.6 Device Placement

Unless otherwise specified, all major components should be placed on top layer. Small components such as ceramic, non-polarized capacitors, resistors and resistor networks can be placed on bottom layer. All high frequency de-coupling capacitors for the ICs shall be placed near the parts. Distribute the capacitors evenly around the IC and locate them as close to the device's power pins as possible (preferably with no vias). In the case where an IC has multiple de-coupling capacitors with different values, alternate the values of those that are side by side as much as possible and place the smaller value capacitor closer to the device.

12.1.7 Device Orientation

It is desirable to have all polarized capacitors oriented with their positive terminals in the same direction. If polarized capacitors are oriented both horizontally and vertically, then all horizontal capacitors should be oriented with the "+" terminal the same direction and likewise for the vertically oriented ones.

12.1.8 Fiducials

Fiducials for automatic component insertion should be placed on the board according to the following guidelines or on recommendation from manufacturer:

- Fiducials for optical auto insertion alignment shall be placed on three corners of both sides of the PWB.
- Fiducials shall also be placed in the center of the land patterns for fine pitch components (lead spacing <0.05").
- Fiducials should be 0.050 inch copper with 0.100 inch cutout (antipad).

12.2 Layout Example

12.2.1 Board Stack and Impedance Requirements

Refer to Figure 20 regarding guidance on the parameters.

PCB design:

Configuration:	Asymmetric dual stripline
Etch thickness (T):	1.0-oz copper (1.2 mil)
Flex etch thickness (T):	0.5-oz copper (0.6 mil)
Single-ended signal impedance:	50 Ω (±10%)
Differential signal impedance:	100 Ω (±10%)

PCB stack-up:

Reference plane 1 is assumed to be a ground plane for proper return path.

Reference plane 2 is assumed to be the I/O power plane or ground.

Dielectric material with a low Loss-Tangent, for example: Hitachi 679gs or equivalent.	(Er): 3.8 (nominal)
Signal trace distance to reference plane 1 (H1):	5.0 mil (nominal)
Signal trace distance to reference plane 2 (H2):	34.2 mil (nominal)

Layout Example (continued)

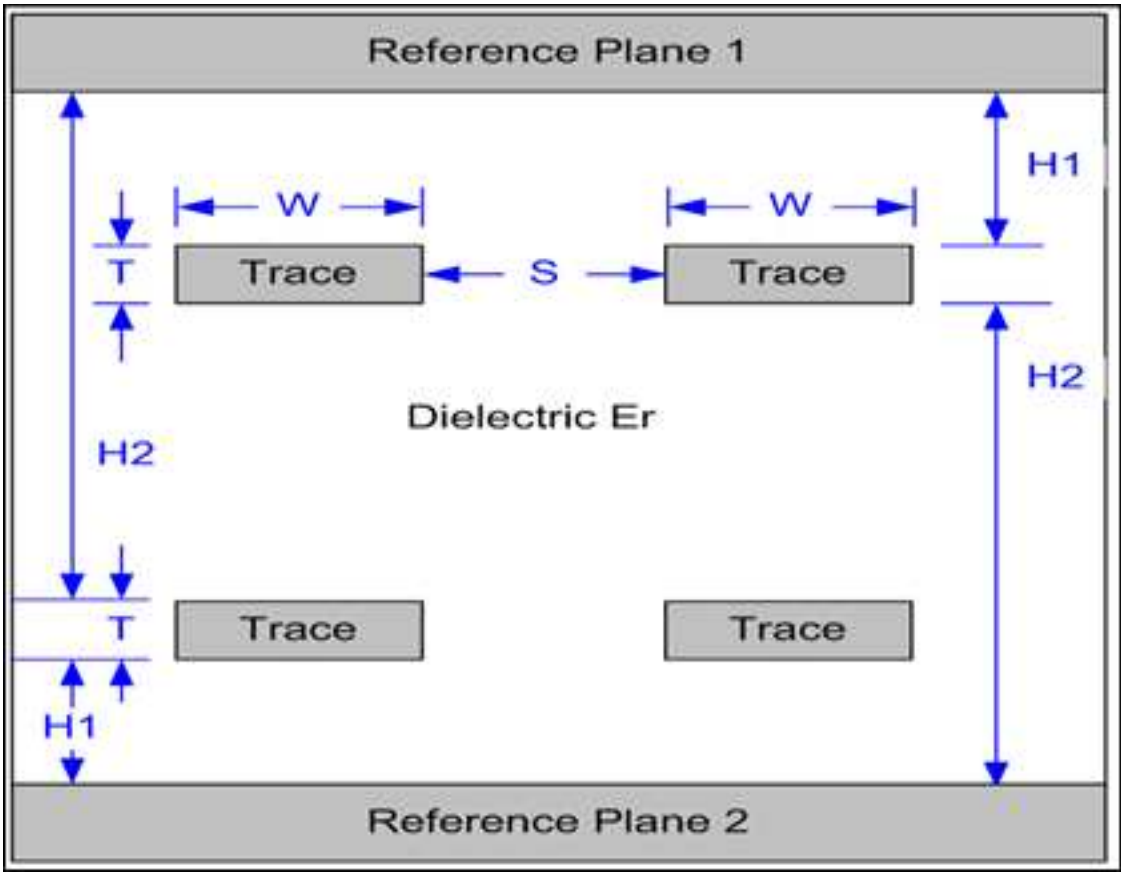


Figure 20. PCB Stack Geometries

Layout Example (continued)

Table 7. General PCB Routing (Applies to All Corresponding PCB Signals)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Line width (W)	Escape routing in ball field	4 .4 (0.1)	4 .3 (0.1)	mil (mm)
	PCB etch data or control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB etch clocks	7 (0.18)	4.25 (0.11)	mil (mm)
Differential signal pair spacing (S)	PCB etch data or control	N/A	5.75 (1) –0.15	mil (mm)
	PCB etch clocks	N/A	5.75 (1) –0.15	mil (mm)
Minimum differential pair-to-pair spacing (S)	PCB etch data or control	N/A	20 (0.51)	mil (mm)
	PCB etch clocks	N/A	20 (0.51)	mil (mm)
	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
Minimum line spacing to other signals (S)	PCB etch data or control	10 (0.25)	20 (0.51)	mil (mm)
	PCB etch clocks	20 (0.51)	20 (0.51)	mil (mm)
Maximum differential pair P-to-N length mismatch	Total data	N/A	10 –0.25	mil (mm)
	Total data	N/A	10 –0.25	mil (mm)

(1) Spacing may vary to maintain differential impedance requirements

Table 8. DMD Interface Specific Routing

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH**	**UNIT**
DMD (LVDS)	SCTRL_AN / SCTRL_AP D_AP(15:0)/ D_AN(15:0)	DCKA_P/ DCKA_N	± 50 (± 1.3)	mil (mm)
DMD (LVDS)	SCTRL_BN/ SCTRL_BP D_BP(15:0)/ D_BN(15:0)	DCKB_P/ DCKB_N	± 50 (± 1.3)	mil (mm)
DMD (LVDS)	SCTRL_CN/ SCTRL_CP D_CP(15:0)/ D_CN(15:0)	DCK_CP/ DCK_CN	± 50 (± 1.3)	mil (mm)
DMD (LVDS)	SCTRL_DN/ SCTRL_DP D_DP(15:0)/ D_DN(15:0)	DCK_CP/ DCK_CN	± 50 (± 1.3)	mil (mm)

Number of layer changes:

- Single-ended signals: Minimize
- Differential signals: Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

Table 9. DMD Signal Routing Length (1)

BUS	MIN	MAX	UNIT
DMD (LVDS)	50	375	mm

(1) Max signal routing length includes escape routing.

Stubs: Stubs should be avoided.

Termination Requirements: DMD interface: None – The DMD receiver is differentially terminated to 100 Ω internally.

Connector (DMD-LVDS interface bus only):

High-speed connectors that meet the following requirements should be used:

- Differential crosstalk: <5%
- Differential impedance: 75 to 125 Ω

Routing requirements for right-angle connectors: When using right-angle connectors, P-N pairs should be routed in the same row to minimize delay mismatch. When using right-angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths. Voltage or low frequency signals should be routed on the outer layers. Signal trace corners shall be no sharper than 45 degrees. Adjacent signal layers shall have the predominant traces routed orthogonal to each other.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Device Handling

All external signals on the DMD are protected from damage by electrostatic discharge, and are tested in accordance with JESD22-A114-B electrostatic discharge (ESD) sensitivity testing human body model (HBM).

Table 10. DMD ESD Protection Limits

PACKAGE TERMINAL TYPE	VOLTAGE (MAXIMUM)	UNIT
Input	2000	V
Output	2000	V
VCC	2000	V
VCCI	2000	V
VOFFSET	2000	V
VBIAS	2000	V
VRESET	2000	V
All MBRST	2000	V

All CMOS devices require proper Electrostatic Discharge (ESD) handling procedures. Refer to drawing 2504641 DMD Handling Specification, for precautions to protect the DMD from ESD and to protect the DMD's glass and electrical contacts. Refer to drawing 2504640 DMD Glass Cleaning Procedure, for correct and consistent methods for cleaning the glass of the DMD, in such a way that the anti-reflective coatings on the glass surface are not damaged.

13.1.2 Device Nomenclature

Figure 21 provides a legend for reading the complete device name for any DLP device.

Table 11. Package-Specific Information

PACKAGE TYPE	ALTERNATE NAME
FLS	LCCC

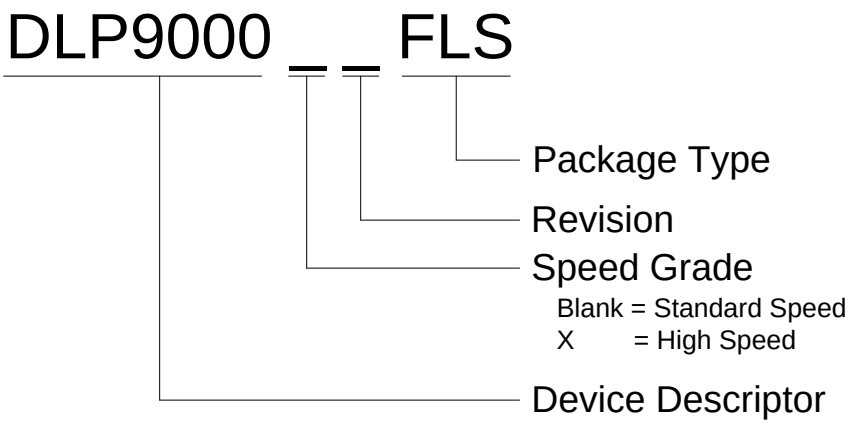


Figure 21. Device Nomenclature

13.1.3 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 22. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

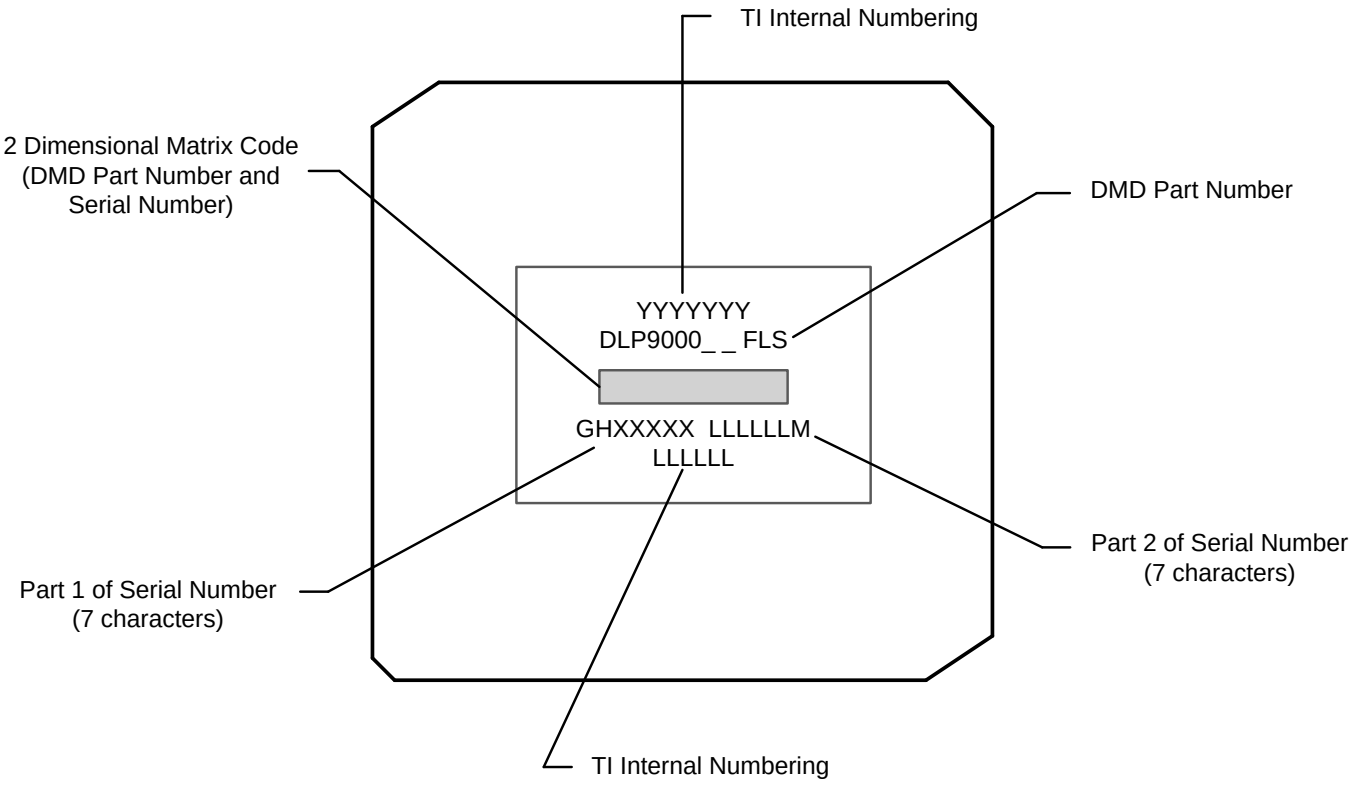


Figure 22. DMD Markings

13.2 Documentation Support

13.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP9000 family of devices:

- DLPC900 Digital Controller Data Sheet (DLPS037)
- DLPC900 Software Programmer's Guide (DLPU018)
- DLPC910 Digital Controller Data Sheet (DLPS064)
- DLPR910 Configuration PROM Data Sheet (DLPS065)

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array and the temperature gradient between any two points on or within the package.

Refer to *Absolute Maximum Ratings* and *Recommended Operating Conditions* regarding applicable temperature limits.

14.2 Package Thermal Resistance

The DMD is designed to conduct the absorbed and dissipated heat back to the series FLS package where it can be removed by an appropriate thermal management system. The thermal management system must be capable of maintaining the package within the specified operational temperatures at the thermal test point locations (refer to Figure 15 or *Micromirror Array Temperature Calculation*). The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions can include light energy absorbed by the window aperture, electrical power dissipation of the array, and parasitic heating. For the thermal resistance, refer to *Thermal Information*.

14.3 Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a thermal test point location is defined as shown in Figure 15 and *Micromirror Array Temperature Calculation*.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP9000BFLS	ACTIVE	CLGA	FLS	355	1	RoHS & Green	NI-PD-AU	N / A for Pkg Type			Samples
DLP9000XBFLS	ACTIVE	CLGA	FLS	355	1	RoHS & Green	NI-PD-AU	N / A for Pkg Type			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

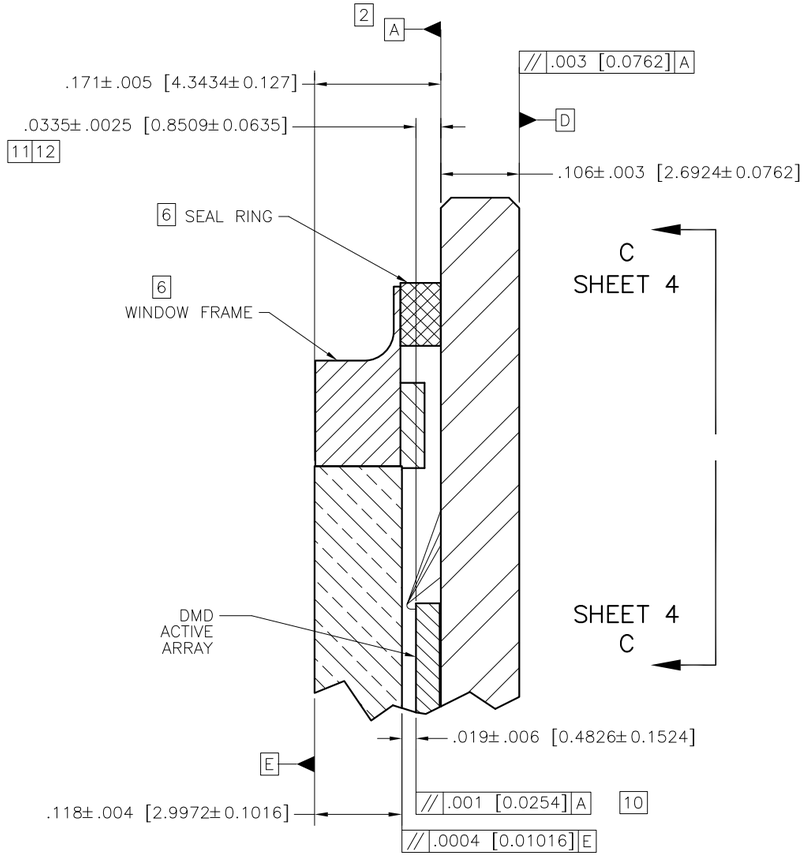
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

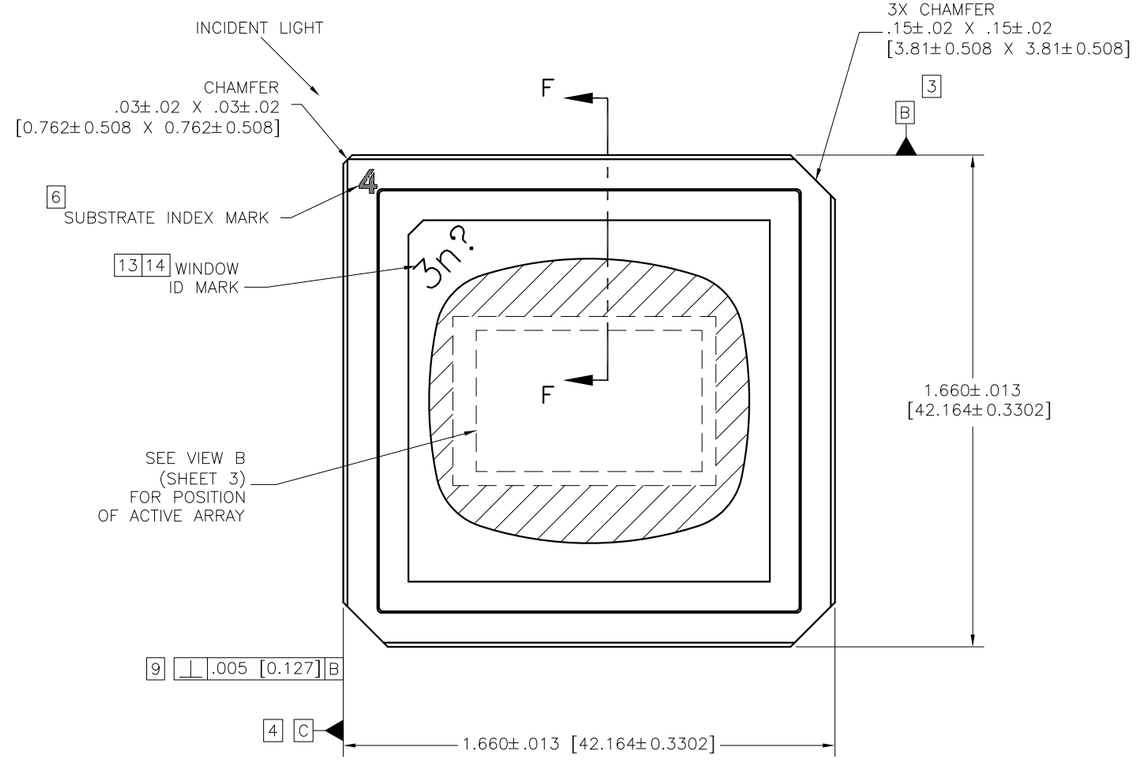
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2098262, INITIAL RELEASE	4/16/09	M. AVERY
B	ECO 2099196, CHANGE DESIGN TO OVAL WINDOW	5/22/09	M. AVERY
C	ECO 2150560, ADD NOTE 15.	05/12/15	M. AVERY
D	ECO 2179202, CHG WINDOW MARK TO INCLUDE UV	1/22/19	B. HASKETT
E	ECO 2179654, DELETE NOTE 7	2/15/19	B. HASKETT

NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M–1994.
2. DATUM A (SYSTEM INTERFACE PLANE) ESTABLISHED BY THREE DATUM AREAS SHOWN IN VIEW A (SHEET 2).
3. DATUM B ESTABLISHED BY TWO DATUM AREAS SHOWN IN VIEW A (SHEET 2).
4. DATUM C ESTABLISHED BY DATUM AREA SHOWN IN VIEW A (SHEET 2).
5. LOCALIZED BACKSIDE SURFACE FLATNESS APPLIES TO ENTIRE SURFACE.
6. SUBSTRATE INDEX MARK, BACK INDEX PAD, SYMBOLIZATION PAD, SEAL RING, AND WINDOW FRAME TO BE ELECTRICALLY CONNECTED TO VSS PLANE IN SUBSTRATE.
7. (DELETED)
8. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND IS THE MAXIMUM VALUE ALLOWED.
9. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE.
10. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
11. DIE HEIGHT TOLERANCE APPLIES TO CENTER OF DMD ACTIVE ARRAY ONLY.
12. DMD ACTIVE ARRAY ROTATION AND LOCATION DIMENSIONS ARE RELATED TO DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY).
13. WINDOW SHALL BE ORIENTED SUCH THAT I.D. MARK ALIGNS WITH SUBSTRATE INDEX MARK AS SHOWN.
14. n AND ? ARE WILD CARD CHARACTERS. n=4 FOR STANDARD VISIBLE WINDOWS; n=7 FOR UV-TRANSMISSIVE WINDOWS. ? CAN BE ANY LETTER.
15. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE SYMBOLIZATION PAD, AS SHOWN. SUBSTRATES WITH Ni/Pd/Au SHALL HAVE THE SAME MARKING, BUT ROTATED UPSIDE-DOWN.



SECTION F–F
SCALE 10/1



PARTS LIST

–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES[MILLIMETERS]
- TOLERANCES: ANGLES ± 1°
  3 PLACE DECIMALS ±.005[0.127]
  2 PLACE DECIMALS ±.01[0.254]
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

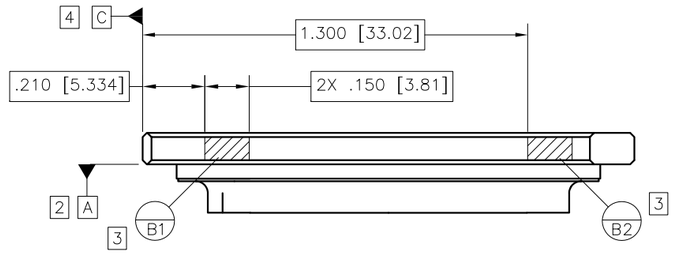
.013 THRU .125 ± .004 / ± .001	.126 THRU .250 ± .005 / ± .001	.251 THRU .500 ± .006 / ± .001
.501 THRU .750 ± .008 / ± .001	.751 THRU 1.000 ± .010 / ± .001	1.001 THRU 2.000 ± .012 / ± .001

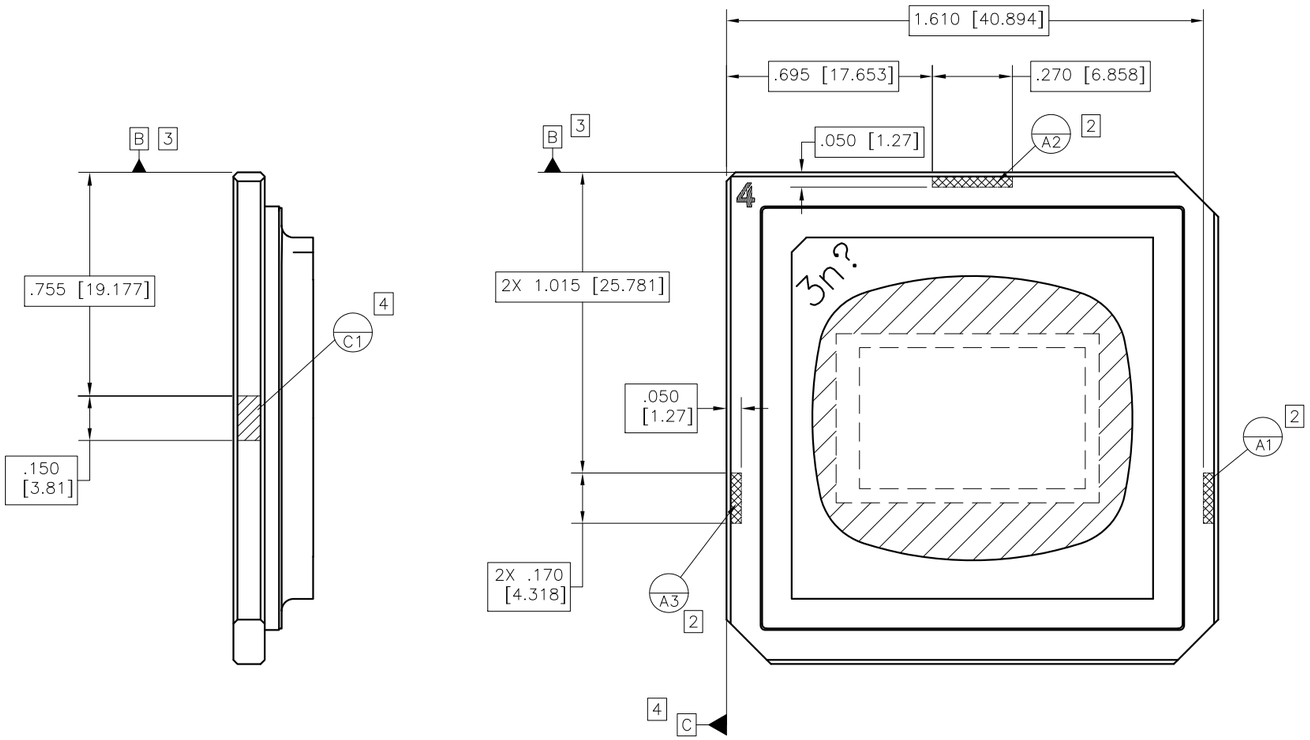
THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
NONE	0314DA
APPLICATION	

DWN M. AVERY	DATE 4/02/09	TEXAS INSTRUMENTS Dallas, Texas
ENGR M. AVERY	4/02/09	ICD, MECHANICAL, DMD .9" WQXGA 2XLVDS TYPE A (FLS PACKAGE)
QA		
APVD		SIZE D · DRAWING NO 2510425 · REV E · SCALE 4/1 · SHEET 1 OF 4

ACED1g

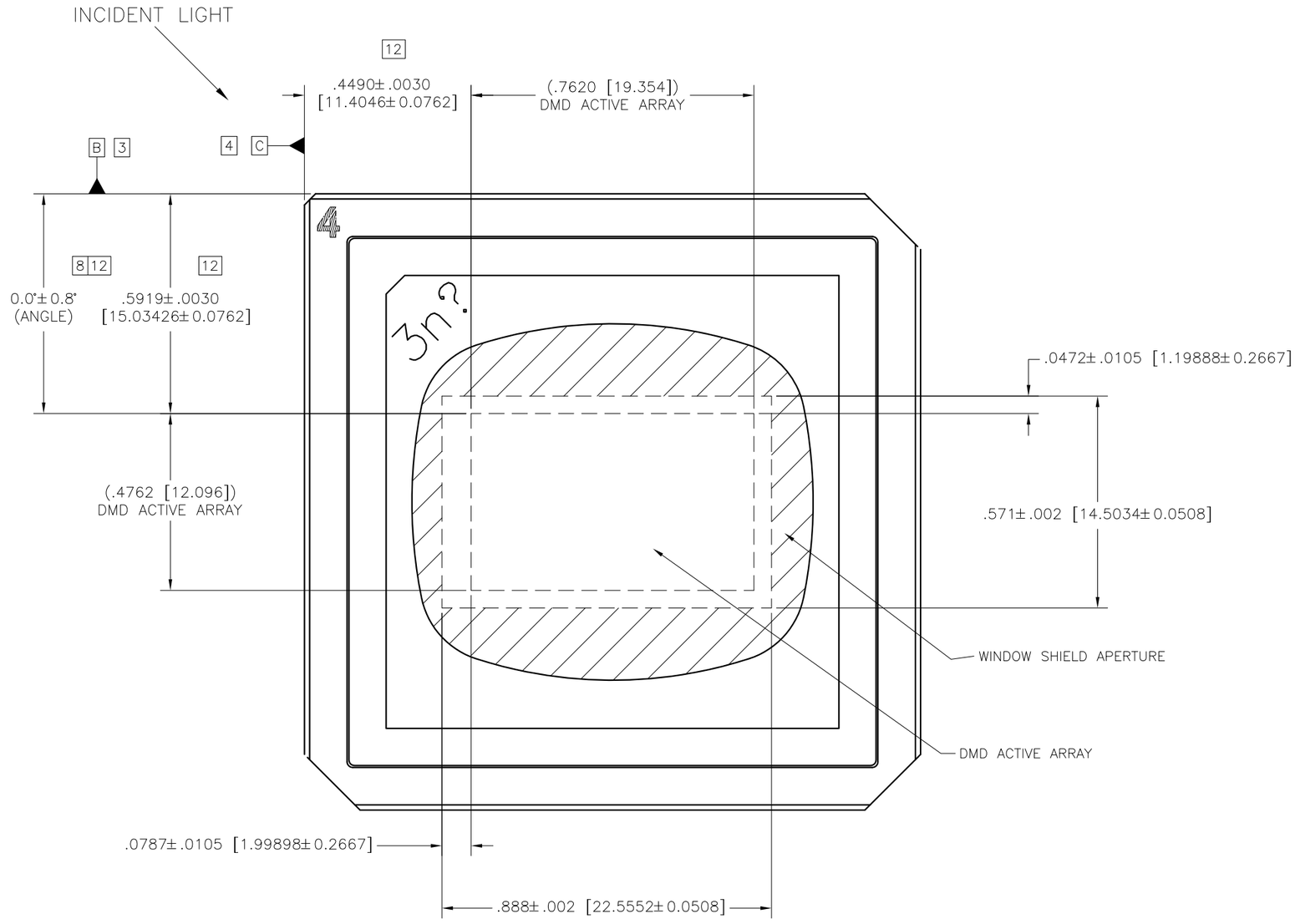




VIEW A (SHEET 1 NOTES)
DATUM A, B AND C DETAILS

Texas Instruments, Dallas, Texas	DWN DATE	SIZE D	DRAWING NO 2510425	REV E
	ISSUE DATE	SCALE 4/1	SHEET 2	

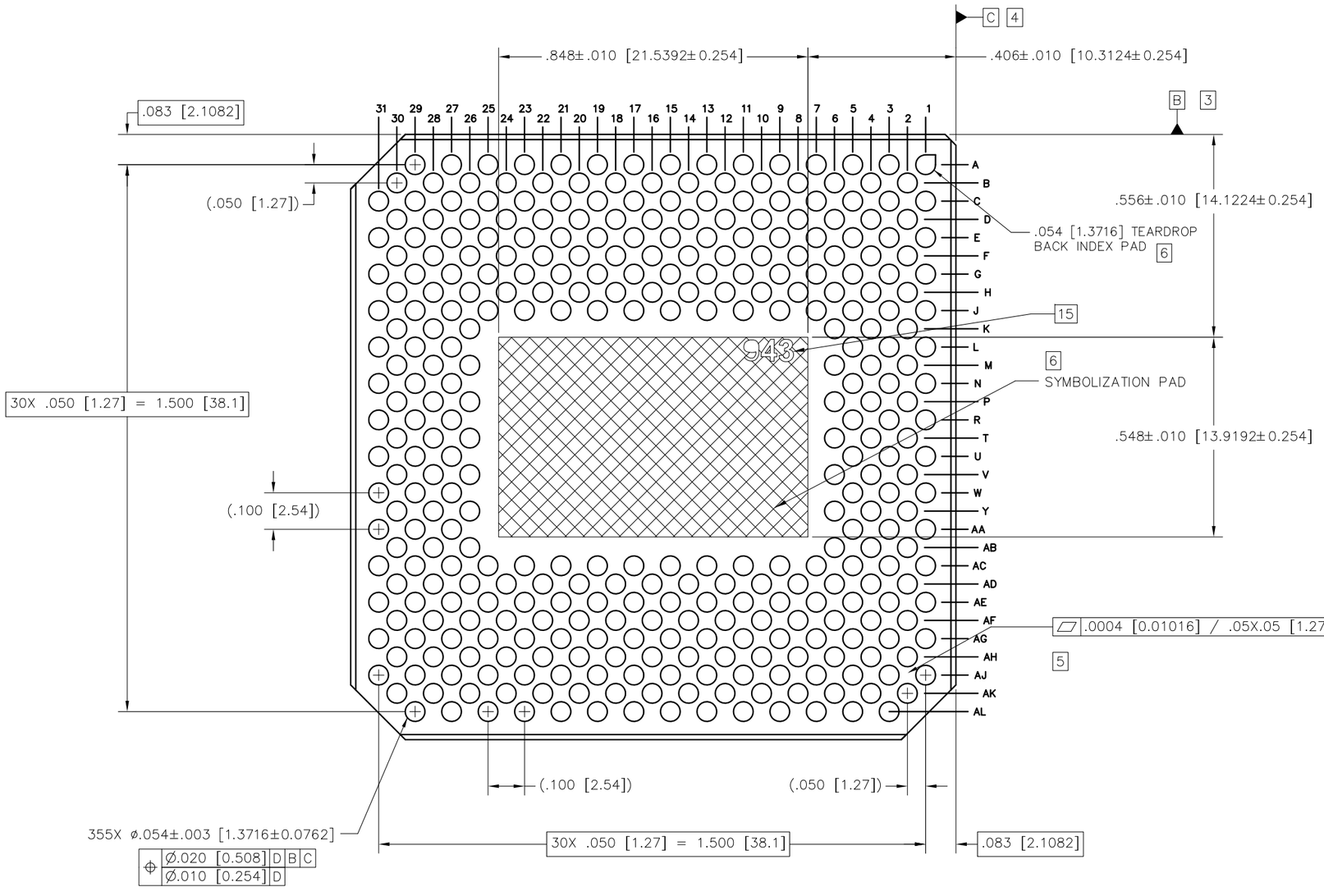
ACED2c



VIEW B (SHEET 1)
POSITION OF ACTIVE ARRAY
SCALE 6/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2510425	REV E
		SCALE 4/1	SHEET 3	

ACED2c



VIEW C–C (SHEET 1)
BACK PADS
SCALE 6/1

Texas Instruments, Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2510425	REV E
		SCALE 4/1	SHEET 4	

ACED2c

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