HIGH-SPEED PWM CONTROLLER

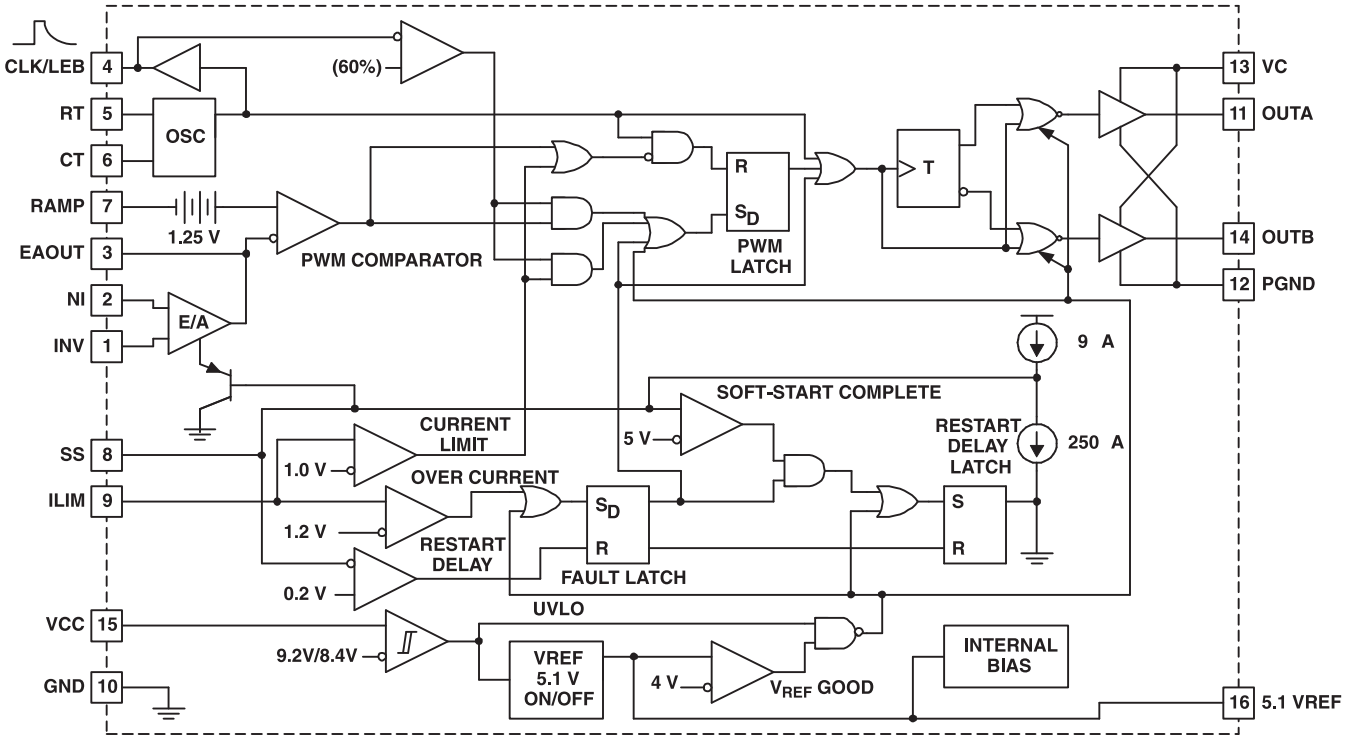
FEATURES

- **Qualified for Automotive Applications**
- **Improved Version of the UC3825 PWM**
- **Compatible With Voltage-Mode or Current-Mode Control Methods**
- **Practical Operation at Switching Frequencies to 1 MHz**
- **50-ns Propagation Delay to Output**
- **High-Current Dual Totem-Pole Outputs: 2 A (Peak)**
- **Trimmed Oscillator Discharge Current**
- **Low 100-µA Startup Current**
- **Pulse-by-Pulse Current-Limiting Comparator**
- **Latched Overcurrent Comparator With Full-Cycle Restart**

DESCRIPTION

The UC2825A pulse-width modulation (PWM) controller is an improved versions of the standard UC3825. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset voltage is 2 mV. Current limit threshold is specified to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead-time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100 µA, is ideal for off-line applications. The output drivers are redesigned to actively sink current during undervoltage lockout (UVLO) at no expense to the startup current specification. In addition, each output is capable of 2-A peak currents during transitions.

BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Functional improvements have also been implemented. The shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2 V. The overcurrent comparator sets a latch that ensures full discharge of the soft-start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft-start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The CLOCK pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC2825A has dual alternating outputs and the same pin configuration of the UC3825. "A" version parts have UVLO thresholds identical to the original UC3825.

See the application report, *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers* (SLUA125) for detailed technical and application information.

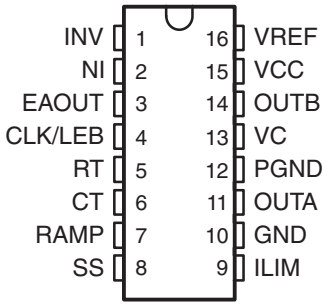
ORDERING INFORMATION(1)

T_J	MAXIMUM DUTY CYCLE	UVLO	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	<50%	9.2 V/8.4 V	SOIC – DW	Reel of 2000	UC2825AQDWRQ1	UC2825AQDW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN ASSIGNMENTS

DW PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CLK/LEB	4	O	Output of the internal oscillator
CT	6	I	Timing capacitor connection for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
EAOUT	3	O	Output of the error amplifier for compensation
GND	10		Analog ground return
ILIM	9	I	Input to the current limit comparator
INV	1	I	Inverting input to the error amplifier
NI	2	I	Noninverting input to the error amplifier
OUTA	11	O	High-current totem-pole output A of the on-chip drive stage
OUTB	14	O	High-current totem-pole output B of the on-chip drive stage
PGND	12		Ground return for the output driver stage
RAMP	7	I	Noninverting input to the PWM comparator with 1.25-V internal input offset. In voltage-mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current-mode operation, this serves as the slope compensation input.
RT	5	I	Timing resistor connection for oscillator frequency programming
SS	8	I	Soft-start input and the maximum duty cycle clamp
VC	13		Power supply for the output stage. This pin should be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor with minimal trace lengths.
VCC	15		Power supply for the device. This pin should be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor with minimal trace lengths
VREF	16	O	5.1-V reference. For stability, the reference should be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

			VALUE
V_{IN}	Supply voltage	VC, VCC	22 V
I_O	Source or sink current, dc	OUTA, OUTB	0.5 A
I_O	Source or sink current, pulse (0.5 µs)	OUTA, OUTB	2.2 A
	Analog inputs	INV, NI, RAMP	–0.3 V to 7 V
		ILIM, SS	–0.3 V to 6 V
	Power ground	PGND	±0.2 V
I_{CLK}	Clock output current	CLK/LEB	–5 mA
$I_{O(EA)}$	Error amplifier output current	EAOUT	5 mA
I_{SS}	Soft-start sink current	SS	20 mA
I_{OSC}	Oscillator charging current	RT	–5 mA
T_J	Operating virtual junction temperature range		–55°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference, V_{REF}							
V_O	Ouput voltage	T_J = 25°C, I_O = 1 mA		5.05	5.1	5.15	V
	Line regulation	12 V ≤ V_{CC} ≤ 20 V			2	15	mV
	Load regulation	1 mA ≤ I_O ≤ 10 mA			5	20	mV
	Total output variation	Line, load, temperature		5.03		5.17	V
	Temperature stability(1)	$T_{(min)}$ < T_J < $T_{(max)}$			0.2	0.4	mV/°C
	Output noise voltage(1)	10 Hz < f < 10 kHz			50		μV_{RMS}
	Long term stability(1)	T_J = 125°C, 1000 hours			5	25	mV
	Short circuit current	VREF = 0 V		30	60	90	mA
			T_J = 125°C	30		110	
Oscillator							
f_{OSC}	Initial accuracy(1)	T_J = 25°C		375	400	425	kHz
		R_T = 6.6 kΩ, C_T = 220 pF, T_J = 25°C		0.9	1	1.1	MHz
	Total variation(1)	Line, temperature		350		450	kHz
		R_T = 6.6 kΩ, C_T = 220 pF		0.85		1.15	MHz
	Voltage stability	12 V < V_{CC} < 20 V				1	%
	Temperature stability(1)	$T_{(min)}$ < T_J < $T_{(max)}$			±5		%
	High-level output voltage, clock			3.7	4		V
	Low-level output voltage, clock				0	0.2	V
	Ramp peak			2.6	2.8	3	V
	Ramp valley			0.7	1	1.25	V
	Ramp valley to peak			1.6	1.8	2	V
		T_J = –40°C		1.55		2	
I_{OSC}	Oscillator discharge current	R_T = Open, V_{CT} = 2 V		9	10	11	mA
			T_J = 125°C	8		11	
Error Amplifier							
	Input offset voltage				2	10	mV
	Input bias current				0.6	3	µA
	Input offset current				0.1	1	µA
	Open loop gain	1 V < V_O < 4 V		60	95		dB
CMRR	Common-mode rejection ratio	1.5 V < V_{CM} < 5.5 V		75	95		dB
PSRR	Power-supply rejection ratio	12 V < V_{CC} < 20 V		85	110		dB
$I_{O(sink)}$	Output sink current	V_{EAOUT} = 1 V		1	2.5		mA
$I_{O(src)}$	Output source current	V_{EAOUT} = 4 V		–0.5	–1.3		mA
	High-level output voltage	I_{EAOUT} = –0.5 mA		4.5	4.7	5	V
	Low-level output voltage	I_{EAOUT} = –1 mA		0	0.5	1	V
	Gain bandwidth product	f = 200 kHz		6	12		MHz
	Slew rate(1)			6	9		V/µs

(1) Specified by design

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM Comparator						
I_{BIAS}	Bias current, RAMP	V_{RAMP} = 0 V		–1	–8	µA
	Minimum duty cycle				0	%
	Maximum duty cycle		85			%
t_{LEB}	Leading edge blanking time	R_{LEB} = 2 kΩ, C_{LEB} = 470 pF	300	375	450	ns
R_{LEB}	Leading edge blanking resistance	$V_{CLK/LEB}$ = 3 V	8	10	12	kΩ
V_{ZDC}	Zero dc threshold voltage, EAOUT	V_{RAMP} = 0 V	1.10	1.25	1.4	V
t_{DELAY}	Delay-to-output time(2)	V_{EAOUT} = 2.1 V, V_{ILIM} = 0 V to 2 V step		50	80	ns
Current Limit / Start Sequence / Fault						
I_{SS}	Soft-start charge current	V_{SS}= 2.5 V	8	14	20	µA
V_{SS}	Full soft-start threshold voltage		4.3	5		V
I_{DSCH}	Restart discharge current	V_{SS}= 2.5 V	100	250	350	µA
I_{SS}	Restart threshold voltage			0.3	0.5	V
I_{BIAS}	ILIM bias current	V_{ILIM} = 0 V to 2 V step			15	A
I_{CL}	Current limit threshold voltage		0.95	1	1.05	V
	Overcurrent threshold voltage		1.14	1.2	1.26	
t_d	Delay-to-output time, ILIM(1)	V_{ILIM} = 0 V to 2 V step		50	80	ns
Output						
	Low-level output saturation voltage	I_{OUT} = 20 mA		0.25	0.4	V
		I_{OUT} = 200 mA		1.2	2.2	
	High-level output saturation voltage	I_{OUT} = –20 mA		1.9	2.9	V
		I_{OUT} = –200 mA		2	3	
t_r, t_f	Rise/fall time(2)	C_L = 1 nF		20	45	ns
Undervoltage Lockout (UVLO)						
	Start threshold voltage		8.4	9.2	9.6	V
	UVLO hysteresis		0.4	0.8	1.2	V
Supply Current						
I_{su}	Startup current	VC = V_{CC} = V_{TH} = –0.5 V		100	300	µA
I_{CC}	Input current			28	36	mA

(2) Specified by design

APPLICATION INFORMATION

The oscillator is a sawtooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin (C_{CT}). The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency (RT) and D_{MAX}. The design equations are:

$$R_T = \frac{3\ V}{(10\ mA) \times \left(1 - D_{MAX}\right)} \qquad C_T = \frac{\left(1.6 \times D_{MAX}\right)}{\left(R_T \times f\right)} \tag{1}$$

Recommended values for R_T range from 1 kΩ to 100 kΩ. Control of D_{MAX} less than 70% is not recommended.

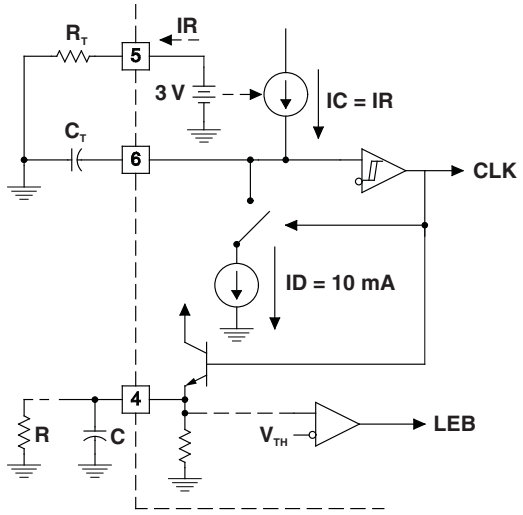


Figure 1. Oscillator

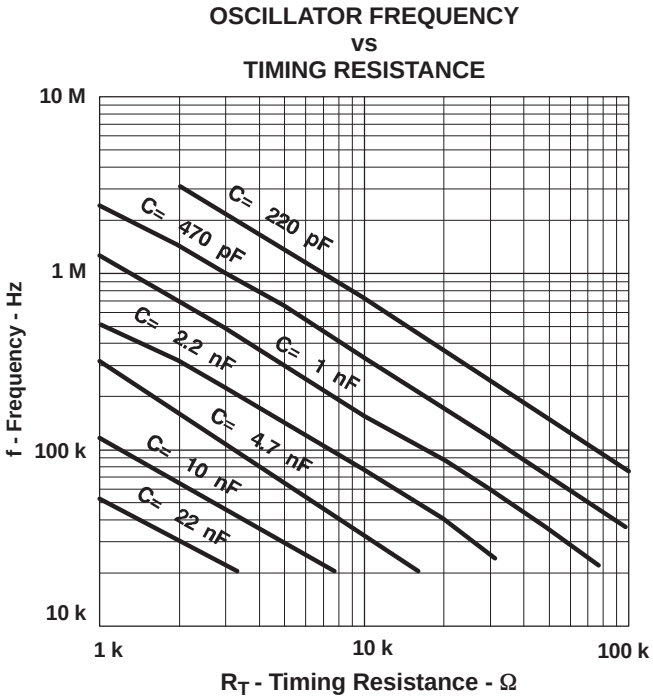


Figure 2.

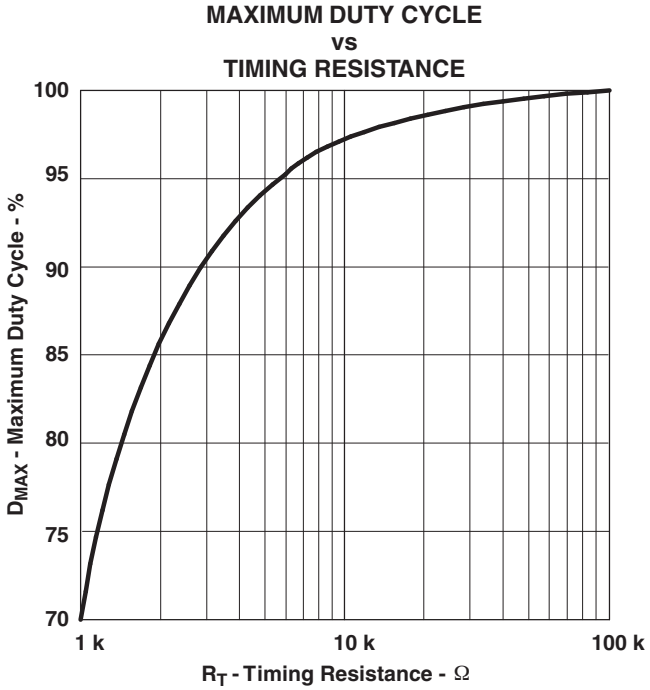


Figure 3.

Leading Edge Blanking (LEB)

The UC2825A performs fixed-frequency PWM control. The outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0% to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. LEB causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of LEB.

To program a LEB period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-kΩ resistor determines the blanked interval. The 10-kΩ resistor has a 10% tolerance. For more accuracy, an external 2-kΩ 1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 kΩ with a tolerance of 2.4%. The design equation is:

$$t_{LEB} = 0.5 \times \left(R \parallel 10\ k\Omega\right) \times C \quad (2)$$

Values of R less than 2 kΩ should not be used.

LEB is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.

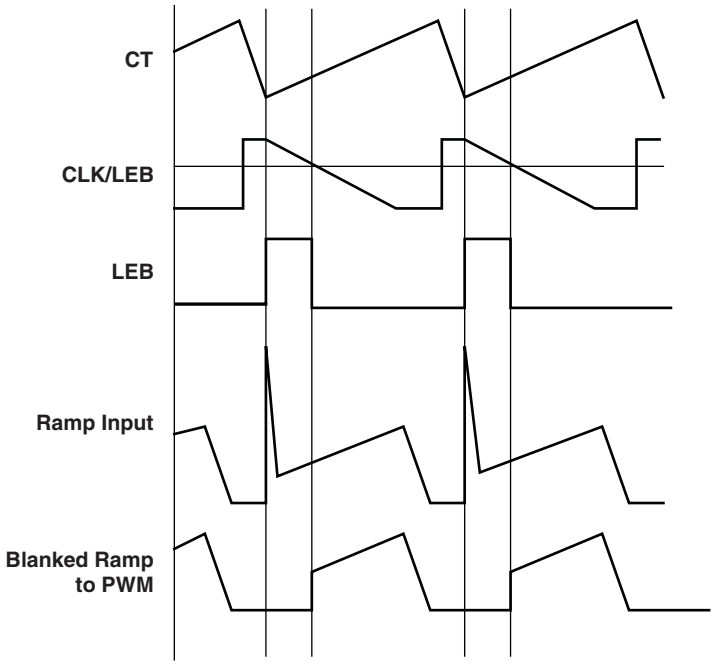


Figure 4. Leading Edge Blanking Operational Waveforms

UVLO, Soft Start, and Fault Management

Soft start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amplifier output is also forced low. While the internal 9-µA source charges the SS pin, the error amplifier output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2 V, the fault latch is set and the output pins are driven low. The soft-start capacitor is then discharged by a 250-µA current sink. No more output pulses are allowed until the soft-start capacitor is fully discharged and ILIM is below 1.2 V. At this time, the fault latch resets and the chip executes a soft start.

Should the fault latch get set during soft start, the outputs are immediately terminated, but the soft-start capacitor does not discharge until it has been fully charged first. This results in a controlled hiccup interval for continuous fault conditions.

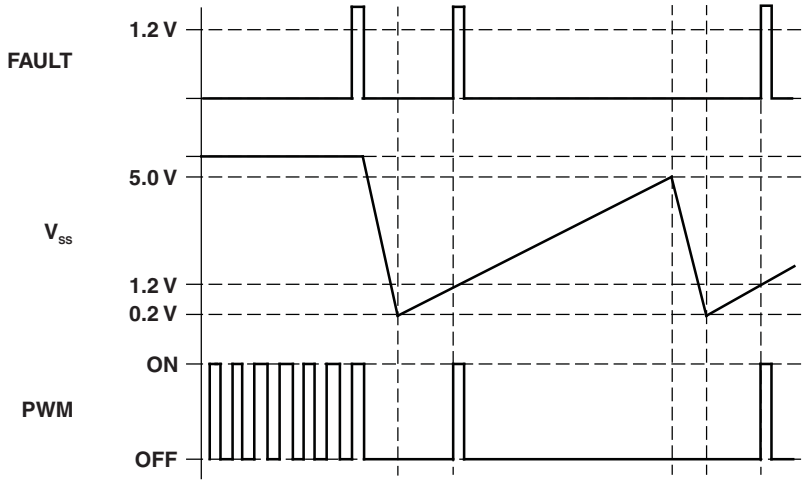


Figure 5. Soft-Start and Fault Waveforms

Active-Low Outputs During UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

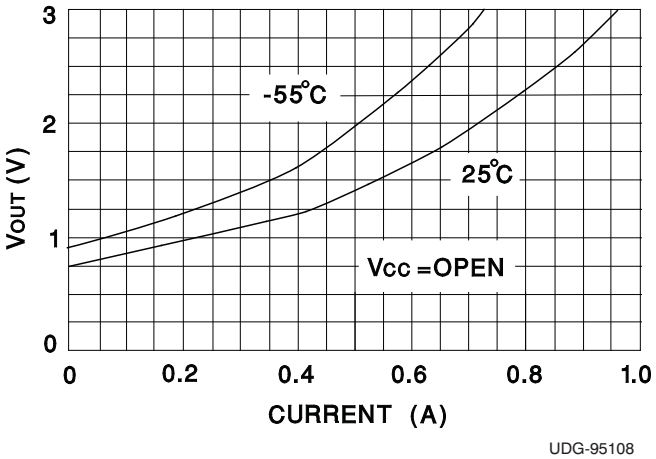


Figure 6. Output Voltage vs Output Current

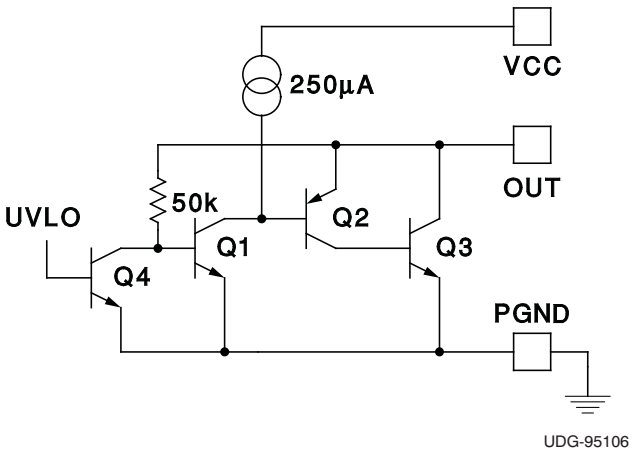


Figure 7. Output Voltage and Current During UVLO

Control Methods

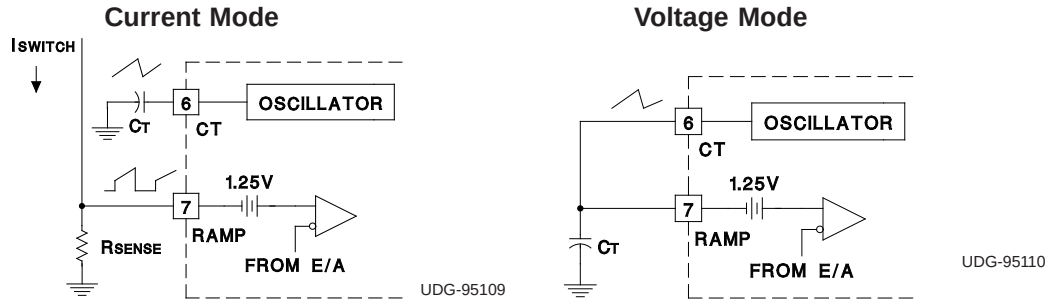


Figure 8. Control Methods

Synchronization

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free-running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10 ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that the CLK/LEB pin no longer accepts an incoming synchronizing signal.

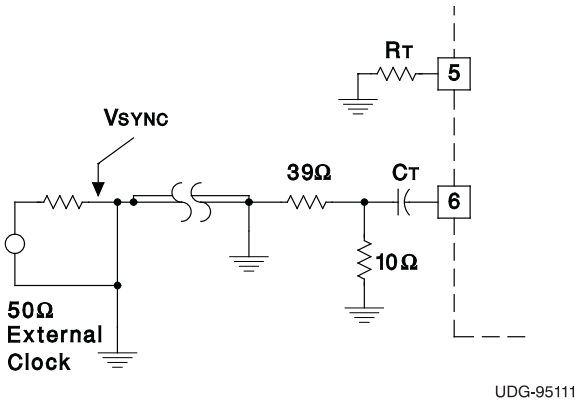


Figure 9. General Oscillator Synchronization

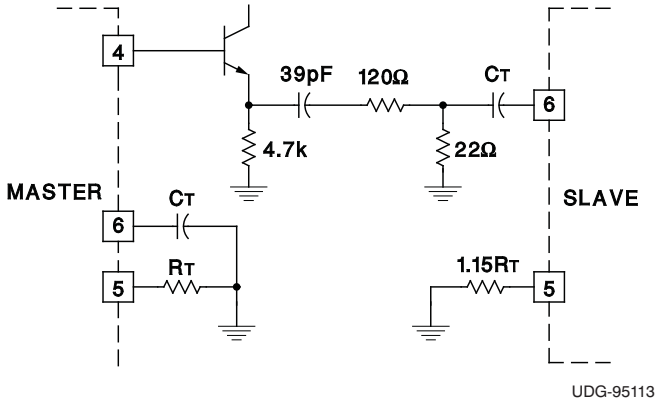


Figure 10. Two Unit Interface

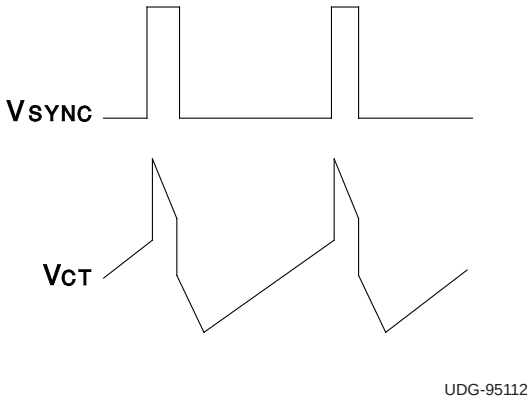


Figure 11. Operational Waveforms

High-Current Outputs

Each totem pole output can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the device's analog circuitry from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) (see Figure 13) from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. Do not use standard silicon diodes.

Although they are single-ended devices, two output drivers are available on the UC2825A. These can be paralleled by the use of a 0.5-Ω (noninductive) resistor connected in series with each output for a combined peak current of 4 A.

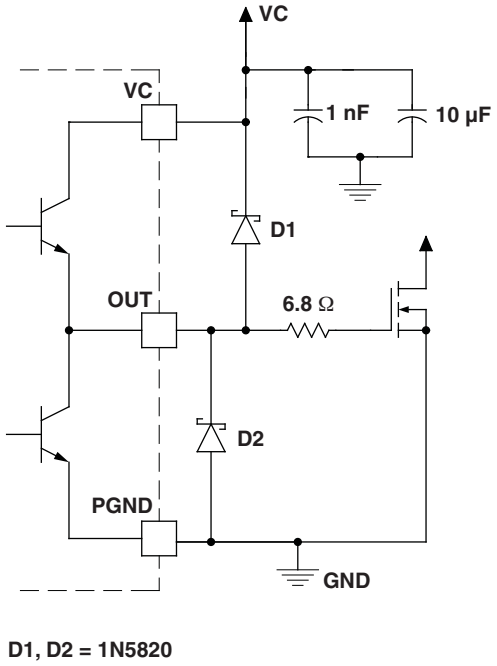


Figure 12. Power MOSFET Drive Circuit

Ground Planes

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high-frequency capacitor. The sources of the power MOSFET should connect to power ground, as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high-current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high-frequency capacitor. Low ESR/ESL ceramic 1-mF capacitors are recommended for both VCC and VREF. All analog circuitry should, likewise, be bypassed to the signal ground plane.

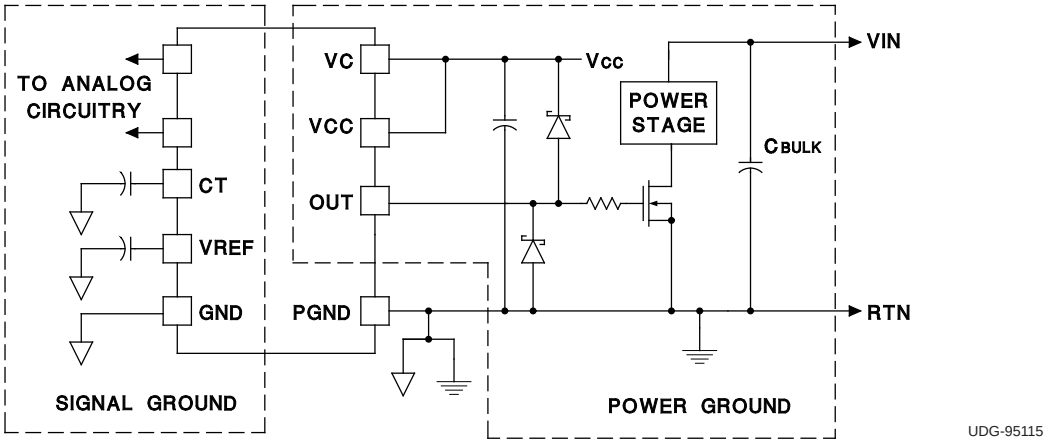


Figure 13. Ground Planes Diagram

Open-Loop Test Circuit

This test fixture is useful for exercising many functions of this device family and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

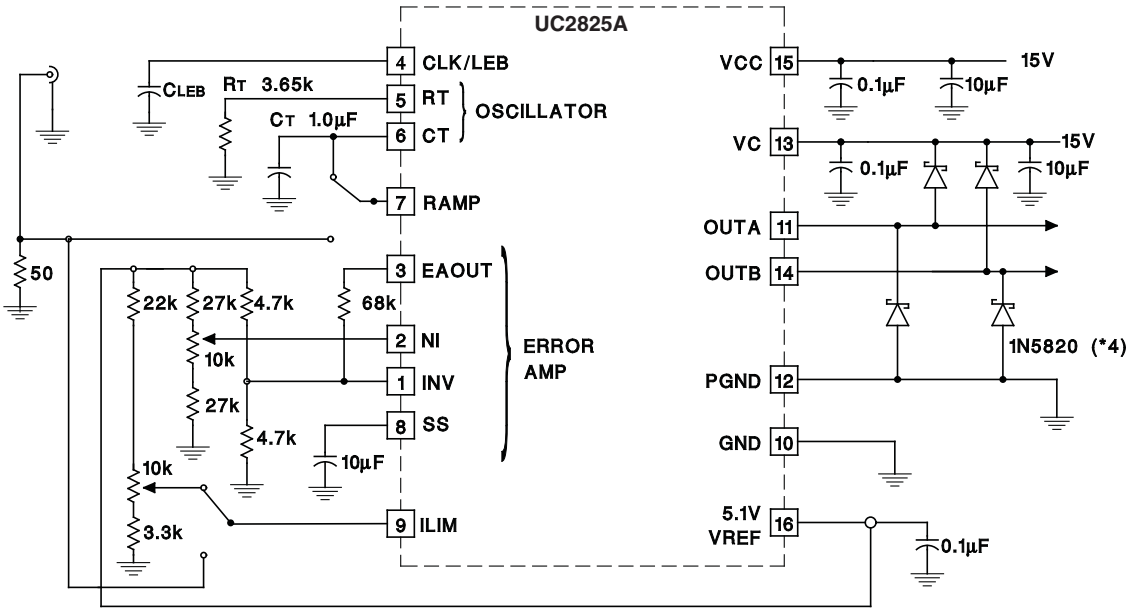


Figure 14. Open-Loop Test Circuit Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2825AQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UC2825AQDW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC2825A-Q1 :

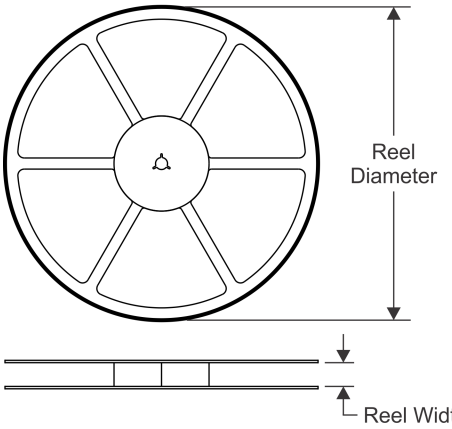
- Catalog: UC2825A
- Enhanced Product: UC2825A-EP

NOTE: Qualified Version Definitions:

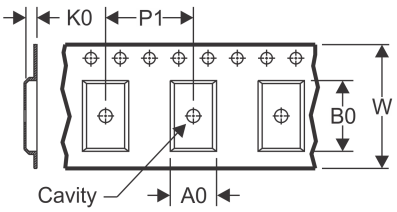
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

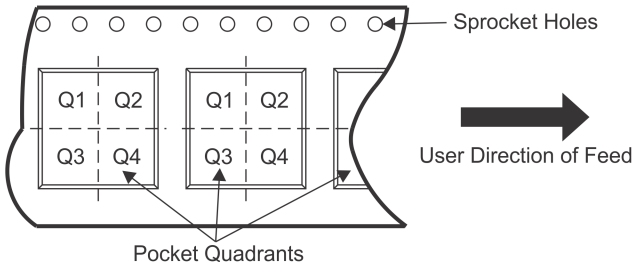


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

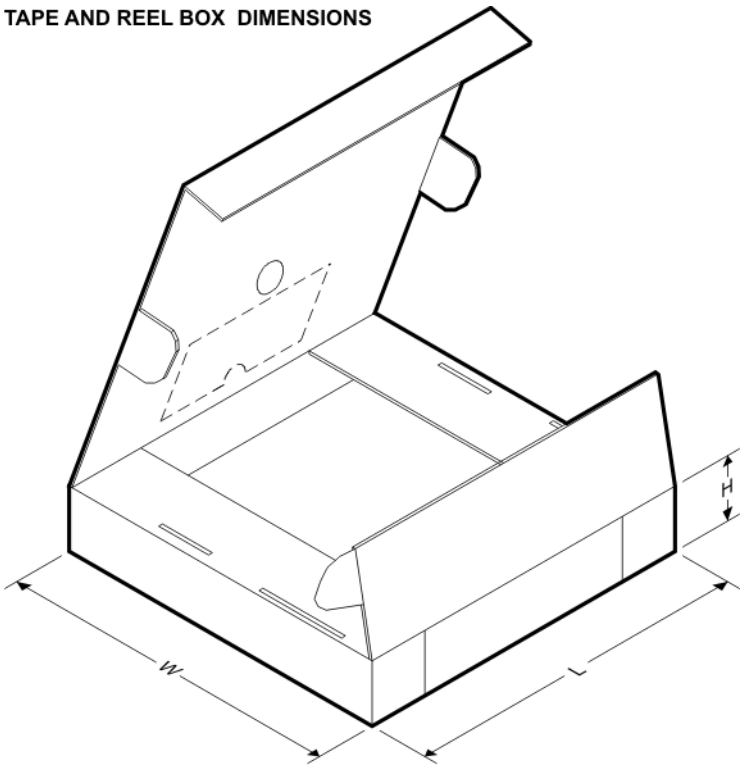
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2825AQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2825AQDWRQ1	SOIC	DW	16	2000	853.0	449.0	35.0

GENERIC PACKAGE VIEW

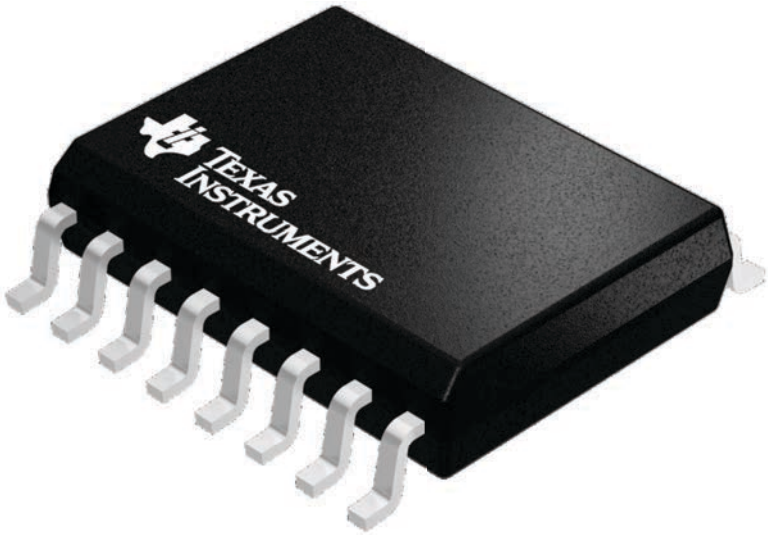
DW 16

SOIC - 2.65 mm max height

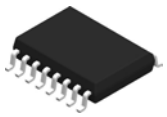
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

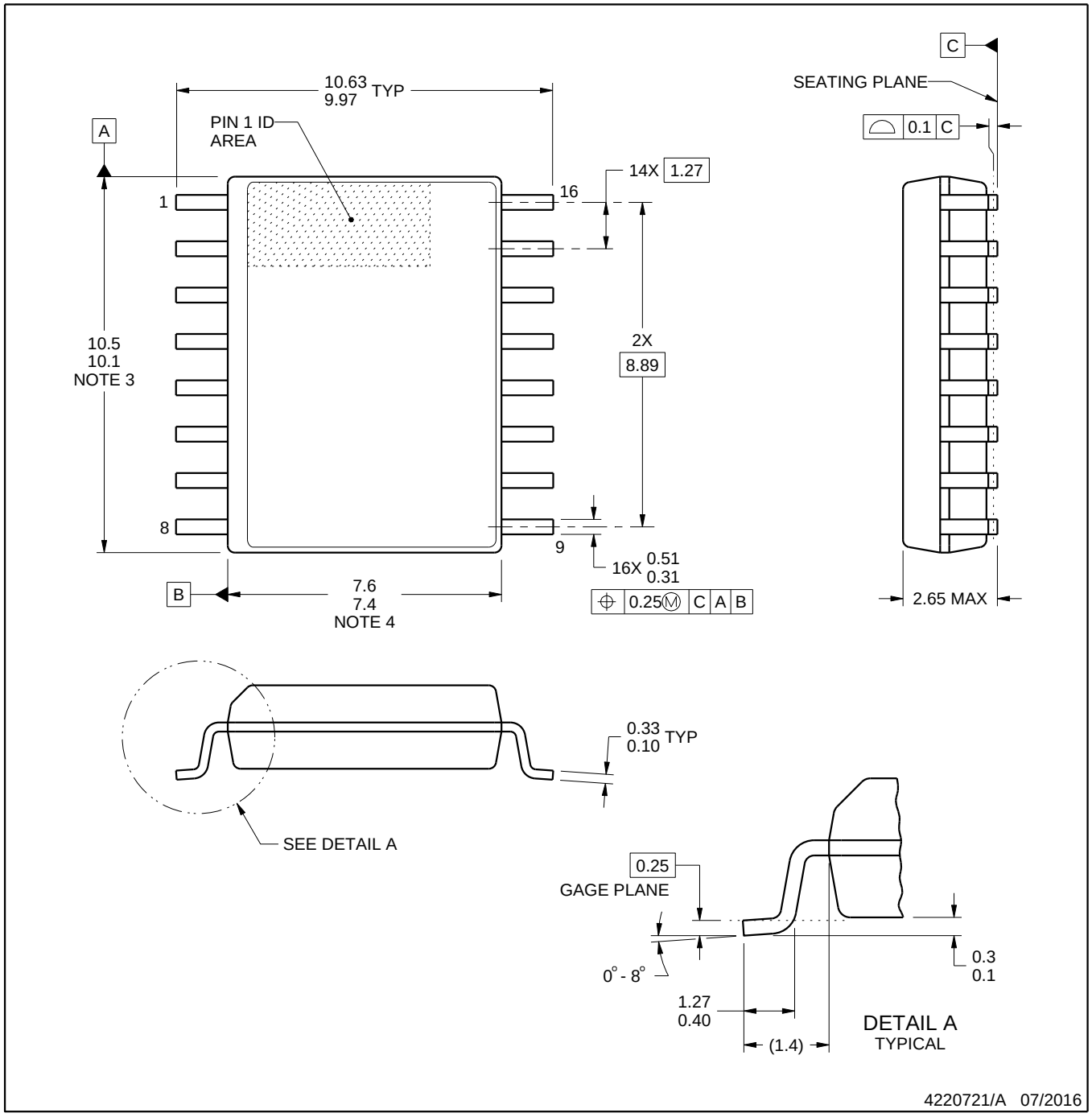


PACKAGE OUTLINE

DW0016A

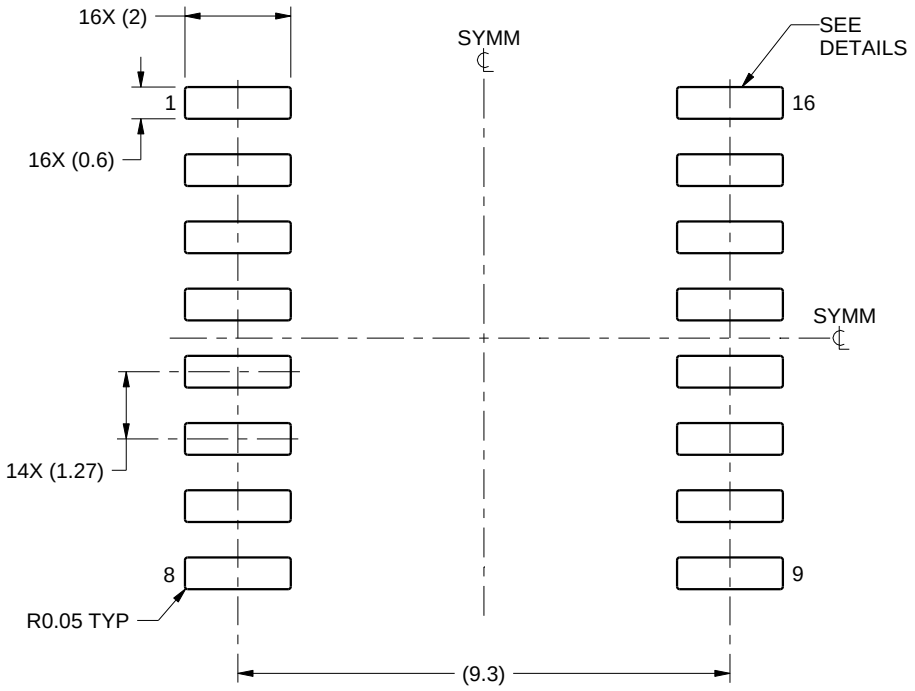
SOIC - 2.65 mm max height

SOIC

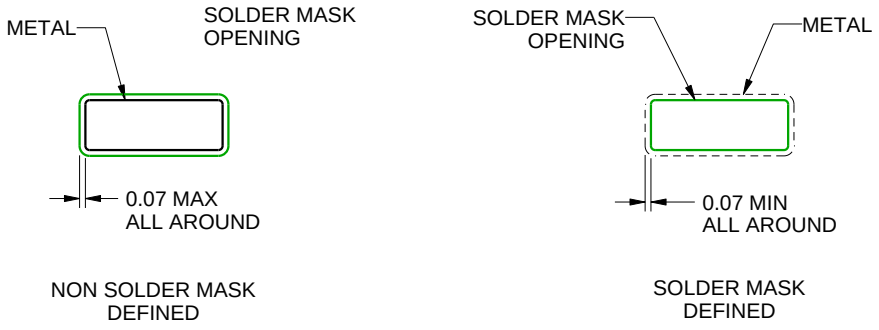


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

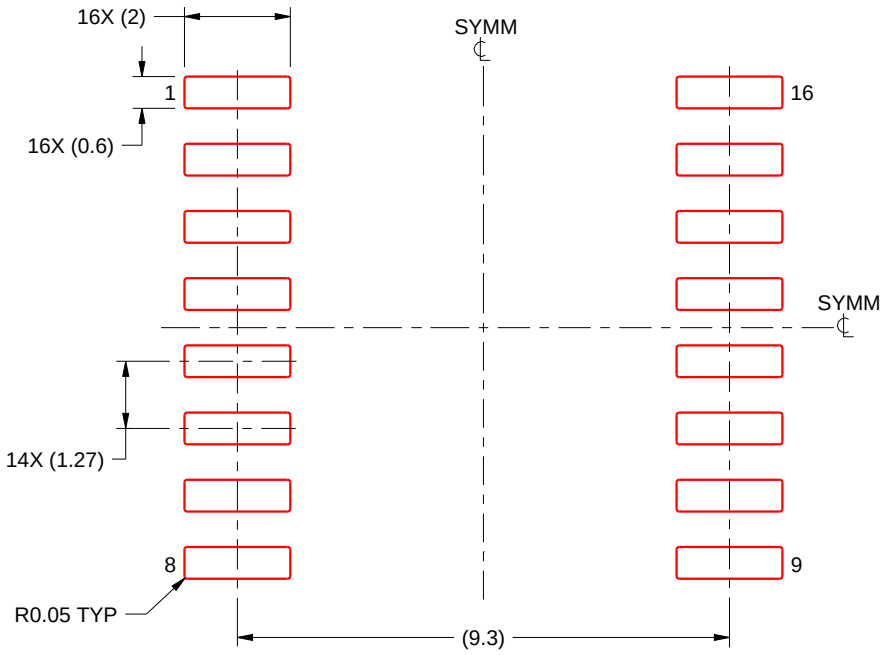


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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