UCC25800-Q1 Open-Loop LLC Transformer Driver for Isolated Bias Supplies

1 Features

- Open-Loop LLC transformer driver
- Ultra-low EMI
- 9-V ~ 34-V supply range
- 6-W output power with 24-V input
- Resistor programmable switching frequency from 100 kHz to 1.2 MHz
- Synchronization to external clock
- Programmable maximum dead-time with automatic dead-time adjustment
- Under voltage lockout
- Adjustable over-current protection threshold
- External disable function
- Input over voltage protection
- Over temperature protection (TSD)
- Fault-code output for system intelligence
- Latched and fault-auto-restart versions available
- 8-Pin DGN package with thermal pad

2 Applications

- Automotive Traction Inverter, IGBT and SiC Gate Driver Bias
- Automotive DC/DC, Automotive On-board Charger
- EV Charging Station, Automotive Super Charger
- UPS and Solar Inverters
- Industrial Motors, Elevators and Escalators

3 Description

The UCC25800-Q1 open-loop LLC transformer driver integrates the switching power stage, the control, and the protection circuits to simplify isolated bias supply designs. The LLC topology allows the design to utilize a transformer with higher leakage inductance, but much smaller parasitic primary-to-secondary capacitance. This low-capacitance transformer design enables an order of magnitude reduction in the common-mode current injection through the bias transformer. This makes the UCC25800-Q1 an ideal solution for the isolated bias supply in various automotive applications to minimize the EMI noise caused by the high speed switching devices. The UCC25800-Q1 operates with soft switching to further reduce the EMI noise.

UCC25800-Q1 has a programmable frequency range of 100 kHz to 1.2 MHz. This high switching frequency reduces the transformer size and footprint, as well as the overall cost of the bias supply. The integrated SYNC function allows the bias supplies in the system to be synchronized with an external clock signal, further reducing the system level noise.

The dead-time of UCC25800-Q1 is adjusted automatically to minimize the conduction loss and simplify the design. The maximum dead-time is programmable to ensure power stage design flexibility.

With the integrated low-resistance switching power stage, the UCC25800-Q1 can achieve a 6-W design with 24-V input. With a fixed input voltage that is above 9 V and below 34 V, the open-loop LLC converter control also helps the output regulation to remain ±5% when the load is above 10%.

The programmable over-current protection (OCP) allows flexibility on the power stage design to minimize the transformer size, further reducing the system cost. The protection features such as adjustable OCP, input OVP, TSD and the protection from pin faults ensure robust operation. A fixed 1.5-ms soft start reduces the inrush current during start-up and fault recovery.

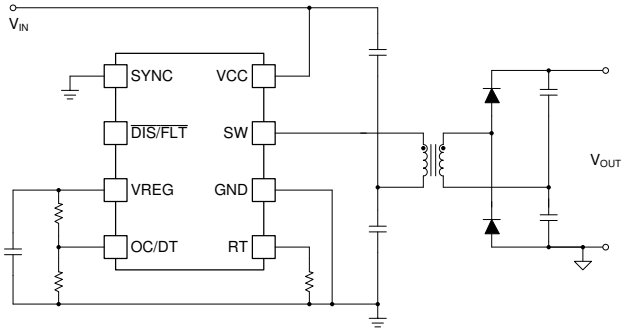
UCC25800-Q1 also provides a dedicated multi-function pin for external disabling, and fault code reporting. The fault code reporting sends the fault code once the bias supply is in the protection mode, allowing the system level controller to make more intelligent decisions during system failure modes.

The UCC25800-Q1 is packaged in an 8-pin DGN package with the thermal pad to enhance its thermal handling capability.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC25800A-Q1	S-PDSO-G8	4.90 mm × 3.00 mm
UCC25800L-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application Diagram

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2021	*	Advance Information release.

5 Device Comparison Table

Part Number	Fault Recovery Behavior
UCC25800A-Q1	Auto recovery
UCC25800L-Q1	Latch

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6 Pin Configuration and Functions

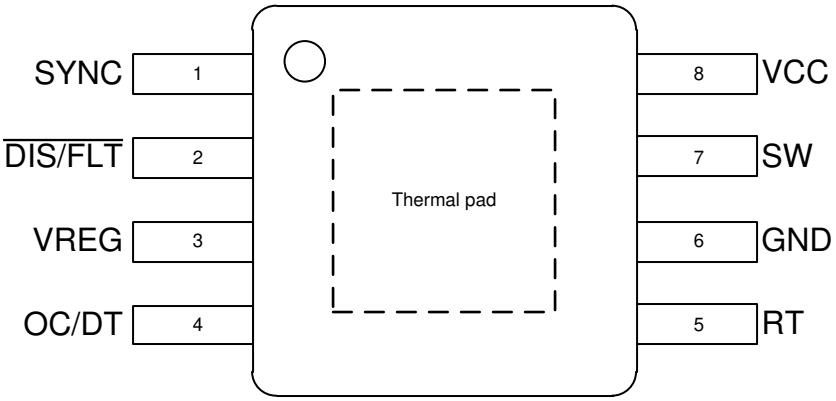

Figure 6-1. DGN Package 8-Pin PDSO Top View

6.1 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SYNC	1	I	External Clock input for frequency synchronization. The internal MOSFETs are switched synchronized with the rising edge of the SYNC signal, with half of the SYNC pin signal frequency.
$\overline{\text{DIS/FLT}}$	2	I/O	UCC25800-Q1 disable pin (active low) and fault code output pin.
VREG	3	O	Internal regulated reference. Put a decoupling capacitor right across VREG pin and GND with shortest distance. The VREG pin can also be used as external reference.
OC/DT	4	I	Voltage on this pin sets the maximum dead-time between the internal switching power devices. The Thevenin resistance on the pin is measured at start-up to set the OCP level.
RT	5	-	Switching frequency setting pin. Connect a resistor from RT pin to ground to set the converter switching frequency. The RT pin can be left open to operate the converter at the default 1.2-MHz switching frequency.
GND	6	-	The GND pin is the return for all the control and power signals. The layout should separate the power and control signals.
SW	7	-	The switch node of the integrated half-bridge. Connect this pin directly to the LLC resonant tank.
VCC	8	I	The input for power and control of UCC25800-Q1. A good high-frequency by-pass capacitor between VCC and GND is needed to ensure high-efficiency, low-EMI design. The by-pass capacitor layout should minimize the VCC-GND-By-pass capacitor loop to reduce the stresses on internal power devices. Referring to Section 15 for layout guidelines.

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7 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC		–0.3	40	V
VREG		–0.3	5.5	V
RT		–0.3	5.5	V
$\overline{\text{DIS/FLT}}$		–0.3	5.5	V
SYNC		–0.3	5.5	V
OC/DT		–0.3	5.5	V
SW		–1	VCC + 1	V
	Peak current	–5.5	5.5	A
	10 ns transient	tbd		V
I_{Qrms}	MOSFET RMS current		600	mA
T_J	Junction temperature	–40	150	°C
T_{AMB}	Ambient temperature	-40	125	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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8 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (SYNC, OC/DT, RT, and VCC)	±750	V
			Other pins	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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9 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	9		34	V
VREG	VREG current	0		1	mA
C_{VREG}	VREG capacitor	0.1		1	µF
R_{RT}	Switching frequency set pin resistor	10			kΩ
C_{RT}	Capacitor on RT			1000	pF
$\overline{DIS/FLT}$	Disable pin	0		5	V
OC/DT	OCP/Dead Time setting pin	1		3.9	V
$R_{OC/DT}$	Thevenin resistance	2.5		22.7	kΩ
$C_{OC/DT}$	Capacitor on OC/DT			1000	pF
SYNC	External sync input pulse voltage	2.4		5	V
$t_{SYNCmin}$	Minimum SYNC pulse width, high	150			ns
	Minimum SYNC pulse width, low	150			ns
SW	Half bridge output pin	–0.6		VCC + 0.6	V
f_{SW}	Switching frequency range	100		1200	kHz
IQ_{RMS}	Internal MOSFET RMS current rating			500	mA
IQ_{Peak}	Internal MOSFET peak current rating, steady state			1	A

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10 Thermal Information

THERMAL METRIC(1)		UCC25800-Q1 DGN (HVSSOP) 8 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	47.9	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	59.1	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	18.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.4	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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11 Electrical Characteristics

Unless otherwise stated: V_{VCC} = 15 V, R_{RT} = open, C_{VREG} = 470 nF, and -40 °C <T_J =T_A < 125 °C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$UVLO_R$	VCC turn on threshold	VCC rising	8	8.5	9	V
$UVLO_F$	VCC turn off threshold	VCC falling	7.5	8	8.5	V
OV_{SD}	VCC overvoltage shutdown threshold	VCC rising	35	37	39	V
OV_{RS}	VCC overvoltage reset	VCC falling	34	36	38	V
OV_{BLNK}	Overvoltage blanking time	VCC=40V	0.75	1.3	2	µs
SUPPLY CURRENT						
$IVCC_{UVLO}$	VCC current during UVLO	V_{VCC} = 7.5 V			500	µA
$IVCC_{RUN}$	Input current, not including FET current	f_{SW} = 1.2 MHz, $\overline{DIS/FLT}$ = 1, SW open, I_{VREG} = 0 mA, VCC = 12 V			10	mA
$IVCC_{DIS}$	Supply current when disabled	No switching, $\overline{DIS/FLT}$ = 0, I_{VREG} = 0 mA			800	µA
VREG OUTPUT						
VREG	Internal regulated reference	VREG open, I_{VREG} = 0 mA, $\overline{DIS/FLT}$ = 0	4.75	5	5.25	V
$VREG_{LINE}$	Line Regulation	VREG open, 9 V ≤ V_{VCC} ≤ 34 V			10	mV
$VREG_{LOAD}$	Load Regulation	0 mA ≤ I_{VREG} ≤ 1 mA	-100			mV
$VREG_{OK}$	Threshold for VREG GOOD	VREG rising	4.05	4.5	4.95	V
$VREG_{LOW}$	VREG fault threshold	VREG falling	3.6	4	4.4	V
MOSFETs						
RDSON	On Resistance	PMOS ISW=-500mA			0.75	Ω
		NMOS ISW=+500mA			0.5	Ω
OSCILLATOR						
f_{SW}	SW switching frequency	V_{RT} = 0.25 V	94	100	106	kHz
		V_{RT} = 2.5 V	0.94	1	1.06	MHz
		Default switching frequency, RT open	1.128	1.2	1.272	MHz
f_{SWtol}	Tolerance	10 kΩ ≤ R_{RT} ≤ 100 kΩ	94		106	%
Duty	Duty cycle	RT open	49	50	51	%
RT_{SHORT}	Short circuit fault theshold		130	150	170	mV
RT_{OPEN}	Open-circuit default f_{OSC} threshold		2.9	3	3.1	V
SYNC						
$SYNC_{RISNG}$	SYNC rising threshold	V_{SYNC} rising	2.0	2.2	2.4	V
$SYNC_{FALLING}$	SYNC falling threshold	V_{SYNC} falling	1.53	1.7	1.87	V
ADAPTIVE DEAD-TIME						
DT_HS_{TH}	High-side dead-time detection threshold with respect to VCC	SW rising		-1		V
DT_LS_{TH}	Low-side dead-time detection threshold	SW falling		1		V
DT_HS_{DELAY}	High-side turn on delay	From SW crossing DT_HS_{TH} to HS turning on		20	45	ns
DT_LS_{DELAY}	Low-side turn on delay	From SW crossing DT_LS_{TH} to LS turning on		20	45	ns
PROGRAMMABLE MAXIMUM DEAD-TIME						
OC/DT_{SHORT}	short threshold for OC/DT pin		450	500	550	mV
OC/DT_{OPEN}	open threshold for OC/DT pin		4.3	4.5	4.7	V

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Unless otherwise stated: V_{VCC} = 15 V, R_{RT} = open, C_{VREG} = 470 nF, and -40 °C <T_J =T_A < 125 °C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DT_{MAX}	Programmable maximum dead-time	$V_{OC/DT}$ = 3.9 V	45	50	55	ns
		$V_{OC/DT}$ = 1.9 V	135	150	165	ns
		$V_{OC/DT}$ = 1 V	1.35	1.5	1.65	µs
OVER-CURRENT PROTECTION						
$I_{OCP1max}$	First level maximum OCP setting threshold	Low side only	0.9	1	1.1	A
$OCP1_{TO}$	OCP1 time out	Peak current exceeds threshold time out to trigger OCP1 fault		2		ms
$I_{OCP2max}$	Second level maximum OCP threshold	Low side and high side	4.5	5	5.5	A
$OCP2_{FILTER}$	OCP2 filter time	Continuous over-current to trigger OCP2 fault, low side and high side		100		ns
OVER-TEMPERATURE PROTECTION						
TSD	Thermal shutdown threshold	$T_J = T_A$ (1)		160		°C
T_{HYST}	Hysteresis	$T_J = T_A$ (1)		20		°C
ENABLE_DISABLE FUNCTION						
EN_{TH}	Enable threshold	$\overline{DIS/FLT}$ rising	2	2.2	2.4	V
DIS_{TH}	Disable threshold	$\overline{DIS/FLT}$ falling	1.53	1.7	1.87	V
I_{pd_DIS}	Internal pull down disable current	$V_{\overline{DIS/FLT}}$ = 5 V	650	750	850	µA
$RESTART_{DEL}$	Restart delay after fault	Non-latch version		100		ms
$FLT_{RSTHmin}$	minimum high pulse width on $\overline{DIS/FLT}$ pin to reset the latched fault				3	µs
$FLT_{RSTLmin}$	minimum low pulse width on $\overline{DIS/FLT}$ pin to reset the latched fault				3	µs

(1) Not production tested. Ensured by design

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12 Detailed Description

12.1 Overview

Modern high voltage and high power inverter and motor drive applications require floating bias supply voltages to power at least the high-side totem-pole switches, whose source (and gate) voltages move up and down with the inverter switch-node. The traditional way of providing small amounts of isolated bias power has been to use a Flyback converter. Often a single Flyback with multiple outputs could generate the required rails for all the switches. However, issues with reliability, redundancy, shock and vibration testing, noise immunity and particularly EMI and common mode current have led to a trend away from the Flyback and centralized architecture toward distributed open-loop approaches. The open-loop approaches such as 50% duty cycle push-pull, open-loop half bridge or full bridge without an output inductor are deployed while the Flyback or Flybuck™ continue to be used by some designs to provide regulated outputs despite the larger common-mode capacitance (transformer primary side to secondary side parasitic capacitance). With the adoption of SiC and GaN devices, the inverter power stage switches at a much higher dv/dt. This causes much larger common-mode current injection through the isolated bias transformers. This drives the needs for a bias supply design with minimum parasitic capacitance. This desire to further reduce the primary-to-secondary capacitance without suffering performance degradation has led some designs to deploy resonant topologies such as the LLC. As the leakage inductance in an LLC is part of the power train, the topology can enable a higher leakage inductance transformer to be used with an associated reduction in the parasitic primary-secondary capacitance. UCC25800-Q1 is a small simple controller enabling this topology to be deployed with low component count, integrated protection features, high switching frequency, high parameter tolerance and robust operation. An 8-pin DGN package with thermal pad is used to provide up to 6-W power handling capability with 24-V input.

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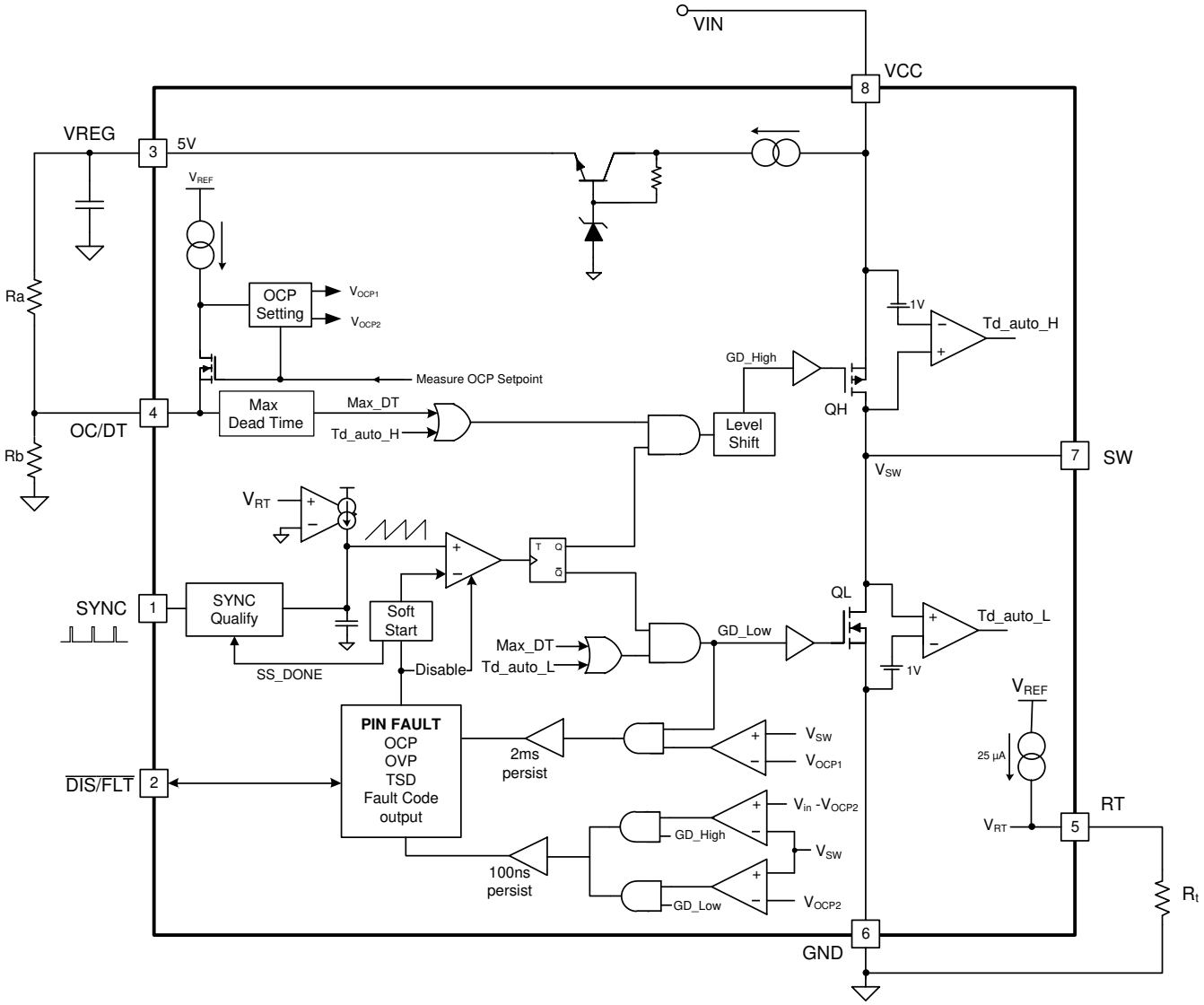
12.2 Functional Block Diagram



12.3 Feature Description

UCC25800-Q1 is an 8-pin open-loop LLC transformer driver that integrates all the control and power devices. It converts a fixed input voltage to an isolated voltage source through an isolation transformer. The relationship between the output voltage and input voltage is fixed, which is determined by the transformer turns-ratio and the rectification method. The open-loop control, together with the LLC resonant converter operation, makes the solution more robust, smaller size, higher efficiency, as well as lower EMI and common mode noise. The UCC25800-Q1 minimizes the external components while provides design flexibility and the robust protection features. The 1.2-MHz maximum switching frequency reduces the transformer size and cost, making it easier to pass the shock and vibration test in the automotive applications. The fault code output allows the designer to identify the protection mode, during the development stage, as well as during normal operation. This makes the development process much easier. It also enables the system controller to make intelligent decisions when bias supply faults happen.

12.3.1 Power Management

The UCC25800-Q1 is powered through VCC pin. When VCC pin voltage is below the UVLO rising threshold ($UVLO_R$), the VREG pin 5-V regulator is disabled (VREG = 0 V). Once the VCC pin voltage exceeds $UVLO_R$, the 5-V regulator is enabled and VREG pin rises, while the $\overline{DIS/FLT}$ pin is internally pulled low through an internal

750-µA current source, ($\overline{DIS/FLT}$ = 0 V). Once the VREG exceeds 4.5 V ($VREG_{OK}$), the $\overline{DIS/FLT}$ pin is released. If the $\overline{DIS/FLT}$ pin is not pulled low externally, it rises to VREG pin voltage level via an internal 100-kΩ pull up resistor. When $\overline{DIS/FLT}$ pin voltage exceeds the rising enable threshold (EN_{TH}), the internal regulators and references are turned on and the Thevenin resistance on the OC/DT pin is read to set the over current protection (OCP) thresholds. After this process is completed the faults are checked and if they are all cleared, the oscillator is enabled and the power stage starts switching. This process normally takes couple hundreds of µs.

If a fault is detected, the internal pull-down current source on the $\overline{DIS/FLT}$ pin is activated, the power stage stops switching and the fault code is outputted.

The rise time of the $\overline{DIS/FLT}$ pin depends on the external loading on the pin. An external pull-up can be added to the pin if there is concern over noise immunity. The values are specified in Section 12.3.6.

When the VCC pin voltage is above the $UVLO_R$ threshold and $\overline{DIS/FLT}$ pin is pulled low externally the UCC25800-Q1 remains disabled with $IVCC_{DIS}$ = 500 µA.

If, after a completed power up sequence, VCC falls below the UVLO falling threshold ($UVLO_F$), the power stage switching is immediately stopped. The VREG pin voltage regulator is disabled making the VREG pin voltage fall.

The VCC pin current is a combination of the IC bias current and the power stage current. It is important to have a low ESL bypass capacitor to minimize the current loop among this capacitor and VCC, GND pins. Refer to Section 15 for details.

12.3.2 Oscillator

The UCC25800-Q1 internal oscillator sets the switching frequency of the power stage. It operates at a 50% duty cycle. Its frequency is set by the voltage on the RT pin. A 25-µA current source flows out of the pin so that the switching frequency can be set by connecting a resistor to ground. The internal oscillator is illustrated in Figure 12-1.

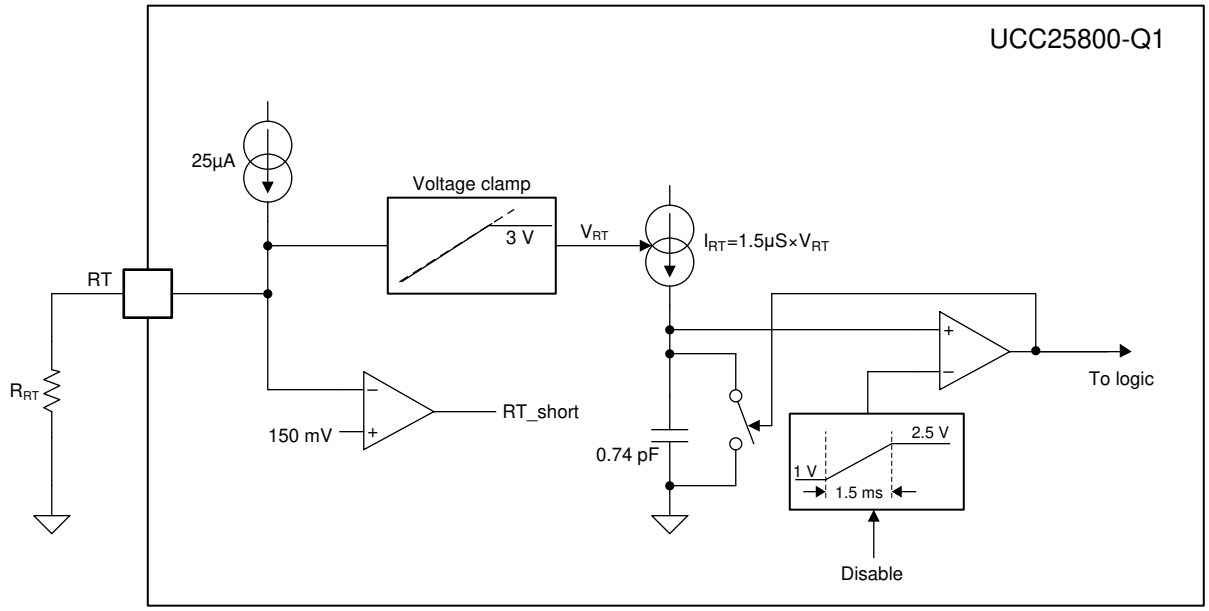


Figure 12-1. Equivalent circuit for internal oscillator

The RT pin resistor for desired switching frequency can be calculated using Equation 1.

$$f_{SW} = R_{RT} \times \frac{10\,Hz}{\Omega} \quad (1)$$

If the RT pin is left open, or an RT pin resistor value results in an RT pin voltage at RT_{OPEN} threshold or above, the power stage will operate with the default switching frequency of 1.2 MHz. If the RT pin voltage is below 150

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mV, the UCC25800-Q1 considers the RT pin shorted to ground and declares a fault. The programmable voltage range on the RT pin is 250 mV to 2.5 V. The relationship between the power stage switching frequency and the RT-pin voltage is shown in Figure 12-2.

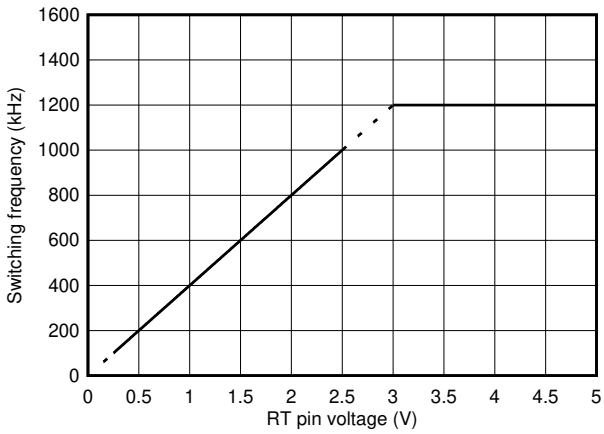

Figure 12-2. Relationship between switching frequency and RT-pin voltage

To avoid the excessive current stress during the start-up process, UCC25800-Q1 integrates a soft-start function. The oscillator is soft started by ramping the oscillator reference from 1 V to 2.5 V, which results in the switching frequency reducing from 2.5 times of the set frequency to the set frequency. Because the current source in the oscillator remains the same while the reference changes, the switching cycle decays linearly. The soft-start time is fixed internally at 1.5 ms. This long soft-start time limits the inrush current when charging large output capacitors. The soft-start is enabled during the start-up and fault recovery process. The switching frequency variation during the start-up time is shown in Figure 12-3.

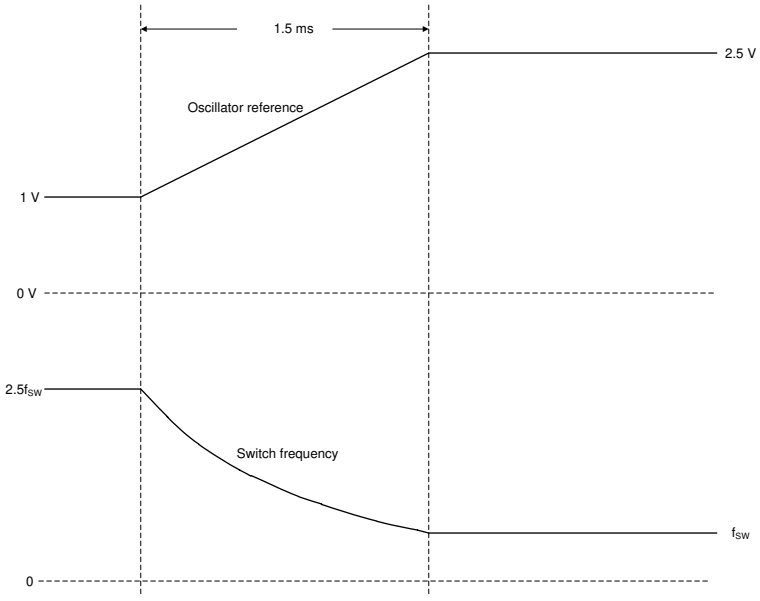

Figure 12-3. Switching frequency during soft start time

In soft-start, the first pulse from the oscillator is a half of the second pulse width (25% of the period at the starting switching frequency) and followed immediately by 50% duty cycle pulses. This is to ensure the LLC transformer magnetizing current is symmetrical from the first pulse to minimize ringing in the system. The high-side switch is always turned on at the first pulse to avoid uncertainty of the circuit operation.

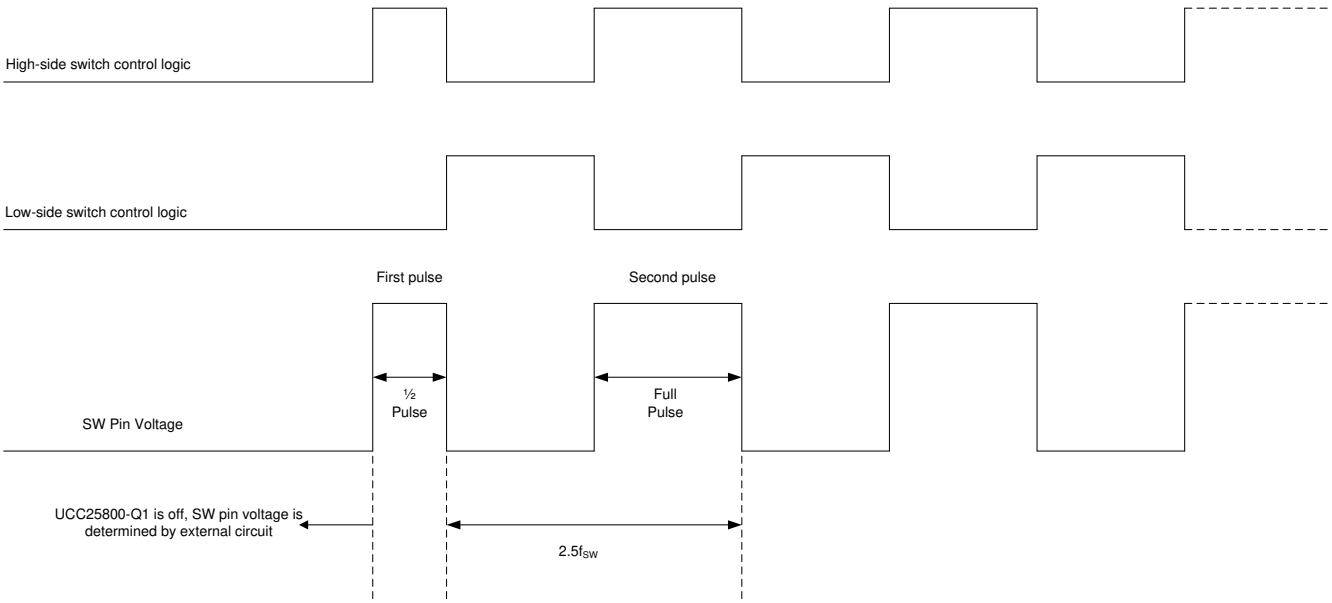

Figure 12-4. SW pin voltage and control logic at the first switching cycle (dead-time is not shown)

12.3.3 External Synchronization

The switching frequency of the UCC25800-Q1 can be synchronized through an external signal connected to the SYNC pin.

In the external synchronization mode, the switching frequency of the resonant converter is half of the SYNC pin signal frequency. Given that, to ensure the output voltage remains within the normal operation range, the half of the frequency of external synchronization signal needs to be between 15% and 30% (nominal) above the programmed switching frequency with a tolerance of 5% or less, as described in Equation 2. A minimum high and low pulse width of 150 ns is required. The SYNC pin logic is compatible with TTL and CMOS levels for the design simplicity. It is recommended to use 50% duty cycle signal.

$$1.15f_{SW} < \frac{1}{2} f_{SYNC} < 1.3f_{SW} \tag{2}$$

where

- f_{SW} is the RT pin programmed power stage switching frequency
- f_{SYNC} is the SYNC pin signal frequency

The external synchronization signal can be applied before or after the UCC25800-Q1 starts up. The external synchronization signal is ignored during the 1.5-ms soft-start time. The switching frequency during soft-start is based on the RT pin voltage as described in Section 12.3.2. After the soft-start, if an external synchronization signal is present and its frequency and pulse width are within the specified range, the switch node is driven by the SYNC pin signal. UCC25800-Q1 also integrates a hand-off algorithm so that when the switching frequency transitions from internal oscillator to the external synchronization signal, the disturbance is minimal and transformer saturation is avoided.

The hand-off algorithm firstly checks the external synchronization signal to ensure it is within the range. If the frequency is not within the acceptable range, the hand off doesn't happen. If the frequency is within the acceptable range, the hand-off algorithm starts to search for optimal transition point and locks the switching frequency with the external SYNC signal. After the frequency is locked, the hand-off algorithm stops monitoring the SYNC pin frequency. It is important to ensure external synchronization source has a stable frequency. There is a watchdog inside UCC25800-Q1 to prevent the external frequency from falling below the set frequency (the watchdog doesn't check if the SYNC pin frequency goes above the range). Once the SYNC pin frequency

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drops below the set frequency, the synchronization is lost and the converter operates with the set frequency determined by RT pin voltage.

The Figure 12-5 shows an oscilloscope screen capture for the controller transition from internal oscillator to the external synchronization signal. The smooth transition can be observed and the SW pin current sees minimal disturbance.

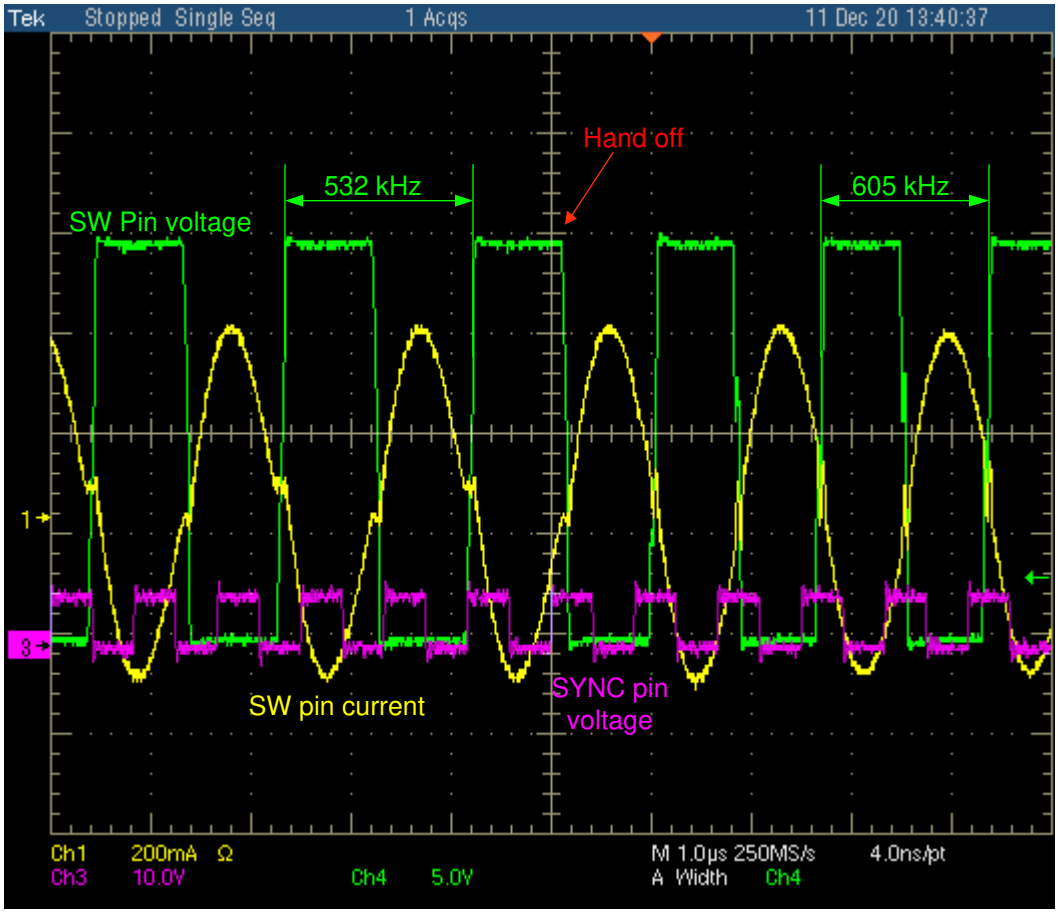

Figure 12-5. Transition from internal oscillator to external synchronization

The internal MOSFET gate drives are toggled on each SYNC pin voltage rising edge, so the switch-node frequency is equal to half of the SYNC pin signal frequency, as shown in Figure 12-6. Due to the internal filter delays, the SW pin switching edge is not aligned with the SYNC pin switching edge. There is ~150ns of delay.

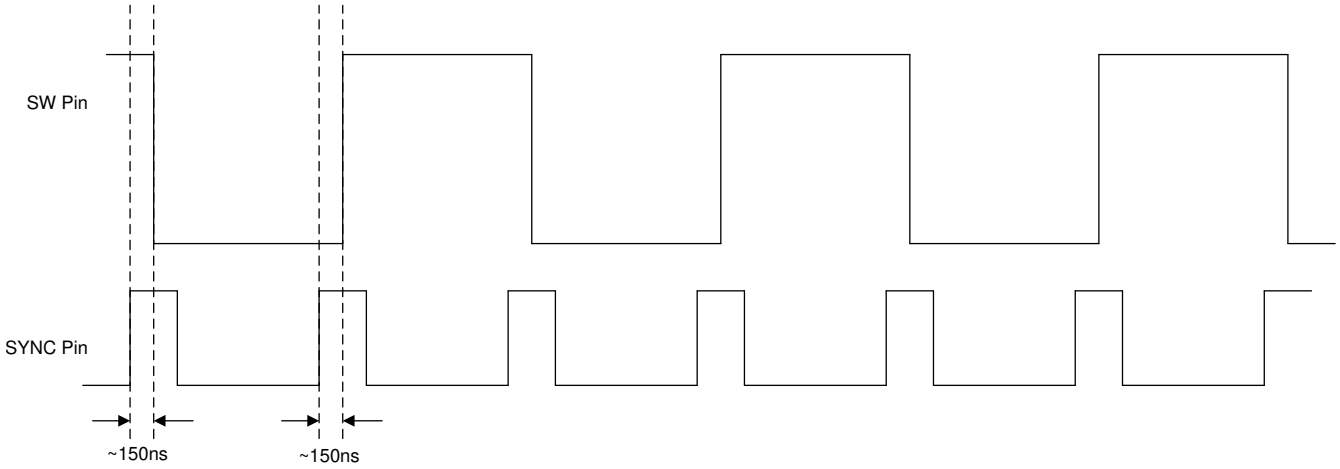

Figure 12-6. Switching frequency driven from external SYNC signal

12.3.4 Dead-Time

A dead-time is needed between the turn off of one switch and the turn on of the other switch to avoid shoot through. This also allows the switch-node voltage to transition to the opposite rail voltage, which reduces switching loss and EMI noise.

12.3.4.1 Adaptive Dead-time

The dead-time in UCC25800-Q1 is detected automatically once the switch-node voltage slews to within 1 V of the opposite rail. This slewing of the node is driven by the current flowing though the SW pin into the resonant tank at the end of the each MOSFET on-time. There must be sufficient current flowing in the SW pin at the end of the on-time to drive the SW pin voltage to the opposite rail. A maximum dead-time is programmed by the voltage on the OC/DT pin. If the SW pin voltage crossing the threshold is not detected within the maximum programmed dead-time, the internal MOSFET is switched on anyway. The adaptive dead-time operation is demonstrated in Figure 12-7

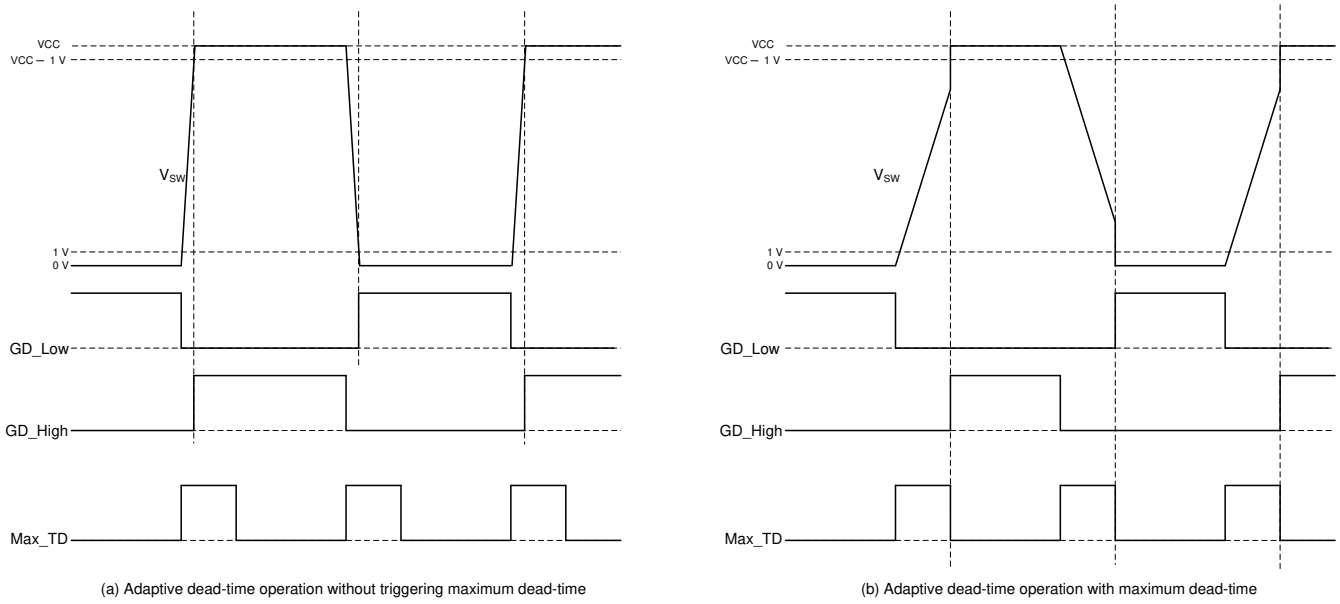

Figure 12-7. Adaptive dead-time operation

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12.3.4.2 Maximum Programmable Dead-time

During operation, the voltage on the OC/DT pin sets a maximum duration of the dead-time. If the adaptive dead-time has not triggered the turn on of the internal MOSFET within this time, it will be switched on when the maximum dead-time is expired. The relationship between the OC/DT pin voltage and this maximum programmable dead-time is shown in the graph below and given by Equation 3. The UCC25800-Q1 also limits the maximum dead-time to be 1/8 of the switching cycle. Therefore, the programmed maximum dead-time would be the lower value of these two.

$$DT_{MAX} = \frac{150ns \cdot V}{V_{OC/DT} - 0.9V} \quad (3)$$

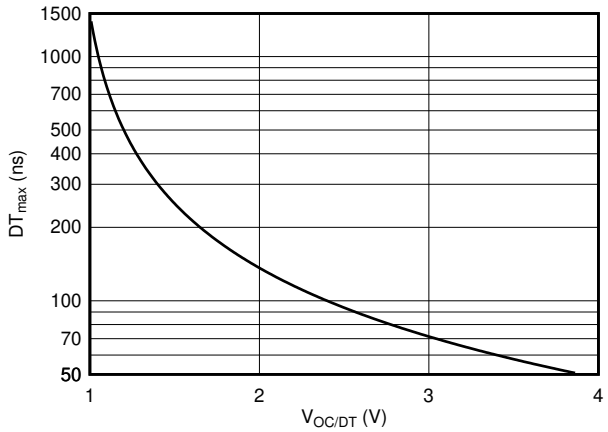

Figure 12-8. Maximum dead time vs. OC/DT pin voltage

When the OC/DT pin voltage falls below 0.5 V, it triggers the pin-short protection. UCC25800-Q1 shuts down. When the OC/DT pin voltage is between 0.5 V to 1 V, the maximum dead-time is set at its maximum value of 1.25 µs. When the OC/DT pin voltage is between 3.95 V and 4.5 V, it triggers the DT-out-of-range fault and UCC25800-Q1 shuts down. When the OC/DT pin voltage is above 4.5 V the UCC25800-Q1 shuts down due to the OC/DT open pin fault protection. When the OC/DT pin voltage is above 3.9 V, the maximum dead-time is set at its minimum value of 50 ns.

12.3.5 Protections

UCC25800-Q1 provides a full set of protection functions to improve the system level reliability, meeting automotive design requirements. The protection functions include programmable two-level over current protection (OCP), input under voltage protection (UVLO), input over-voltage protection (OVP), and over-temperature protection (TSD). The UCC25800-design considers possible pin fault conditions such as pin open, pin short, etc. Extra protection mechanisms are also integrated inside the design. Furthermore, UCC25800-Q1 has two options for the fault response: fault auto-recovery and latched fault recovery. This helps to meet different system requirements.

12.3.5.1 Over-Current Protection

The UCC25800-Q1 has two levels of over-current protection (OCP).

- The first level (OCP1) triggers if the current through the low-side MOSFET exceeds programmed threshold I_{OCP} during its on-time in each switching cycle for 2 ms. Refer to OCP Threshold Setting for OCP1 threshold programming details.
  - OCP1 detection is only based on low-side MOSFET current, when the SW pin current flows into the SW pin
- The second level (OCP2) triggers if the current in either the high- or low-side MOSFET exceeds $5 \cdot I_{OCP}$ for 100 ns.
  - The OCP2 threshold is set significantly above OCP1 threshold to allow the unit to cope with heavy load surges for a short duration, or during the start-up to charge the large output capacitor. If OCP2

is exceeded, it indicates that there is a serious fault in the system. OCP2 tracks OCP1 so that events like output overload can still trip OCP2, even if the current limit is set well below the UCC25800-Q1's maximum current limit.

- During soft-start
  - The OCP1 is disabled
  - The OCP2 threshold is fixed at its maximum value of 5 A
- After soft-start
  - OCP1 is enabled, with the threshold I_{OCP} equal to the programmed value
  - OCP2 threshold becomes 5 times of the programmed I_{OCP} level.
- The OCP1 over-current timer is implemented as an up-down counter to ensure that the repetitive short over-current events as well as a sustained 2 ms over current trigger the OCP.
  - OCP1 over-current timer counts up if the SW current crosses I_{OCP} for longer than 100 ns in each switching cycle
  - OCP1 over-current timer counts down if the SW current doesn't cross I_{OCP} for longer than 100 ns in the entire switching cycle
  - The internal counter for OCP1 over-current timer counts up in 2 ms from 0 to the trip threshold and counts down in 180 ms from the trip threshold down to 0.
- OCP2 detection has an analog filter which filters out pulses of less than 100 ns.

A minimum restart time of 100 ms is imposed before restarting from over current protection to keep the RMS current in the UCC25800-Q1 below its limit. The OCP behaviors are illustrated in Figure 12-9 and Figure 12-10.

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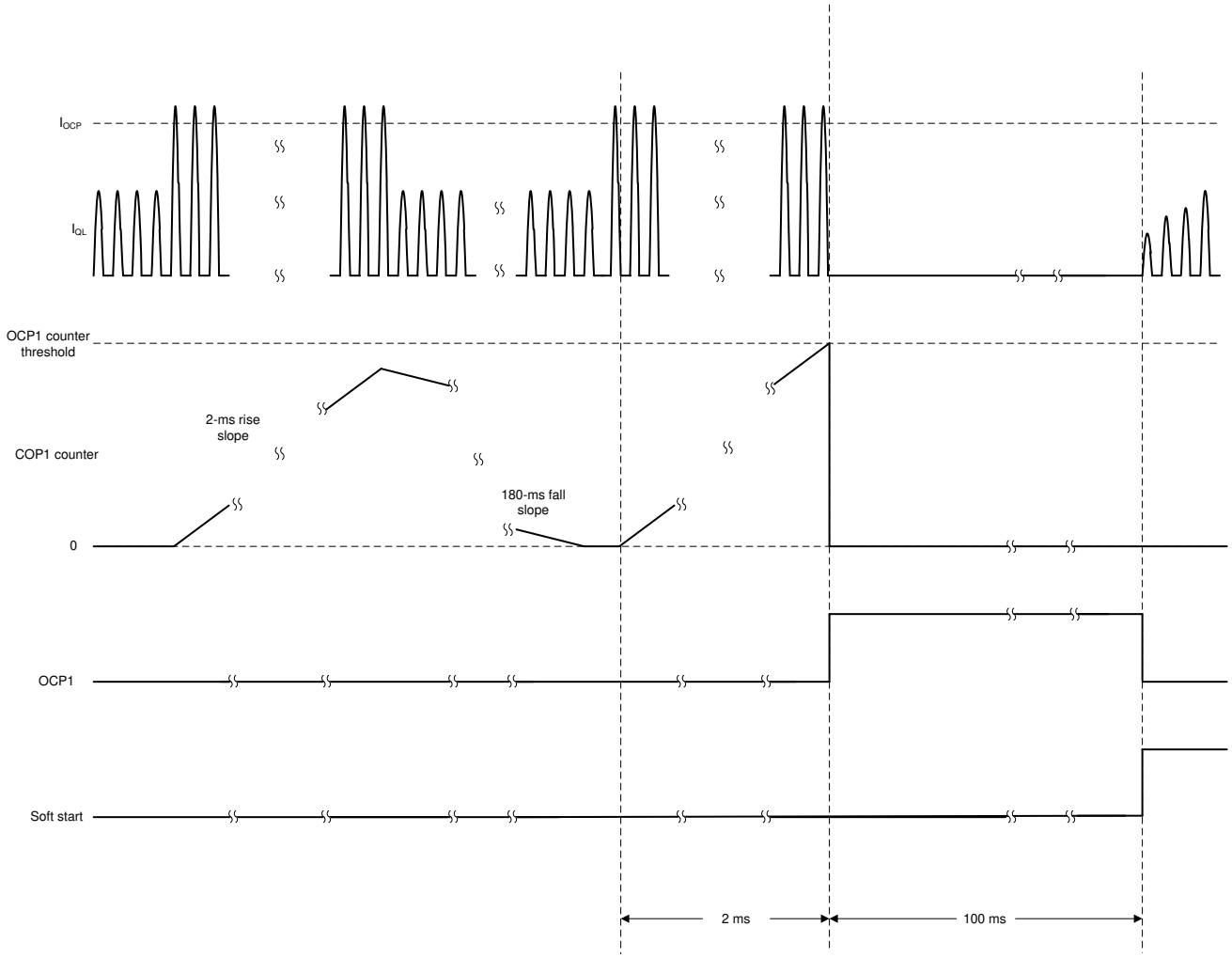


Figure 12-9. OCP1 protection and recovery behavior

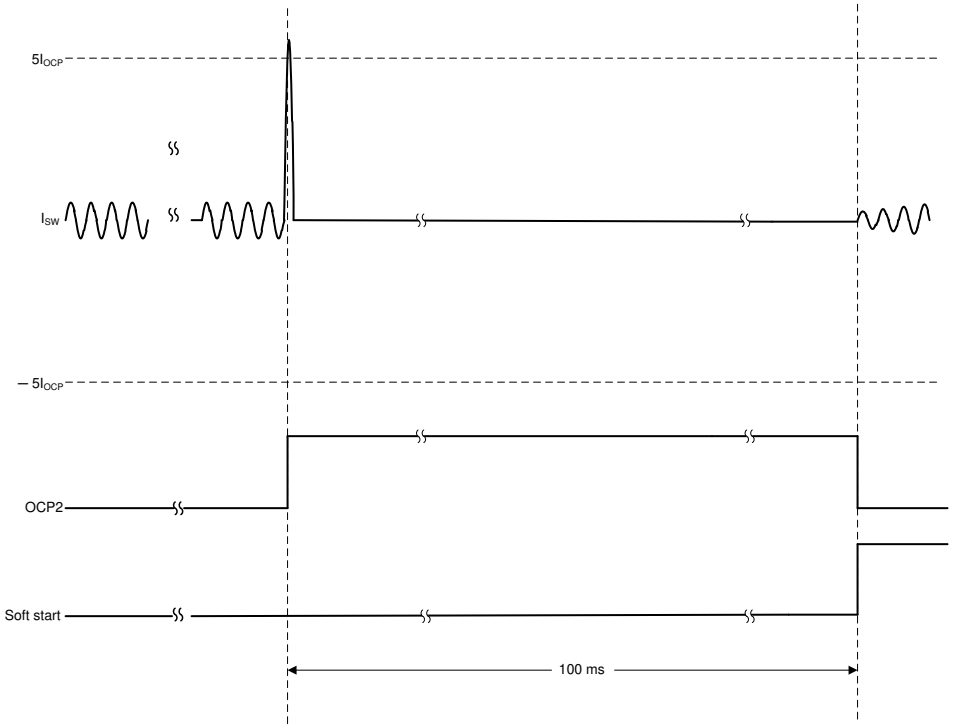
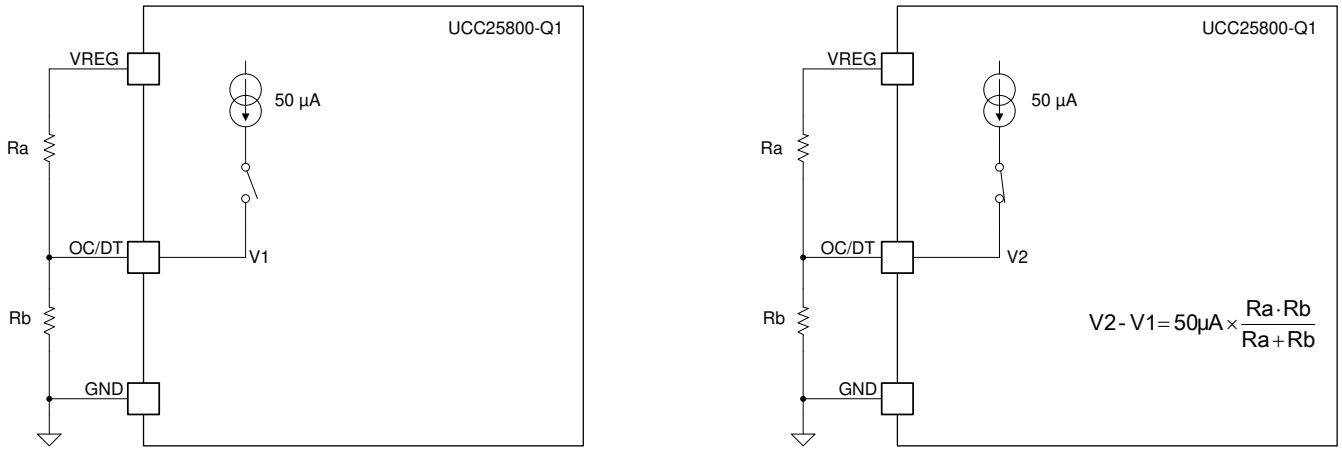


Figure 12-10. OCP2 protection and recovery behavior

12.3.5.1.1 OCP Threshold Setting

The UCC25800-Q1 is able to support 6-W output power with 24-V input. For designs with lower power levels, the over-current protection (OCP) threshold can be adjusted accordingly to limit the maximum output power to improve the system reliability.

The OCP threshold setting shares the same pin as the maximum dead-time programming through OC/DT pin. During the UCC25800-Q1 start-up, after its VREG pin settles down to its final value, an internal 50-µA current source flowing out of OC/DT pin is turned on and off. The voltage on the OC/DT pin is measured at the current source on and off conditions. The measured voltage difference is used to set the OCP threshold. After the OCP setting is determined, the current source is turned off, so that the voltage on the OC/DT pin can be used for the maximum dead-time setting.



(a) Current source is off

(b) Current source is on

Figure 12-11. Equivalent circuit for reading OCP setting

According to the Thevenin's theorem, the measured voltage difference is the current source multiplied by the Thevenin resistance on the voltage divide on OC/DT. The OCP settings using different Thevenin resistance are summarized in Table 12-1. The Thevenin resistance can be calculated using Equation 4.

$$R_{th} = \frac{Ra \cdot Rb}{Ra + Rb} \tag{4}$$

Table 12-1. OCP Settings

	OCP1 _1	OCP1_2	OCP1_3	OCP1_4	OCP1_5	OCP1_6
R_{th}	22.25 kΩ ~ 23.15 kΩ	16.4 kΩ ~ 17 kΩ	11.7 kΩ ~ 12.1 kΩ	7.95 kΩ ~ 8.25 kΩ	4.9 kΩ ~ 5.1 kΩ	2.45 kΩ ~ 2.55 kΩ
OCP1 threshold (I_{OCP})	1/6 $I_{OCP1max}$	1/3 $I_{OCP1max}$	1/2 $I_{OCP1max}$	2/3 $I_{OCP1max}$	5/6 $I_{OCP1max}$	$I_{OCP1max}$
OCP2 threshold during soft-start	5 A	5 A	5 A	5 A	5 A	5 A
OCP2 threshold after soft-start	5/6 $I_{OCP1max}$	5/3 $I_{OCP1max}$	5/2 $I_{OCP1max}$	5/3 $I_{OCP1max}$	25/6 $I_{OCP1max}$	5 $I_{OCP1max}$

To ensure accurate reading of the Thevenin resistance, the time constant of R_{th} and any capacitance connected to the OC/DT pin should not be greater than 20 µs. For this reason, the maximum recommended capacitance on the pin is 1 nF. It is not required to add capacitance to the pin.

The OC/DT pin voltage during start-up is illustrated in Figure 12-12.

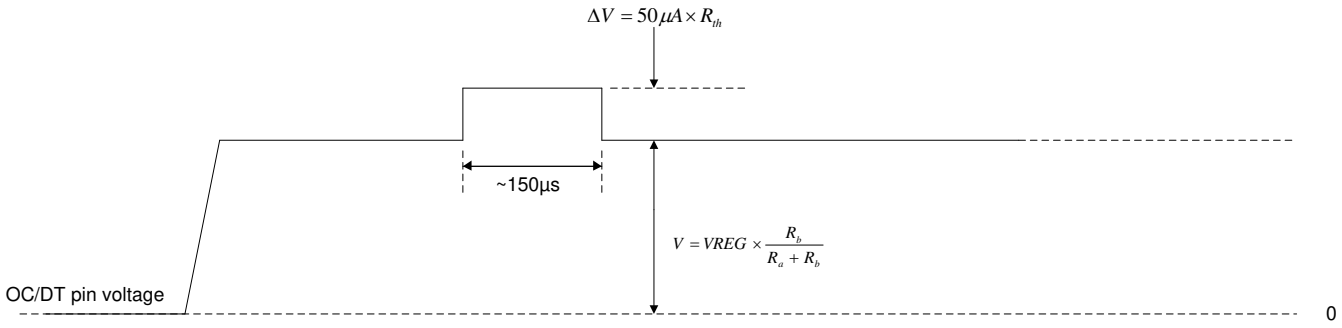


Figure 12-12. OC/DT pin voltage during start-up

12.3.5.1.2 Output Power Capability

Figure 12-13 below shows the output power capability of the UCC25800-Q1 at different input voltages and switching frequencies with its highest OCP set-point (I_{OCP} = $I_{OCP1max}$ = 1 A), based on an input-output efficiency of 90%. There are two limiting factors on the UCC25800-Q1 power handling capability, the OCP1 threshold and the thermal stress.

OCP1 serves as an over-power limit rather than over current protection since it has a 2-ms timer. Given its maximum value is 1 A and considering the sinusoidal current shaped, UCC25800-Q1 limits its maximum output power proportionally to the input voltage. In Figure 12-13, the 100-kHz line is approximately the OCP1 limit.

The thermal limitation is to prevent the UCC25800-Q1 junction temperature from becoming too high. Assuming its loss is only the IC bias consumption and the MOSFET conduction loss, at 125ºC ambient temperature and 90% efficiency, the maximum output power creates the loss to make the UCC25800-Q1 junction temperature reach 150ºC. From the curves shown in Figure 12-13, it can be observed, with higher the switching frequency, the IC power consumption becomes more and the maximum power capability drops.

The power handling capability can be increased by increasing the input voltage or lowering the switching frequency, but it can't exceed the OCP1 limit.

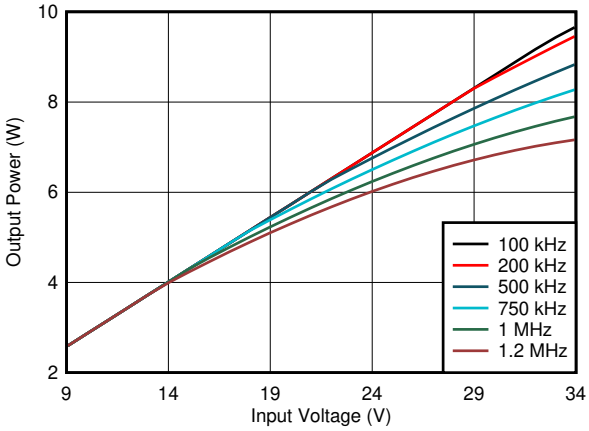


Figure 12-13. Power rating curves

12.3.5.2 Input Over-Voltage Protection (OVP)

Due to the lack of feedback, UCC25800-Q1 is equipped with an input over-voltage protection to prevent the output voltage from becoming too high, in case its input voltage becomes too high. If the VCC-pin voltage exceeds the over-voltage set-point of OV_{SD} for over-voltage blanking time (OV_{BLNK}, 1.3 µs typical), the input over-voltage protection is triggered. In case of input over-voltage protection is triggered, the fault mode is activated, stopping the switching, discharging the $\overline{DIS/FLT}$ pin and disabling the UCC25800-Q1. Before restarting from an OVP fault, the input voltage should be below the OVP recovery threshold OV_{RS}. For the non-latched fault response option, the UCC25800-Q1 attempts to restart after 100 ms as described in Section 12.4.5.

The over-voltage protection threshold is a fixed value and can't be programmed.

12.3.5.3 Over-Temperature Protection (TSD)

Over-temperature protection is required, primarily to stop the internal MOSFETs from failing in either high ambient temperature operation conditions or due to self-heating from high switching current. Over Temperature occurs when the junction temperature goes above the TSD threshold of 160°C (typical). In case of over temperature, the fault mode is activated, stopping the switching, discharging the $\overline{DIS/FLT}$ pin and disabling the UCC25800-Q1. Before restarting from a TSD fault, the junction temperature should be below the over-temperature protection recover threshold (TSD-T_{HYST}). Over-temperature protection parameters are ensured by design.

12.3.5.4 Pin-Fault Protections

Table 12-2 below shows the UCC25800-Q1 response to open and short circuits on the pins of the UCC25800-Q1. For example, the SYNC function operates on the rising edge of the SYNC pin. Hence if the pin is open or short the only impact is the loss of synchronization functionality. The UCC25800-Q1 continues to operate as normal at the switching frequency programmed by the RT pin. The "✖" indicates that the UCC25800-Q1 will or may become damaged. The "-" indicates no effect on the circuit operation. "Indeterminate" means the IC behavior is unpredictable.

Table 12-2. Pin Open and Short Response

Pin	Open	Short to GND
SYNC	Normal operation with the programmed frequency	Normal operation with the programmed frequency
$\overline{DIS/FLT}$	ON	OFF
VREG	OFF (VREG open)	OFF
OC/DT	Fault (OC/DT open)	Fault (OC/DT short)
RT	f_{SW}= 1.2 MHz	Fault (RT short)
GND	Unknown	-
SW	V_{out} = 0	Fault (OCP) / ✖

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Table 12-2. Pin Open and Short Response (continued)

Pin	Open	Short to GND
VCC	OFF	OFF

Table 12-3. Pin To Pin Shorts Responses

	SYNC	$\overline{\text{DIS/FLT}}$	VREG	OC/DT	VCC	SW	GND	RT
SYNC	-							
$\overline{\text{DIS/FLT}}$	- / OFF	-						
VREG	No SYNC	Always enabled	-					
OC/DT	- / OC/DT Fault	Indeterminate	Fault (OC/ DT_OPEN)	-				
VCC	✖	✖	✖	✖	-			
SW	✖	OCP Fault / ✖	✖	Fault / ✖	Fault / ✖	-		
GND	No SYNC	OFF	OFF	Fault (OC/ DT_SHORT)	IC not biased	Fault (OCP)/ ✖	-	
RT	Indeterminate	Indeterminate	Fault (RT_OPEN)	Indeterminate	✖	✖	Fault (RT_SHORT)	-

12.3.5.5 VREG Pin Protection

VREG pin is an internal linear regulator output and the bias pin for most of the internal circuits. It is important to ensure a good regulated voltage on VREG pin. A low ESL decoupling capacitor is recommended between VREG to GND. The layout should follow the Layout Guidelines.

VREG pin is equipped with two sets of protection functions to prevent the pin from being left open or over loaded from external circuit.

When VREG pin is left open, since there is no decoupling capacitor, the internal linear regulator becomes unstable. UCC25800-Q1 recognizes this condition, stops the operation, shuts down the internal linear regulator, and enters the latch-off mode. VCC needs to be recycled to clear this protection. This behavior is the same for the fault auto-recovery version (UCC25800A-Q1) and the fault latched version (UCC25800L-Q1).

To prevent VREG pin from being over-loaded, the VREG pin has its own over-current protection. During start-up, when VREG pin voltage starts to rise, before it reaches $VREG_{OK}$, the VREG pin current is limited to 45 mA. Once its voltage crosses $VREG_{OK}$, the VREG pin current limit changes to a 25-mA . During the normal operation, if the VREG pin is over loaded and its voltage drops below $VREG_{low}$ threshold, the UCC25800-Q1 shuts down the linear regulator and enters latch-off mode. VCC needs to be recycled to clear this protection. This behavior is the same for the fault auto-recovery version (UCC25800A-Q1) and the fault latched version (UCC25800L-Q1).

12.3.6 $\overline{\text{DIS/FLT}}$ Pin operation

The $\overline{\text{DIS/FLT}}$ pin is an Input/Output from the UCC25800-Q1. It can be

- Externally driven to enable or disable the UCC25800-Q1
- Read as a status flag telling whether the UCC25800-Q1 is in fault mode or not and specifically what fault it is
- Left floating to enable the UCC25800-Q1 by default.

Internally the pin is tied high through a 100-kΩ pull-up resistor from VREG. This pull-up is only activated after the VREG pin is high. If the UCC25800-Q1 enters the fault mode, the $\overline{\text{DIS/FLT}}$ pin is pulled low internally via a 750-µA current source. When the pin is low, switching is inhibited.

The $\overline{\text{DIS/FLT}}$ internal pull-down current source is activated during the power-up sequence once the VCC voltage exceeds the UVLO rising threshold. Once the VREG voltage has risen above the $VREG_{OK}$ threshold, the pull-down current source is released and the $\overline{\text{DIS/FLT}}$ pin rises (unless it is externally pulled down). Once the $\overline{\text{DIS/FLT}}$ pin voltage exceeds the EN_{TH} threshold, the UCC25800-Q1 is enabled. When $\overline{\text{DIS/FLT}}$ pin falls below the DIS_{TH} the UCC25800-Q1 is disabled. When the UCC25800-Q1 is disabled its power consumption is reduced to $IVCC_{DIS}$.

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If there is concern about noise coupling to the $\overline{\text{DIS/FLT}}$ pin it can be pulled up with an external resistor to an external rail or to VREG. In order to read the pin as a status flag any external resistor value must be high enough that the 750-µA current source can pull the pin below the threshold level of the device reading the pin. It is recommended that the minimum external pull-up to 5 V is 10 kΩ and to 3.3 V is 4.7 kΩ if the pin is to be read as a fault output.

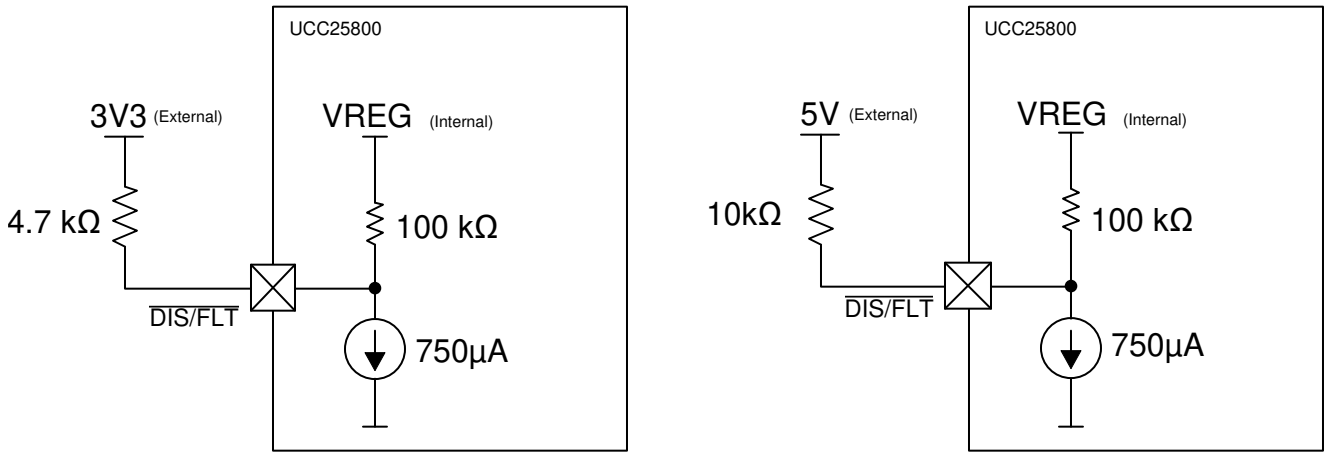

Figure 12-14. $\overline{\text{DIS/FLT}}$ pin external pull-up

If the $\overline{\text{DIS/FLT}}$ pin functionality is not required it can be left floating or tied to VREG and the UCC25800-Q1 will operate normally.

12.3.6.1 FAULT Codes

When the UCC25800-Q1 enters fault mode, it outputs a train of pulses to indicate which faults have occurred through the $\overline{\text{DIS/FLT}}$ pin. The pulse train consists of a number 50% duty cycle pulses at 50 kHz, (i.e. 10-µs wide pulses), where the number of pulses indicates the fault listed in Table 12-4. The pulse train is created through controlling the internal 750-µA pull-down current source, together with the 100-kΩ pull-up resistor.

Table 12-4. Fault codes

Number of Pulses	Fault
1	OCP1
2	OCP2
3	Input over-voltage protection
4	Over temperature protection
5	DT out of range
6	OC/DT open
7	OC/DT short
8	RT short

The pulse train is output 10 µs after the fault has been asserted. Transmission of the fault code begins with a 100-µs wide high pulse. If more than one fault is detected, the codes are transmitted successively based on the order in Table 12-4, as shown below in Figure 12-15.

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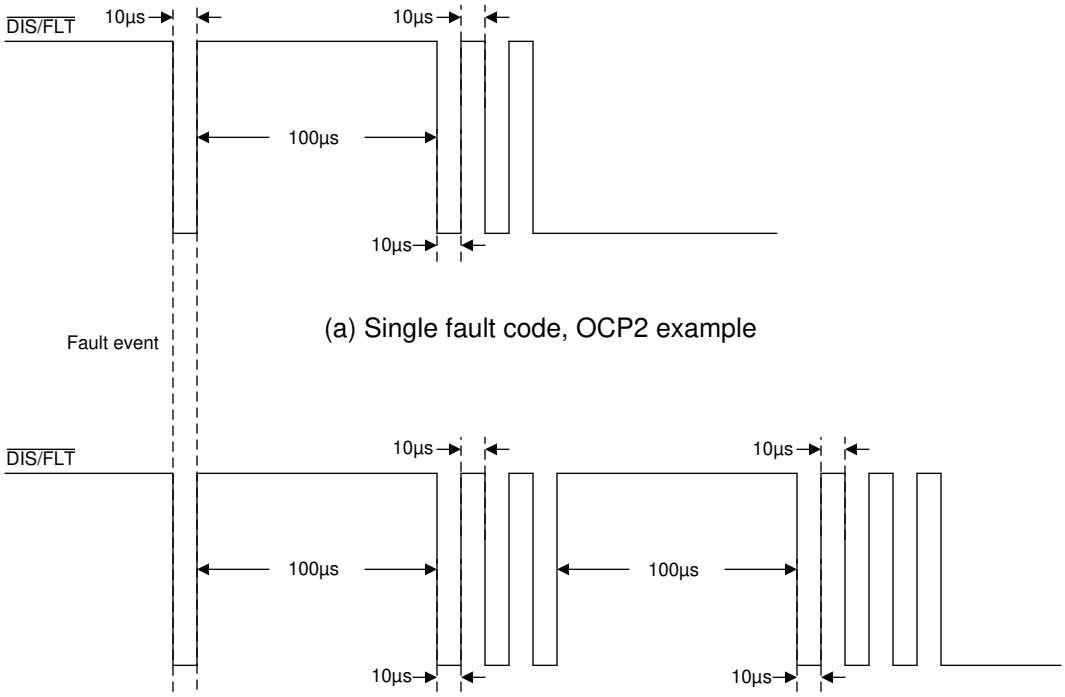

(a) Single fault code, OCP2 example

(b) Multiple fault codes, OCP2 and input over-voltage example

Figure 12-15. Fault code diagram

12.4 Device Functional Modes

Depending on the operating condition, the UCC25800-Q1 can operate in different modes, including UVLO, soft-start, normal operation, disabled and the fault modes.

12.4.1 UVLO Mode

When the input voltage on VCC is less than the UCC25800-Q1 UVLO threshold, the UCC25800-Q1 is disabled. There is no switching on the SW pin.

12.4.2 Soft-start Mode

After the VCC voltage is above the UVLO threshold, all the faults are cleared, and $\overline{\text{DIS/FLT}}$ is released, the converter operates in the soft-start mode. During the soft-start, the switching frequency gradually decreased to reduce the current stress. The soft-start mode duration is 1.5 ms. The UCC25800-Q1 always operates in soft-start mode during startup or after fault recovery. Refer to Section 12.3.2 for the details of soft-start.

12.4.3 Normal Operation Mode

Most of the cases, UCC25800-Q1 operates in the normal operation mode. The switching frequency is fixed, either determined by the RT pin voltage or external synchronization signal.

12.4.4 Disabled Mode

When the $\overline{\text{DIS/FLT}}$ pin is pulled low externally, the UCC25800-Q1 enters the disabled mode. In this mode, the VREG pin is regulated while the SW pin remains off. The VCC current consumption is reduced to the disable current $IVCC_{DIS}$.

12.4.5 Fault Modes

Occasionally, different fault conditions happen and UCC25800-Q1 protects the system from more severe damage by entering the fault modes.

UCC25800-Q1 fault modes are:

- Over current (OCP1 and OCP2)
- Over temperature (TSD)
- Input over-voltage
- OC/DT open
- OC/DT short
- RT short

OCP1 occurs when the resonant current during the internal low side MOSFET on time exceeds I_{OCP} for 2 ms. OCP2 occurs when the current in either MOSFET exceeds 5 times of the I_{OCP} for more than 100 ns.

Over temperature protection (TSD) occurs when the junction temperature goes above TSD threshold.

Input over-voltage protection occurs when VCC voltage goes above over-voltage shut-down (OV_{SD}) threshold for more than 1.3 µs.

OC/DT open protection occurs if the OC/DT pin exceeds 4.5 V after the OCP check has been completed.

OC/DT short protection occurs if the OC/DT pin falls below 500 mV.

RT short protection occurs when RT pin is below 150 mV.

When any fault occurs the switching is immediately (after individual detection delays) stopped. The $\overline{\text{DIS/FLT}}$ pin is internally pulled down and when it crosses the disable threshold DIS_{TH} and the UCC25800-Q1 current consumption is reduced to $IVCC_{DIS}$. The VREG regulator remains enabled and the RT pin remains at its programmed level.

When the UCC25800-Q1 enters fault mode it pulses the pull-down current on the $\overline{\text{DIS/FLT}}$ pin on and off to output a fault code and signal which fault has been triggered as explained in Section 12.3.6.1.

For the fault auto recovery version, after a delay time of 100 ms, the $\overline{\text{DIS/FLT}}$ pin is released and, if it is not pulled low externally. When it crosses the EN_{TH}, the UCC25800-Q1 is enabled, the power up sequence occurs and the switching can start again. Before starting switching, the faults are checked again. If the protection that caused the fault condition is still present, the switching is not started and a new fault condition is asserted, fault codes are transmitted again. After that, the $\overline{\text{DIS/FLT}}$ pin is again discharged and UCC25800-Q1 current consumption is again reduced to $IVCC_{DIS}$. This fault and power-up sequence is automatically cycled until all the faults are cleared.

For the latched fault recovery version, the UCC25800-Q1 remains in fault mode indefinitely unless the latch is cleared. The latch can be cleared by pulling the $\overline{\text{DIS/FLT}}$ pin high (after it has been pulled low (below DIS_{TH})) for longer than 2 µs and then pulled low for longer than 6 µs. After that, when the $\overline{\text{DIS/FLT}}$ pin voltage crosses the EN_{TH} threshold, the UCC25800-Q1 is enabled. The power up sequence occurs and the switching can start again. Also in this version the faults are checked before starting switching and if they are not all cleared (see above) the switching is not enabled and a new latched fault condition occurs. The fault codes for any faults which have not been cleared are transmitted. Again, to exit from this latched fault condition and try a new restart, the $\overline{\text{DIS/FLT}}$ pin has to be toggled. The latch can also be cleared by power cycling the UCC25800-Q1, which clears all the faults and commences the start-up sequence once the VCC exceeds the UVLO rising threshold again.

Table 12-5 below shows the sequence for the latching and non-latching variants depending on the configuration of the $\overline{\text{DIS/FLT}}$ pin.

Table 12-5. Fault mode behavior for latched and auto-recovery fault response parts

$\overline{\text{DIS/FLT}}$ Pin	Auto-recovery fault response	Latched fault response
Tied High	Fault mode triggered. Fault code output pull down enabled. UCC25800-Q1 auto restarts after 100 ms	Fault mode triggered. Fault code output pull down enabled. Power is cycled to restart
Open	Fault mode triggered. Fault code output pull down enabled. UCC25800-Q1 auto restarts after 100 ms.	Fault mode triggered. Fault code output pull down enabled. Power cycled to restart
Driven externally	Fault mode triggered Fault code output pull down enabled. UCC25800-Q1 auto restarts after 100 ms if pin is not pulled low externally.	Fault mode triggered. Fault code output pull down enabled. Pin toggled or power cycled to restart. OCP1 has a minimum 100-ms restart time.

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13 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

13.1 Application Information

The isolated bias supply is required in many applications, such as the gate driver bias for the traction inverters, on board chargers in electrical vehicles. It is also used in other sensing and control circuits in the electrical vehicles to minimize the noise or provide safety isolation. The UCC25800-Q1 based open-loop LLC converter provides a reliable solution for these applications. It uses the open-loop control to improve the noise immunity. The LLC topology is able to operate at a higher switching frequency with soft switching, achieve high efficiency and low EMI, reducing the transformer size. Furthermore, the LLC topology is able to absorb the transformer leakage inductance as part of the resonant circuit. This allows the transformer to have extremely low primary side to secondary side parasitic capacitance, which reduces the system level common-mode noise. Besides, this also helps to simplify the transformer construction and reduces the transformer cost.

13.2 Typical Application

In the automotive traction inverters or on-board chargers, a regulated bus voltage is often generated from the 12-V battery and then processed by the isolated bias supplies to provide the gate driver bias power for the inverter switches, as shown in Figure 13-1. The isolated bias supply can be used to bias the high-side switches or low-side switches, to provide the isolation for function, safety, or noise immunity.

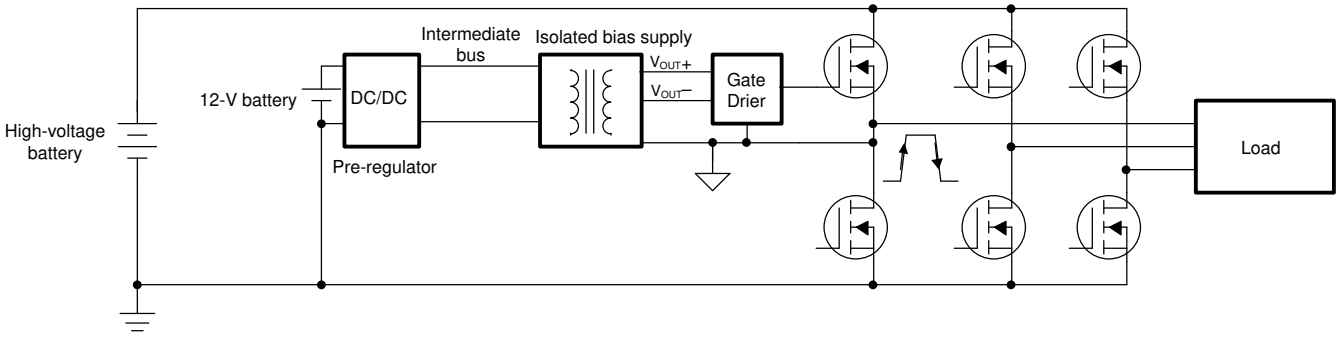

Figure 13-1. Gate driver bias supply example for automotive traction inverter

When the isolated based bias supply used in the inverter applications, especially for the high side switches, the high dv/dt on the inverter switch-node can couple through the bias supply transformer and causes extra EMI noise, as demonstrated in Figure 13-2.

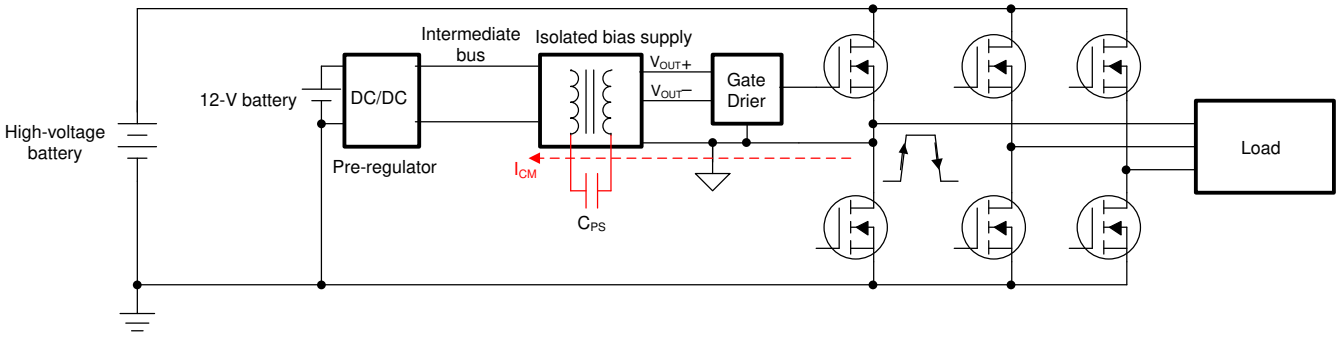

Figure 13-2. Noise coupling path from inverter power stage to isolated bias supply

Given the high dv/dt is caused by the inverter power stage, to minimize this noise coupling, it is desired to minimize the transformer primary side to secondary side parasitic capacitor (inter-winding capacitor) C_{PS}. Popular topologies, such as Flyback or Push-pull, require the minimum leakage inductance to improve the efficiency, reduce the voltage and current stress, as well as minimize the noise created by the converter. In turn, this type of transformers suffers from larger inter-winding capacitance. When they are used in the gate driver bias supply applications, the high dv/dt from the inverter power stage could be coupled through the transformer inter-winding capacitance to the low voltage side. This creates a much severe EMI noise issue. Instead, the LLC topology utilizes the transformer leakage inductance as its resonant component, allowing the converter to use a transformer with larger leakage inductance but much smaller inter-winding capacitance. This results in less system EMI noise challenges.

13.2.1 LLC Converter Operation Principle

Different than the traditional PWM converters, LLC converters adjust the output voltage through varying the switching frequency. It is often called a PFM (Pulse Frequency Modulation) converter. As shown in Figure 13-3, the LLC has three resonant elements, the resonant inductor (L_r), the magnetizing inductor (L_m), and the resonant capacitor (C_r). In the isolated bias supply design, the transformer leakage inductance, and the magnetizing inductor can be used as part of the resonant circuit. The only external resonant component would be the resonant capacitor.

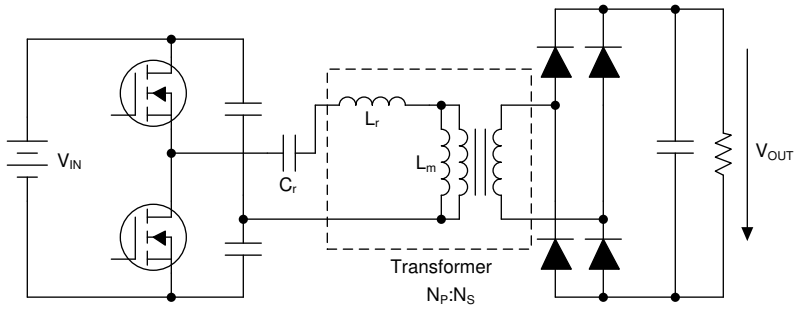

Figure 13-3. LLC Converter

At the resonant switching frequency (series resonant frequency of L_r and C_r), the impedance of the resonant tank (L_r and C_r) is equal to zero. The input and output voltage are virtually connected together through the transformer. Therefore, the gain of the converter is equal to the transformer turns ratio, as shown in Equation 5.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{2}\frac{N_S}{N_P} \tag{5}$$

In this equation, the ½ comes from the half-bridge architecture that the transformer primary side only sees half of the input voltage.

UCC25800-Q1 controls the LLC converter operates at a fixed switching frequency very close to the resonant frequency, to create an output voltage proportional to the input voltage, through a transformer turns-ratio. Depending on the location of the resonant capacitor, the LLC converter can be configured as primary-side resonant (as shown in Figure 13-3), or secondary-side resonant (as shown in Figure 13-4). Once the resonant capacitor is moved to the secondary side, the magnetizing inductor no longer affects the converter gain. Therefore, the converter is less sensitive to the switching frequency and resonant component tolerances. The secondary-side resonant is more suitable for the open-loop LLC converter and it is a preferred configuration for UCC25800-Q1.

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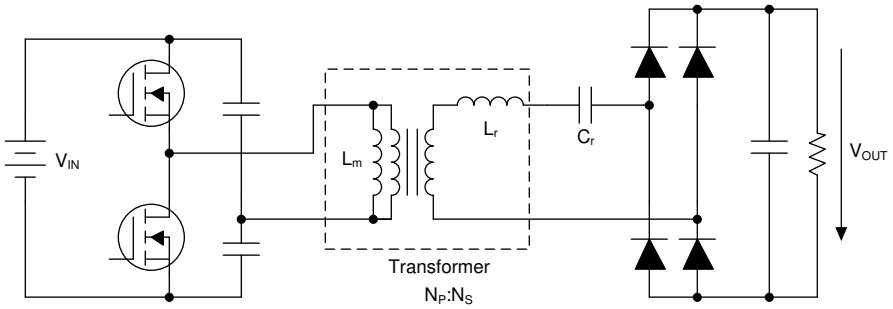


Figure 13-4. Secondary side resonant LLC converter

Furthermore, the secondary-side full-wave rectifier can be replaced with a voltage-doubler rectifier. Together with splitting the resonant capacitor into two, as shown in Figure 13-5, the converter configuration becomes simpler and fewer diodes are used. In this case, the transformer primary side sees half of the input voltage and the transformer secondary side sees half of the output voltage. The converter voltage gain becomes purely the transformer turns-ratio, as shown in Equation 6.

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \tag{6}$$

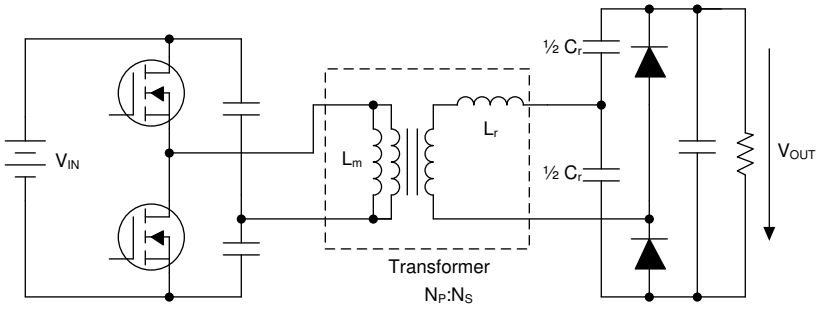
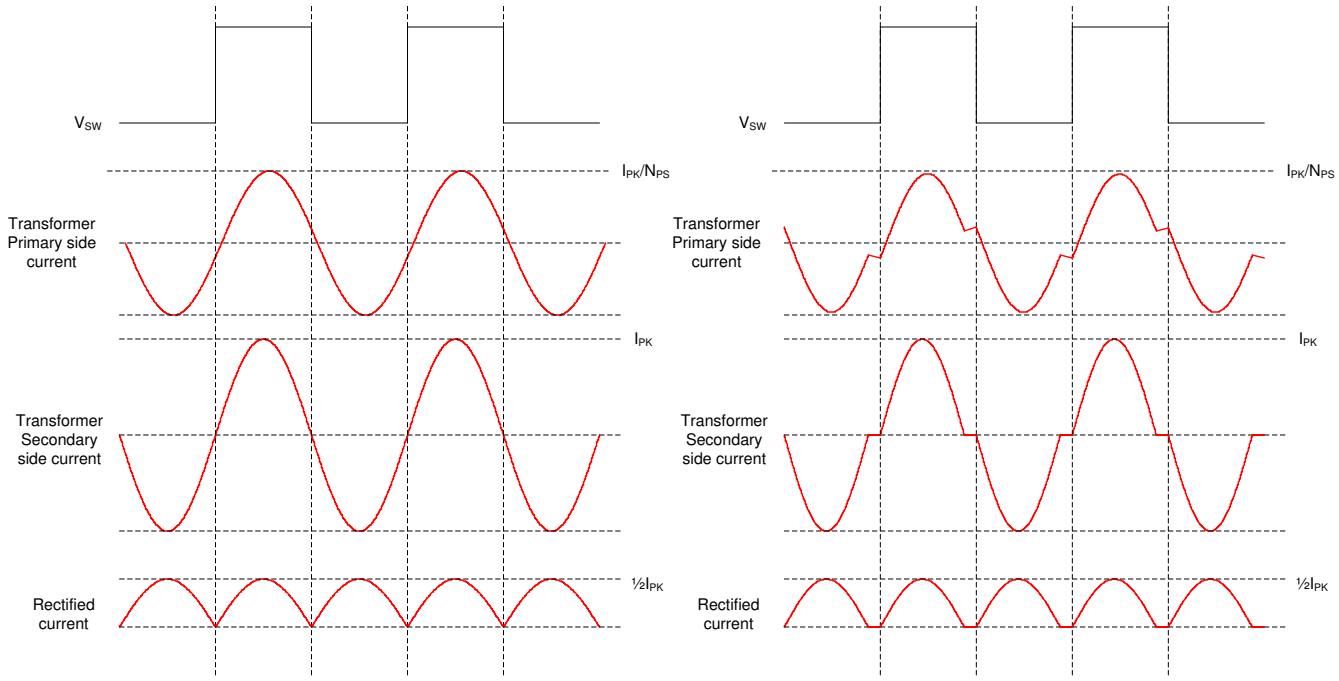


Figure 13-5. Secondary side resonant LLC converter with voltage doubler rectifier

The LLC operation waveforms are shown in Figure 13-6, when switching frequency is equal to the resonant frequency or below the resonant frequency.

ADVANCE INFORMATION



(a) Switching frequency equal to resonant frequency (b) Switching frequency below resonant frequency

Figure 13-6. LLC converter operation waveforms

13.2.2 Design Requirements

A 2-W traction inverter gate driver bias supply is used to demonstrate the design process based on UCC25800-Q1.

Table 13-1. Electrical Performance Specifications

Parameter	Test Conditions	Min	Nom	Max	Unit
Input Characteristics					
V_{IN}, Input voltage, DC			15		V
Output Characteristics					
V_{OUT1}, set point, DC		17.93	18.10	18.27	V
I_{OUT1}, output current range		0		85	mA
V_{OUT1}, regulation	I_{OUT1} = I_{OUT2}, 0 to full load	-1.0		1.0	%
V_{OUT2}, set point		-5.02	-4.98	-4.94	V
I_{OUT1}, output current range		-85		0	mA
V_{OUT2}, regulation	I_{OUT1} = I_{OUT2}, 0 to full load	-1.0		1.0	%
V_{OUT1}, peak to peak ripple	I_{OUT1} = I_{OUT2}, full load		50		mV
V_{OUT2}, peak to peak ripple	I_{OUT1} = I_{OUT2}, full load		35		mV
System Characteristics					
f_{SW}, switching frequency	Normal operation		500		kHz
I_{OC}, Over current limit			100		mA

13.2.3 Detailed Design Procedure

The design of UCC25800-Q1 based isolated bias supply involves both the power-stage design and the controller parameters design.

The power-stage design involves the selection of the transformer and the resonant capacitors.

ADVANCE INFORMATION

Step 1: Transformer turns-ratio selection

Given the UCC25800-Q1 based isolated bias supply operates with open-loop control, the voltage accuracy is not able to get down to 1%. The post regulators, such as a linear regulator can be used to achieve 1% regulation accuracy. Therefore, when design the LLC converter output voltage, the headroom for the post regulator stage needs to be considered.

At the resonant frequency, together with the voltage doubler output, the LLC converter voltage gain is equal to the transformer turns-ratio. Therefore, the transformer turns-ratio can be calculated as:

$$N_P:N_S=N_{PS}=\frac{V_{IN}}{V_{OUT1}+V_{OUT2}+2V_F+V_{headroom}}=\frac{15V}{18V+5V+2\times0.5V+1V}=\frac{15V}{25V}=0.6 \quad (7)$$

Where:

- V_F is the output diode forward voltage drop
- $V_{headroom}$ is the extra headroom needed for the post regulator

Step 2: Calculate transformer volt-second rating

The transformer volt-second rating on the primary side can be calculated as:

$$VS=\frac{V_{IN}}{2}\frac{1}{4f_{SW}}=\frac{15V}{2}\times\frac{1}{4\times500kHz}=3.75V\cdot\mu s \quad (8)$$

Step 3: Calculate the transformer currents

The transformer sees highest RMS current right before over current protection. According to Figure 13-6, the output current is equal to the average current of the secondary-side rectified current. When load current is at the over current protection level of 100 mA, the primary side current can be calculated. The transformer primary-side and secondary-side peak and RMS current can be calculated based on Equation 9 through Equation 12.

$$I_{rms_S}=\frac{\pi}{\sqrt{2}}I_{OC}=\frac{\pi}{\sqrt{2}}\times100mA=222mA \quad (9)$$

$$I_{pk_S}=\sqrt{2}I_{rms_S}=314mA \quad (10)$$

$$I_{rms_P}=\frac{I_{rms_S}}{N_{PS}}=\frac{222mA}{0.6}=370mA \quad (11)$$

$$I_{pk_P}=\frac{I_{pk_S}}{N_{PS}}=\frac{314mA}{0.6}=523mA \quad (12)$$

From step 1 through 3, the key transformer information can be summarized in Table 13-2. It can be used to share with transformer vender to get the transformer designed and manufactured. It is recommended to leave some design margins (30%~50%) to consider the tolerance of the components.

Table 13-2. Transformer parameter summary

Parameter Name	Value	Unit
Primary side to secondary side turns ratio	0.6	
Primary side volt-second	3.75	Vμs
Primary side peak current	523	mA
Primary side RMS current	370	mA
Secondary side peak current	314	mA
Secondary side RMS current	222	mA

To minimize the transformer inter-winding capacitance, the split chamber bobbin is recommended, as shown in Figure 13-7.

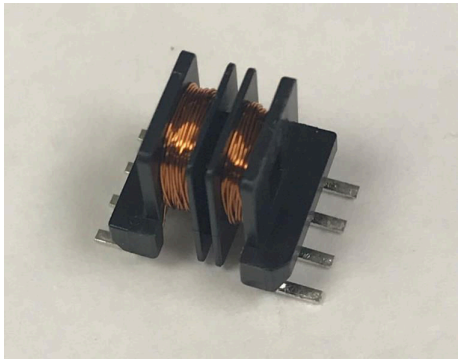


Figure 13-7. Split chamber bobbin

Another key transformer parameter is the magnetizing inductance. When using the core without the air gap, if the transformer magnetizing inductance is more than 20 times higher than the leakage inductance, the air gap is not needed. Otherwise, a minimum air gap is recommended without causing extra manufacture cost.

Based on the calculation results, Wurth transformer 750319177 is selected to be the transformer. It has a turns ratio of N_{PS} = 1:1.67, which is 0.6. The magnetizing inductance measured from primary side is 16.5 µH and the leakage inductance measured from primary side is 0.75 µH. Given the secondary-side resonant is used, the leakage inductance should be measured from secondary side, with primary side shorted, at the resonant frequency. The secondary-side leakage inductance is measured as 1.4 µH.

Step 4: Select resonant capacitor

The resonant capacitor selection is based on the resonant frequency. Choose the resonant tank resonant frequency 10~15% above the switching frequency.

$$C_r = \frac{1}{4\pi^2 L_r f_r^2} = \frac{1}{4\pi^2 L_r (1.1 f_{sw})^2} = 60nF \quad (13)$$

When using the voltage double rectifier, each resonant capacitor value should be half of this value. Therefore, a 22-nF resonant capacitor can be used on each of the resonant capacitor.

Step 5: Choose output capacitor

The output capacitor selection is based on the output voltage ripple requirement. The output capacitor can be calculated based on Equation 14. Choose the output capacitor according to the ripple requirement and the gate driver requirement. Design the capacitor based on half of the ripple amplitude so that there is margin for the voltage ripple caused by the capacitor ESR. A 10-µF capacitor can be used in this case. It should be noticed that the ceramic capacitor loses its capacitance when the voltage is applied.

$$C_{out} > \frac{I_{OUT} \times 0.421}{4 V_{ripple} f_{SW}} = \frac{85mA \times 0.421}{4 \times 50mV \times 500kHz} = 0.358\mu F \quad (14)$$

Step 6: Choose primary side DC blocking capacitor

The primary-side half-bridge DC blocking capacitors need to be much larger than the resonant capacitor. Given the high-switching frequency design, low ESR X7R capacitors with value between 1 µF and 10 µF are recommended.

Once the power stage is set up, the programming pins of the IC can be set up accordingly. Given the minimum external components, setting up the UCC25800-Q1 is extremely easy.

Step 7: Setting up RT pin resistor

ADVANCE INFORMATION

To set the switching frequency to 500 kHz, according to the description in Oscillator, the RT pin resistor can be calculated as:

$$R_{RT}=f_{SW}\times\frac{\Omega}{10Hz}=500kHz\times\frac{\Omega}{10Hz}=50k\Omega \quad (15)$$

Given 50 kΩ is not a standard resistor value, we can choose R_{RT} value to be 49.9 kΩ.

Step 8: Setting up OC/DT pin resistor divider

The OC/DT pin is a multi-function pin. It sets up the maximum dead-time for the adaptive dead-time, and set up the OCP levels for over current protection.

For the dead-time setting, we generally choose 5~10% of the switching cycle, as the maximum dead-time. This value can be further adjusted according to the measurement result, depending on the soft switching conditions. According to Equation 3, the voltage on DT/CT pin should be:

$$V_{OC/DT}=\frac{150ns\cdot V}{DT_{MAX}}+0.9V=\frac{150ns\cdot V}{\frac{0.05}{500kHz}}+0.9V=2.4V \quad (16)$$

The OCP setting is determined by the primary-side peak current. In Equation 12, the primary-side peak current is calculated as 523 mA. Leaving extra 30% margin, the OCP1 level should be roughly 680 mA. OCP1_4 can be used as the OCP1 setting.

According to Table 12-1, the Thevenin resistance should be between 7.95 kΩ and 8.25 kΩ. We can use the value in the middle to set up the resistor and verify the Thevenin resistance after the resistor values are calculated,

The pull-up resistor can be calculated as

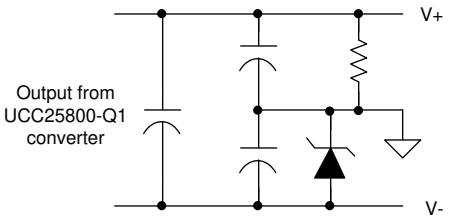
$$R_a=\frac{R_{th}V_{REG}}{V_{OC/DT}}=\frac{8.1k\Omega\times5V}{2.4V}=16.875k\Omega\approx16.9k\Omega \quad (17)$$

And the pull-down resistor can be calculated as

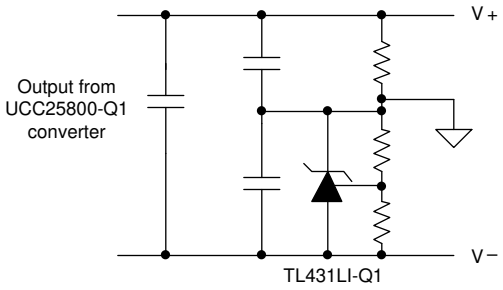
$$R_b=\frac{R_{th}V_{REG}}{V_{REG}-V_{OC/DT}}=\frac{8.1k\Omega\times5V}{5V-2.4V}=15.58k\Omega\approx15.4k\Omega \quad (18)$$

It can be seen, due to the limited standard resistor value, the selected resistor values are different than the calculated resistor values. The Thevenin resistance needs to be checked. In this case, the Thevenin resistance is 8.058 kΩ and it is within the OCP1_4 setting range.

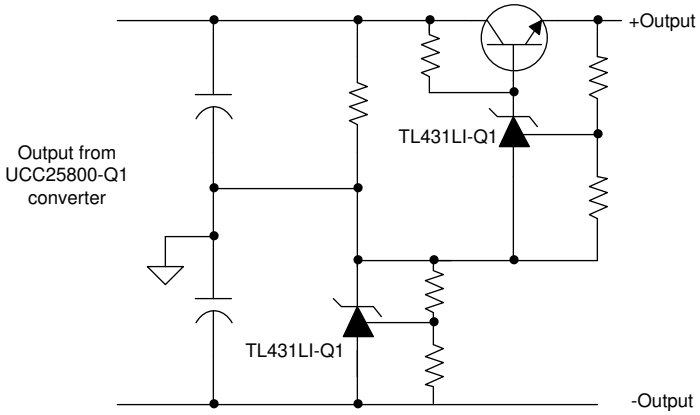
The UCC25800-Q1 based LLC converter can output a single output. It needs some help to split it into the dual outputs needed for the final designs. Depending on the regulation accuracy requirement, the splitting can be done using a simple Zener diode, a shunt-regulator, or even with a linear regulator, as demonstrated in Figure 13-8.



(a) Split the output voltage using Zener diode



(b) Split the output voltage using shunt-regulator



(c) splitting the output voltage using shunt-regulator and linear regulator

Figure 13-8. Different ways of splitting single output voltage to positive and negative outputs

Using the Zener diode, the negative rail voltage is determined by the Zener voltage and the rest of the output voltage becomes the positive rail. Due to the tolerance of the Zener diode, a shunt-regulator can be used to improve the negative rail voltage accuracy. Furthermore, a linear regulator can be added to improve the positive rail voltage accuracy as well. The designer can choose the right solution based on the performance and cost tradeoffs.

In this design, the shunt-regulator and linear-regulator are used to get 1% accuracy required for the positive and negative rail. ATL431-Q1 is used as the shunt-regulator and the voltage reference for the linear regulator. Given the reference voltage of ATL431-Q1 is 5 V, to create 5-V shunt-regulator voltage, a 1 kΩ and 1 kΩ voltage divider can be used to set up the 5-V regulation voltage. On the positive rail side, to create 18-V output voltage, 6.34 kΩ and 1 kΩ can be used to set up the output voltage divider ((6.34+1)×2.5=18.35V).

With all the calculated circuit parameters, the design schematic is shown in Figure 13-9.

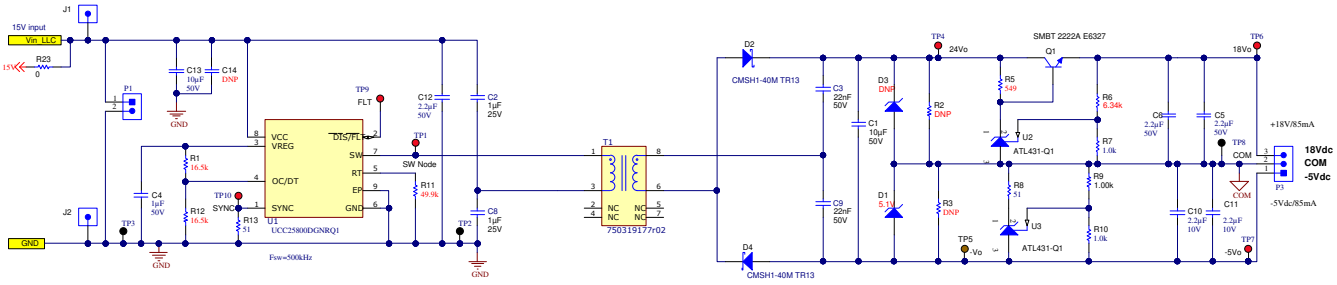


Figure 13-9. Circuit schematic for the designed isolated bias supply

13.2.4 Application Curves

Figure 13-10. LLC output voltage load regulation

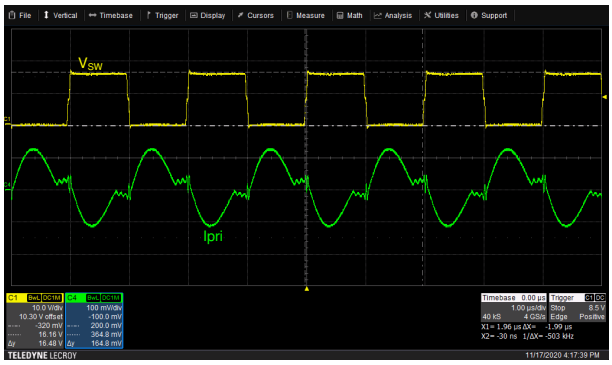


Figure 13-11. Switch-node Voltage (yellow) and Current (Primary side, 0.2V/A) at Full Load

13.3 What to Do and What Not to Do

Do

- Good decoupling between VCC and GND, minimize the loop of VCC-GND and the decoupling capacitor
- Use transformer with split chamber bobbin to minimize the EMI noise coupling from the inverter power stage
- UCC25800-Q1 can be used to drive single higher power transformer or multiple lower power transformer
- Setting the OCP1 level according to the designed load
- Use post regulator if the voltage regulation requirement can't be met
- Add Zener clamp at output if the output load can be completely removed
- If cost is acceptable, use NP0 or C0G type resonant capacitor, or use X7R with much higher voltage rating than needed
- Sufficient copper area for thermal management if the ambient temperature is high or the power level is high

Not to Do

- Long VCC-GND decoupling capacitor trace
- Set up the OCP1 to the highest level for all designs

ADVANCE INFORMATION

14 Power Supply Recommendations

The UCC25800-Q1 drives an LLC converter with constant switching frequency to make the LLC converter operate near its resonator frequency. When LLC converter operates at its resonant frequency, the impedance of the resonant tank is equal to zero. The input and output voltage is virtually connected together, through the transformer turns-ratio. Given the LLC converter is a half-bridge converter, the transformer primary side only sees half of the input voltage. If the secondary side uses voltage double rectifier, it also only sees half of the output voltage. The relationship between the input and output voltage is simply the transformer turns-ratio. Given that, to achieve a fixed output voltage, the input voltage needs to be fixed. Even though the UCC25800-Q1 is recommended to operate with an input voltage source between 9 V and 34 V, it is meant to be one fixed voltage within this voltage range. Given the relationship between input and output voltages is simply the transformer turns-ratio, the accuracy of the input would impact the accuracy of the output. There is no requirement from the UCC25800-Q1, while the input voltage accuracy is demanded by the output voltage requirements.

When the input voltage is very close to the 9 V end, because it is very close to the UVLO threshold UVLO_F, sufficient input bypass capacitor is recommended to ensure the load transient won't cause the VCC voltage drops below UVLO threshold UVLO_F.

15 Layout

Given the minimum external components, UCC25800-Q1 layout is quite straight forward. The main considerations would be the power loop and the grounding.

15.1 Layout Guidelines

- The most important layout guideline is to minimize the VCC-GND-decoupling capacitor loop. This loop carries all the switching current, it is important to have a low ESL decoupling capacitor between VCC and GND, with the minimum loop. Refer to Layout Example for how to layout the bypass capacitor on VCC to GND.
- Return all control signals to GND pin through a separated plane. Avoid sharing path between the signal ground and the power ground. Use a short trace to connect GND pin to the thermal PAD.
- Separate the power stage components and signal component to minimize the coupling between these components
- Short VREG-GND-decoupling capacitor loop is recommended. A low ESL decoupling capacitor between VREG and GND is needed to ensure stable operation of the internal linear regulator.
- Decoupling capacitors can be added on RT and DT/OC pin to improve the noise immunity. Refer to Recommended Operating Conditions for recommended maximum capacitor values.
- When external synchronization is not used, it is recommended to short SYNC pin to GND.
- Other general power supply design layout guidelines such as minimize the current loop for high di/dt and minimize the copper area of the switch-node with high dv/dt.
- The secondary side of the LLC converter is often connected with the high dv/dt node in the end equipment. In these cases, is recommended to minimize the secondary-side copper area.

15.2 Layout Example

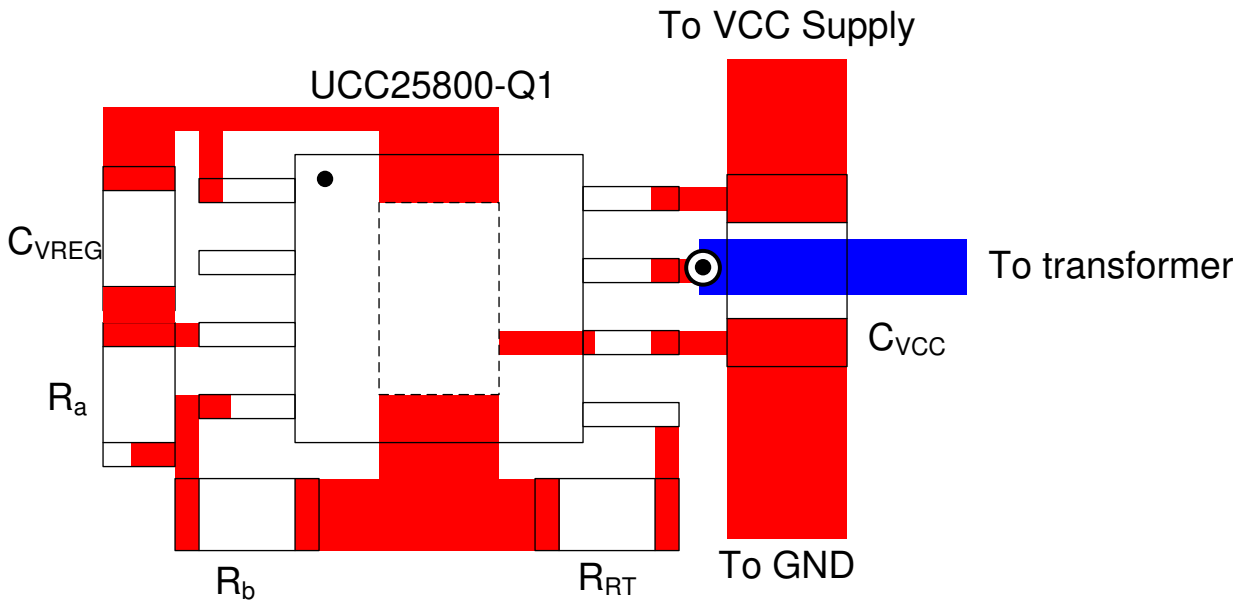


Figure 15-1. Layout example

16 Device and Documentation Support

17 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC25800ADGNQ1	ACTIVE	HVSSOP	DGN	8	80	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

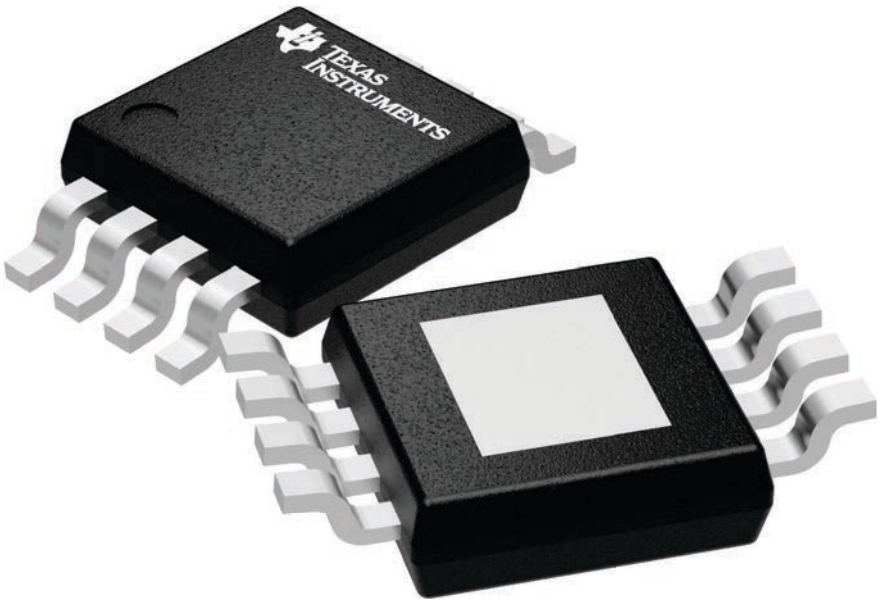
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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