TPS22950 5.5V、2.7A、34mΩ 可调限流负载开关

1 特性

- 输入电压范围 (V_{IN})：1.8V 至 5.5V
- 输出电流限制 (I_{LIMIT})：0.05A 至 3.5A（典型值）
- 热关断 (TSD)
- 导通电阻 (R_{ON})：
  - V_{IN} = 5V 时，R_{ON}：34mΩ（典型值）
  - V_{IN} = 3.3V 时，R_{ON}：41mΩ（典型值）
- 慢速开通时序可限制浪涌电流（典型值）：
  - V_{IN} = 5V 时，t_{ON}：800us
  - V_{IN} = 3.3V 时，t_{ON}：550us
- 常开的反向电流阻断 (RCB)
- 故障指示 (FLT)
- 快速输出放电 (QOD)：150Ω
- 智能 ON 引脚下拉电阻 ($R_{PD,ON}$)：
  - ON ≥ V_{IH} (I_{ON})：50nA（最大值）
  - ON ≤ V_{IL} ($R_{PD,ON}$)：500kΩ（典型值）
- 低功耗：
  - 导通状态 (I_Q)：40uA（典型值）
  - 关闭状态 (I_{SD})：0.2uA（典型值）

2 应用

- 个人电子产品
- 平板电脑
- 笔记本电脑
- 游戏机
- 附件

3 说明

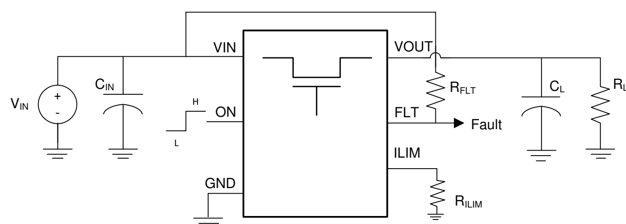
TPS22950 器件是一款小型单通道负载开关，能够通过可调输出电流限制、反向电流阻断和热关断提供强大的故障保护功能。

开关导通状态由数字输入控制，此输入可与低压控制信号直接连接。首次加电时，此器件使用智能下拉电阻来保持 ON 引脚不悬空，直到系统定序完成。故意将该引脚驱动为高电平 (>V_{IH}) 之后，便会断开智能下拉电阻，以防止不必要的功率损耗。

TPS22950 采用标准 WCSP 封装，工作环境温度范围为 –40°C 至 125°C。

器件信息

器件型号	封装	封装尺寸（标称值）
TPS22950	WCSP (6)	1.106mm × 0.706mm



典型应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2020	*	Initial release.

5 Pin Configuration and Functions

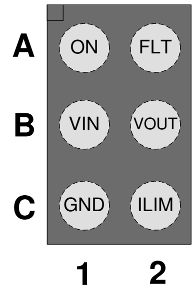


图 5-1. TPS22950 WCSP - 6 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ON	A1	I	Active high switch control input. Do not leave floating.
FLT	A2	O	Open-drain output, pulled low during thermal shutdown or reverse current-conditions.
VIN	B1	I	Switch Input.
VOUT	B2	O	Switch Output.
GND	C1	-	Device ground.
ILIM	C2	O	Adjusts device current limit through a resistor to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	–0.3	6	V
V_{OUT}	Maximum Output Voltage Range	–0.3	6	V
V_{ON}	Maximum ON Pin Voltage Range	–0.3	6	V
V_{FLT}	Maximum FLT Pin Voltage	–0.3	6	V
I_{MAX}	Maximum Continuous Output Current		2.7	A
$I_{MAX,PLS}$	Maximum Pulsed Output Current (T_J = 85°C, duty cycle = 2%)		4.1	A
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	1.8		5.5	V
V_{OUT}	Output Voltage Range	0		5.5	V
V_{IH}	ON Pin High Voltage Range	1		5.5	V
V_{IL}	ON Pin Low Voltage Range	0		0.35	V
I_{LIM}	Output Current Limit	0.05		3.5	A
T_A	Ambient temperature	–40		125	°C
TJ	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS22950	UNIT
		YBH (WCSP)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	1.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[(1)]		TPS22950 YBH (WCSP) 6 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	39.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Unless otherwise noted, the characteristics in the following table apply across the recommended operating input voltage range with a load of C_L = 0.1 µF, R_L = 100 Ω. Typical Values are at 5V and T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Supply (VIN)							
$I_{Q, VIN}$	VIN Quiescent Current	V_{ON} ≥ V_{IH}, VOUT = Open	-40°C to 85°C		44	60	µA
			-40°C to 125°C			60	µA
$I_{SD, VIN}$	VIN Shutdown Current	V_{ON} ≤ V_{IL}, VOUT = GND	25°C		0.2	0.4	µA
			-40°C to 85°C			9	µA
			-40°C to 125°C			46	µA
ON-Resistance (RON)							
R_{ON}	ON-State Resistance	V_{IN} = 5V, I_{OUT} = -200 mA	25°C		34	41	mΩ
			-40°C to 85°C			49	mΩ
			-40°C to 125°C			54	mΩ
R_{ON}	ON-State Resistance	V_{IN} = 3.3V, I_{OUT} = -200 mA	25°C		41	51	mΩ
			-40°C to 85°C			62	
			-40°C to 125°C			68	
R_{ON}	ON-State Resistance	V_{IN} = 1.8V, I_{OUT} = -200 mA	25°C		67	90	mΩ
			-40°C to 85°C			105	mΩ
			-40°C to 125°C			116	mΩ
Output Current Limit (ILIM)							
I_{LIM}	Output Current Limit	R_{ILIM} = 610Ω V_{OUT} - V_{IN} = 0.3V	-40°C to 125°C	1.54	2	2.46	A
		R_{ILIM} = 1.15kΩ V_{OUT} - V_{IN} = 0.3V	-40°C to 125°C	0.75	1	1.25	A
		R_{ILIM} = 2.21kΩ V_{OUT} - V_{IN} = 0.3V	-40°C to 125°C	0.38	0.5	0.62	A
		R_{ILIM} = 19.2kΩ V_{OUT} - V_{IN} = 0.3V	-40°C to 125°C	0.034	0.05	0.066	A
t_{LIM}	Current Limit Response Time	Output hard short (I_{OUT} > I_{LIM})	-40°C to 125°C		5		µs
Reverse Current Blocking (RCB)							
V_{RCB}	Activation Threshold	V_{OUT} Rising; V_{OUT} > V_{IN}	-40°C to 125°C		44		mV
	Release Threshold	V_{OUT} Falling; V_{OUT} > V_{IN}	-40°C to 125°C		16		mV
t_{RCB}	Response Time	V_{OUT} = V_{IN} + 1V	-40°C to 125°C		3		µs
$I_{OUT,RCB}$	Reverse Leakage Current into VOUT	V_{ON} ≤ V_{IL} V_{IN} = 0V, V_{OUT} = 5V	-40°C to 125°C			38	µA
Fault Indication (FLT)							
$V_{OL, FLT}$	Output Low Voltage	I_{FLT} = 1 mA	-40°C to 125°C			0.1	V
$t_{D,FLT}$	Fault Delay Time	V_{ON} ≥ V_{IH}	-40°C to 125°C		10		µs
I_{FLT}	Off State Leakage	V_{ON} ≤ V_{IL}	-40°C to 125°C			50	nA

6.5 Electrical Characteristics (continued)

Unless otherwise noted, the characteristics in the following table apply across the recommended operating input voltage range with a load of C_L = 0.1 µF, R_L = 100 Ω. Typical Values are at 5V and T_A = 25°C.

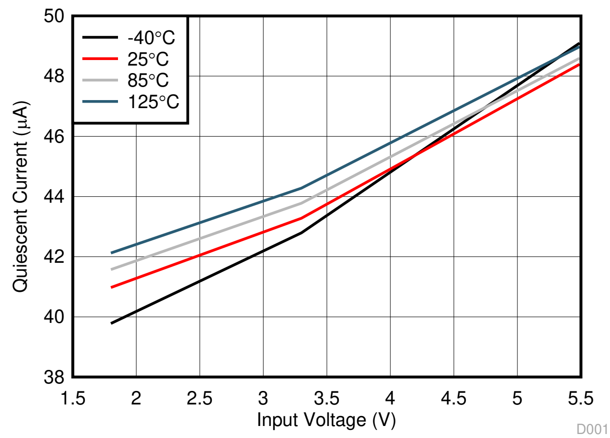
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Enable Pin (ON)							
$R_{PD, ON}$	Smart Pull Down Resistance	$V_{ON} \le V_{IL}$	-40°C to 125°C		500	650	kΩ
I_{ON}	ON Pin Leakage	$V_{ON} \ge V_{IH}$	-40°C to 125°C			50	nA
R_{QOD}	Quick Output Discharge Resistance	VIN = 5V $V_{ON} \le V_{IL}$	-40°C to 125°C		100	160	Ω
R_{QOD}	Quick Output Discharge Resistance	VIN = 3.3V $V_{ON} \le V_{IL}$	-40°C to 125°C		150	185	Ω
R_{QOD}	Quick Output Discharge Resistance	VIN = 1.8V $V_{ON} \le V_{IL}$	-40°C to 125°C		200	355	Ω
Thermal Shutdown (TSD)							
TSD	Thermal Shutdown	Rising	N/A		170		°C
		Falling (Hysteresis)	N/A		150		°C

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies at 25°C with a load of C_L = 1 µF, R_L = 100 Ω

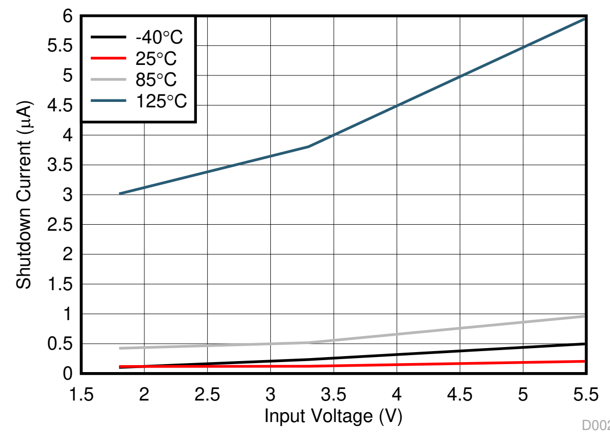
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	V_{IN} = 5V		800		µs
t_{ON}	Turn ON Time	V_{IN} = 3.3V		550		µs
t_{ON}	Turn ON Time	V_{IN} = 1.8V		400		µs
t_R	Output Rise Time	V_{IN} = 5V		600		µs
t_R	Output Rise Time	V_{IN} = 3.3V		320		µs
t_R	Output Rise Time	V_{IN} = 1.8V		200		µs
t_D	Output Delay Time	V_{IN} = 5V		260		µs
t_D	Output Delay Time	V_{IN} = 3.3V		250		µs
t_D	Output Delay Time	V_{IN} = 1.8V		260		µs
t_{OFF}	Turn OFF Time	V_{IN} = 5V		20		µs
t_{OFF}	Turn OFF Time	V_{IN} = 3.3V		15		µs
t_{OFF}	Turn OFF Time	V_{IN} = 1.8V		17		µs
t_{FALL}	Output Fall Time	V_{IN} = 5V		118		µs
t_{FALL}	Output Fall Time	V_{IN} = 3.3V		120		µs
t_{FALL}	Output Fall Time	V_{IN} = 1.8V		130		µs

6.7 Typical Characteristics



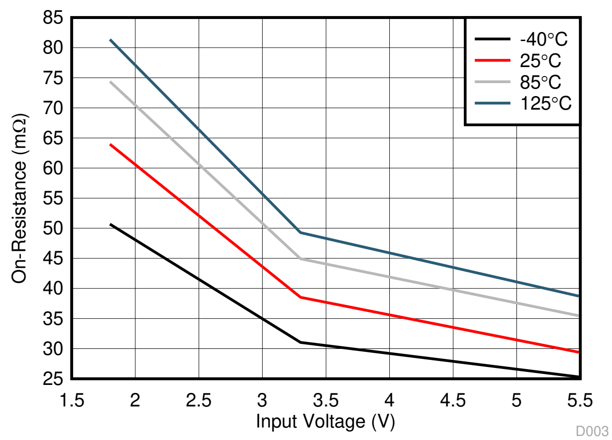
$V_{ON} \geq V_{IH}$

图 6-1. Quiescent Current vs. Input Voltage



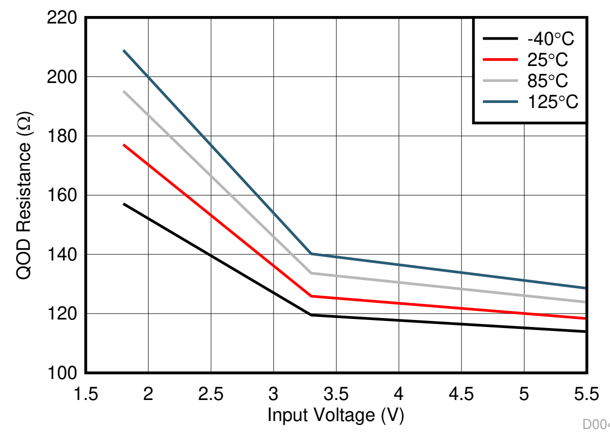
$V_{ON} \leq V_{IL}$

图 6-2. Shutdown Current vs. Input Voltage



$V_{ON} \geq V_{IH}$ I_{OUT} = –200 mA

图 6-3. On-Resistance vs. Input Voltage



$V_{ON} \leq V_{IL}$

图 6-4. QOD Resistance vs. Input Voltage

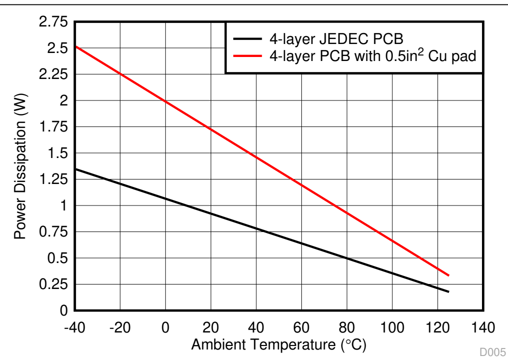


图 6-5. Maximum Power Dissipation vs Ambient Temperature

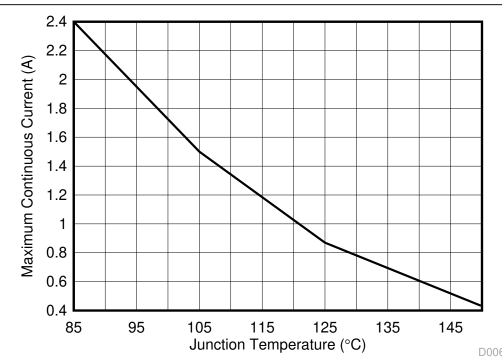
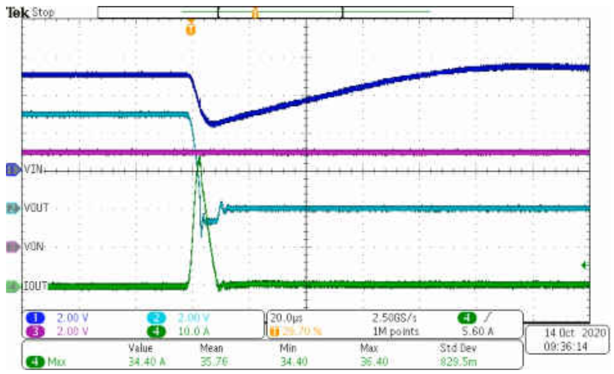


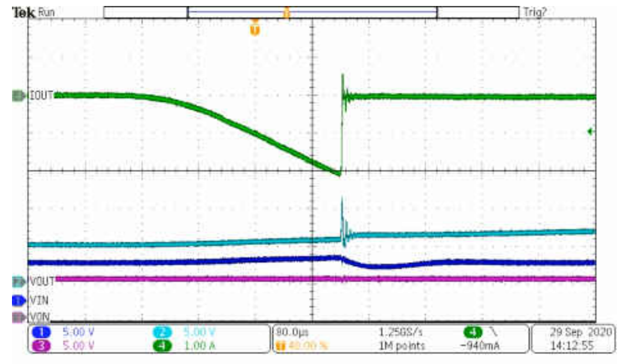
图 6-6. Maximum Continuous Current vs Junction Temperature

6.7 Typical Characteristics (continued)



V_{IN} = 5V V_{ON} = 5V

图 6-7. Short Circuit Response



V_{IN} = 5V V_{ON} = 5V

图 6-8. Reverse Current Blocking

7 Parameter Measurement Information

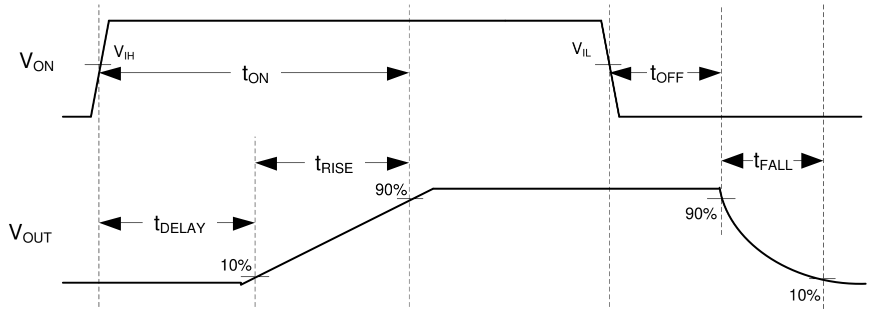


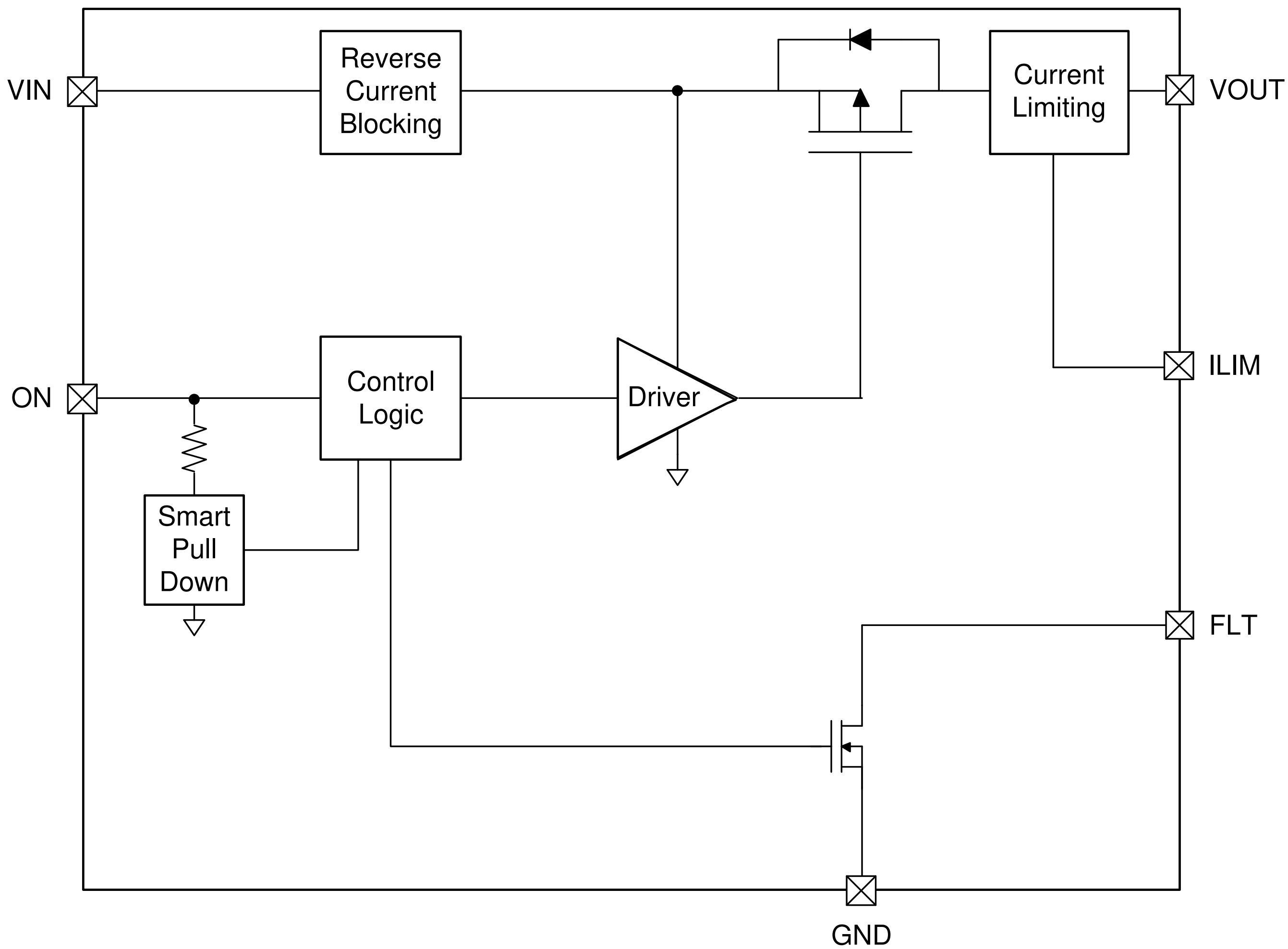
图 7-1. Timing Waveform

8 Detailed Description

8.1 Overview

This section describes the switch features and functional behavior.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Current Limiting

The TPS22950 responds to overcurrent conditions by limiting its output current to the I_{LIM} level shown in the Figure below.

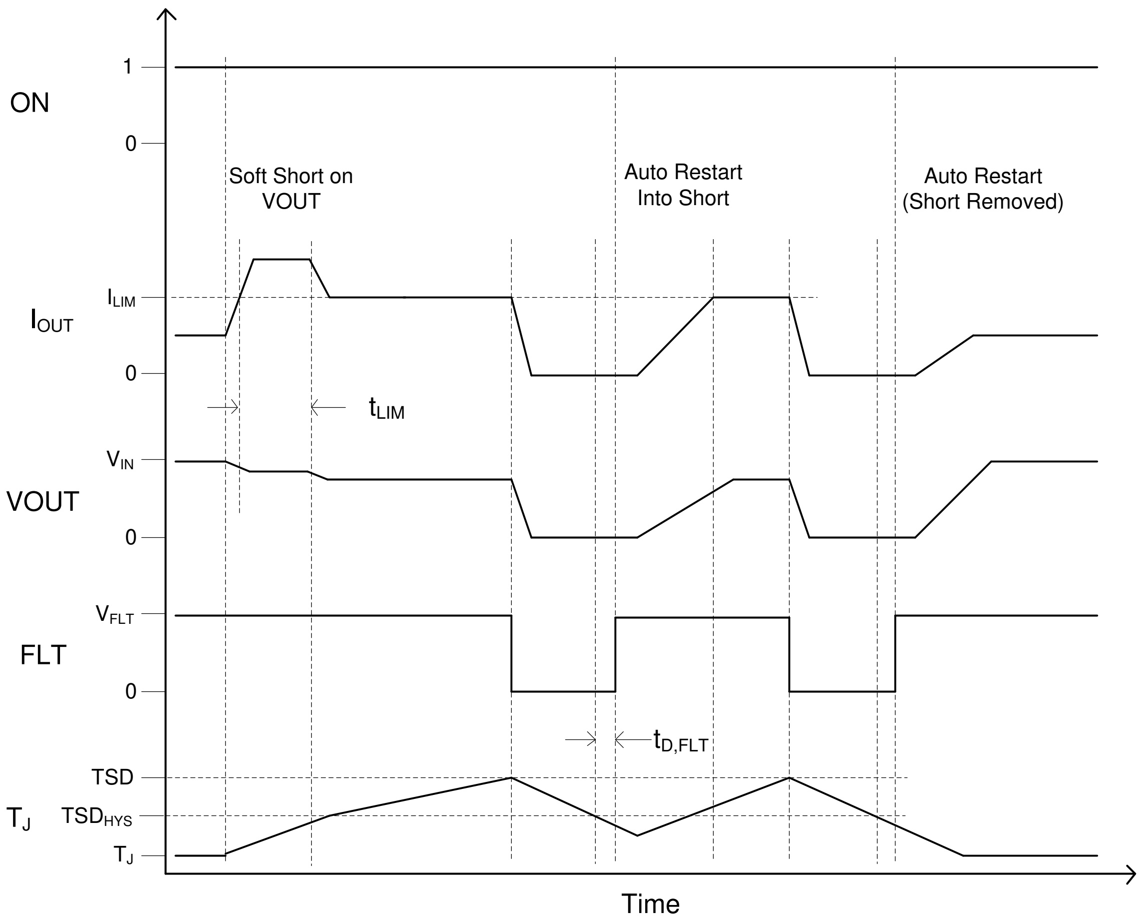


图 8-1. Output Current Limit for Short Circuit Protection (t_{LIM})

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present on the output and the ON pin is toggled high, turning the device on. The output voltage is held near zero potential with respect to ground and the TPS22950 ramps the output current to I_{LIM}. The TPS22950 device will limit the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and the device turns itself off. The device remains off until the junction temperature has lowered to TSD_{HYS}, and the device will turn itself back on. This will cycle until the overload condition is removed.

The second condition is when a short circuit, partial short circuit, or transient overload occurs after the device has been fully powered on. The device responds to the overcurrent condition within time t_{LIM} (see figure below), and before this time the current is able to exceed I_{LIM}. In the case of a fast transient, the current-sense amplifier is overdriven and momentarily disables the internal power FET. The current-sense amplifier recovers and limits the output current to I_{LIM}. Similar to the previous case, the TPS22950 limits the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and begins thermally cycling on and off.

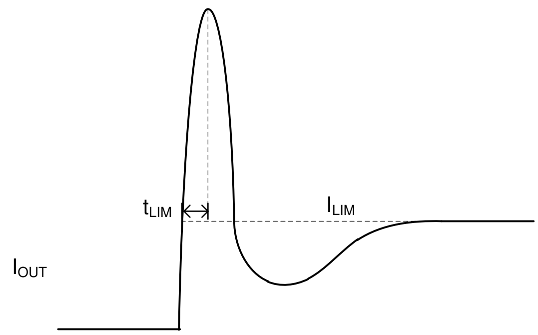


图 8-2. Transient Current Limit Waveform

8.3.1.1 Adjusting the current limit

The current limit is adjusted by connecting an external resistor from the ILIM pin to GND. The current limit resistor can be chosen using the equation:

$$I_{LIM} = 1.18 \times (R_{ILIM})^{-1.072} \quad (1)$$

8.3.2 Reverse Current Blocking (RCB)

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN}, there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold is exceeded (about 900 mA), there is a delay time (t_{RCB}) before the switch turns off to stop the current flow. The switch will remain off and block reverse current as long as the reverse voltage condition exists. Once V_{OUT} has dropped below the release voltage threshold (V_{RCB}) the device will turn back on. When the ON pin is pulled low, the device will constantly block reverse current.

8.4 Device Functional Modes

The tables below summarize the Device Functional Modes.

表 8-1. Output Connection Table

ON	Fault Condition	VOUT State	FLT State
L	N/A	Hi-Z	Hi-Z
H	None	VIN (via R_{ON})	Hi-Z
H	Output Short	Current Limited	Hi-Z
H	Thermal Shutdown	Hi-Z	L
H	Reverse Current	Hi-Z	L

表 8-2. Smart-ON Functional Modes ($R_{PD,ON}$)

ON	ON Pin
≤ V_{IL}	Pull Down Active
≥ V_{IH}	No Pull Down

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22950 device can be used to set an adjustable current limit.

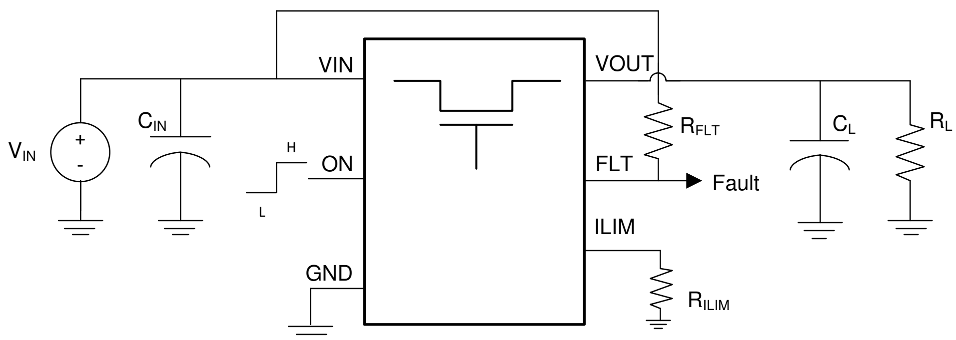


图 9-1. Typical Application

9.2.1 Design Requirements

For this example, the values below are used as the design parameters.

表 9-1. Design Parameters

PARAMETER	VALUE
Input Voltage (V_{IN})	5 V
Load Current (mA)	100 mA
Typical Current Limit (mA)	500 mA

9.2.2 Detailed Design Procedure

In this example the nominal load current is 100 mA, so the current limit can be set to 500 mA without disrupting normal operation. Use 方程式 2 to calculate the resistor needed on the ILIM pin.

$$I_{LIM} = 1.18 \times (R_{ILIM})^{-1.072} \quad (2)$$

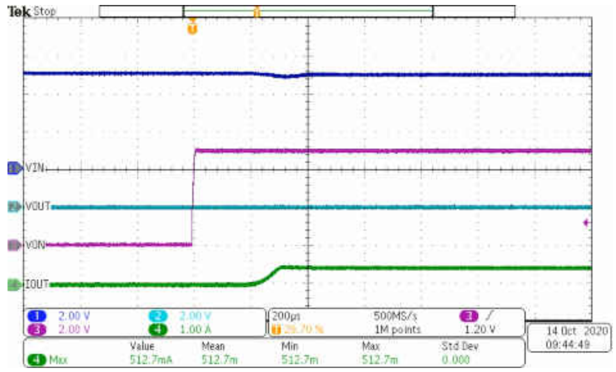
where

- I_{LIM} = Typical current limit setting
- R_{ILIM} = Resistor on the ILIM pin

Based on 方程式 2, a 2.21-kΩ resistor should be used on the ILIM pin to set a typical current limit of 500 mA.

9.2.3 Application Curves

The below scope shot shows the device turning on into a fault condition and limiting the current to the specified amount of 500 mA.



R_{ILIM} = 2.5 kΩ　　V_{OUT} = GND

图 9-2. TPS22950 Turning On into an Output Short

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.8 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

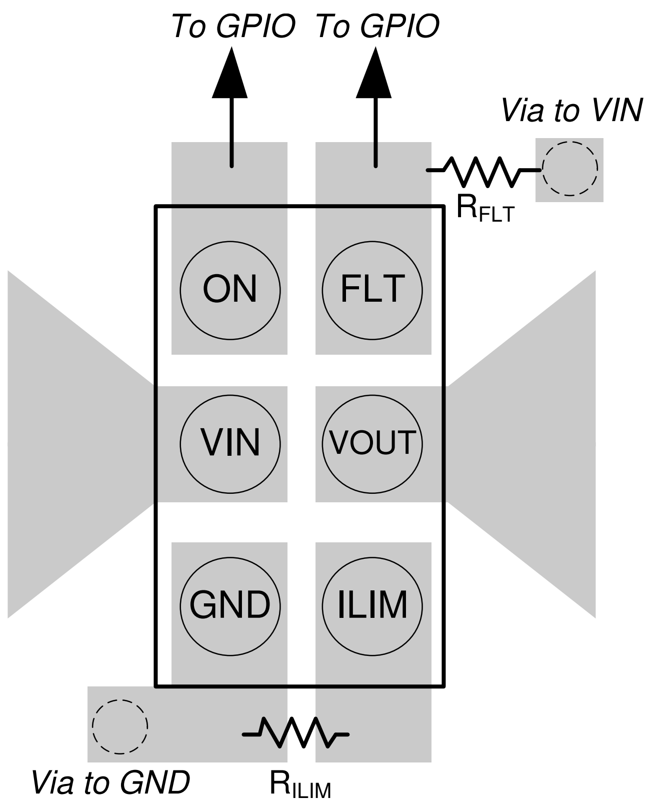


图 11-1. TPS22950 Layout Example

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

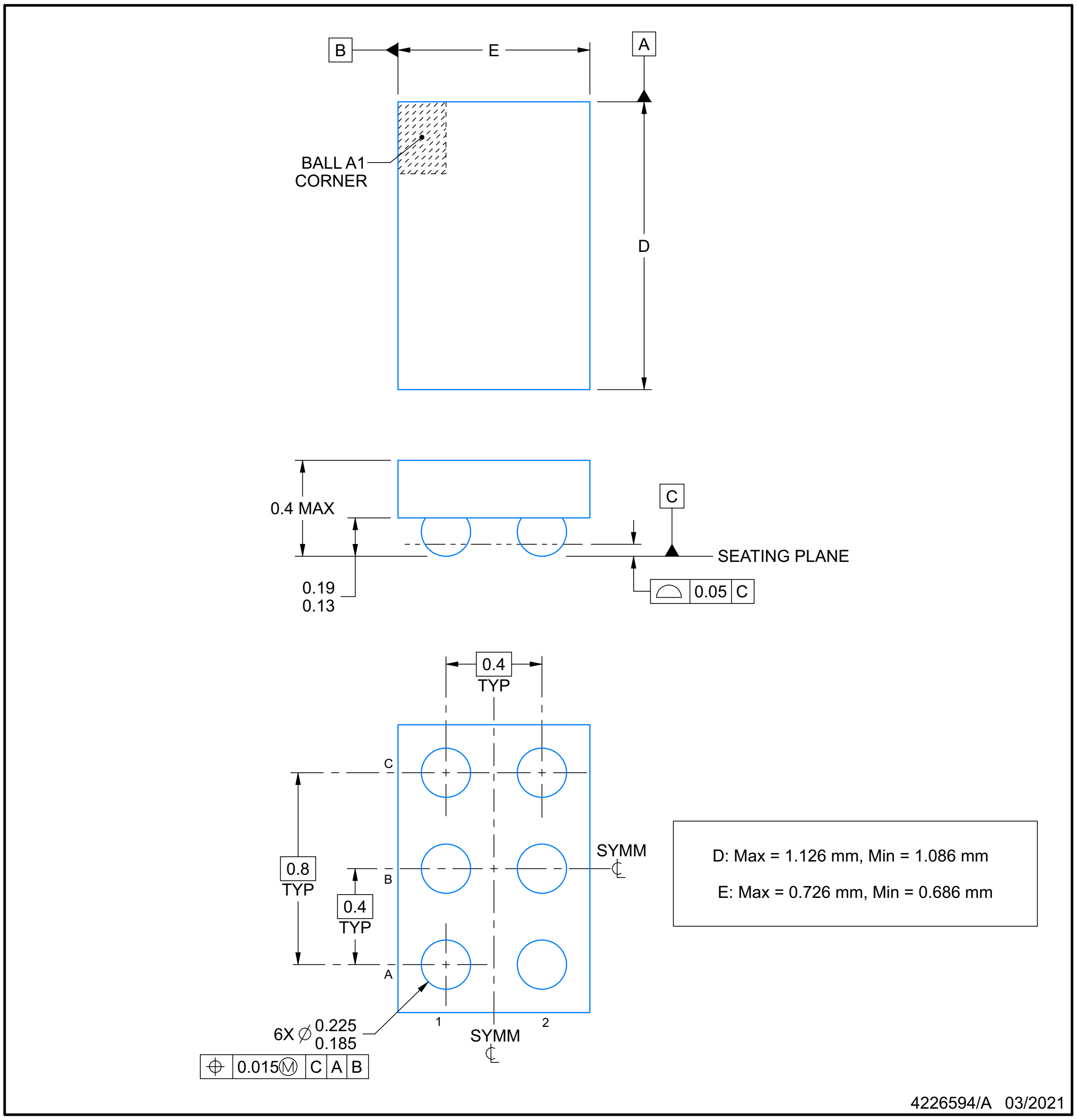
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YBH0006-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

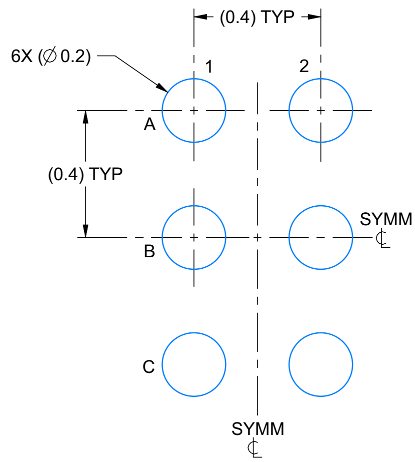
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

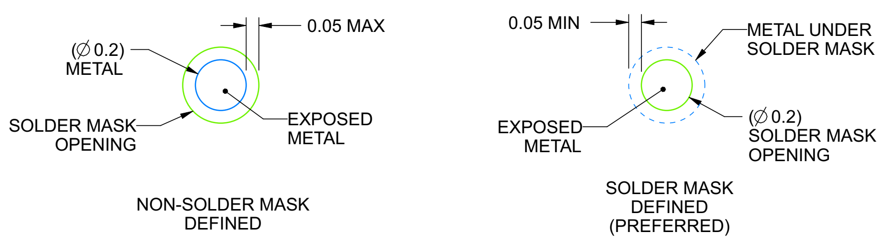
YBH0006-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4226594/A 03/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

TEXAS INSTRUMENTS
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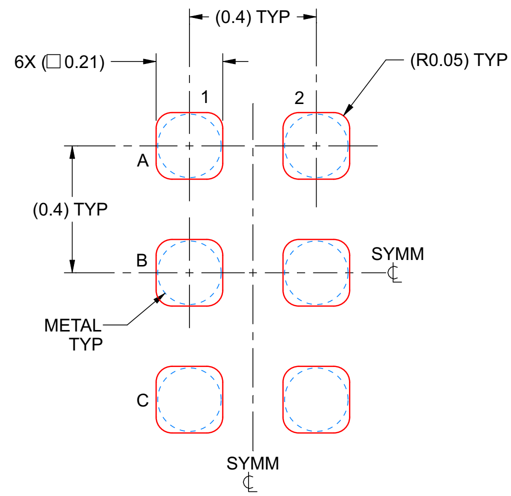
EXAMPLE STENCIL DESIGN

YBH0006-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4226594/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22950YBHR	ACTIVE	DSBGA	YBH	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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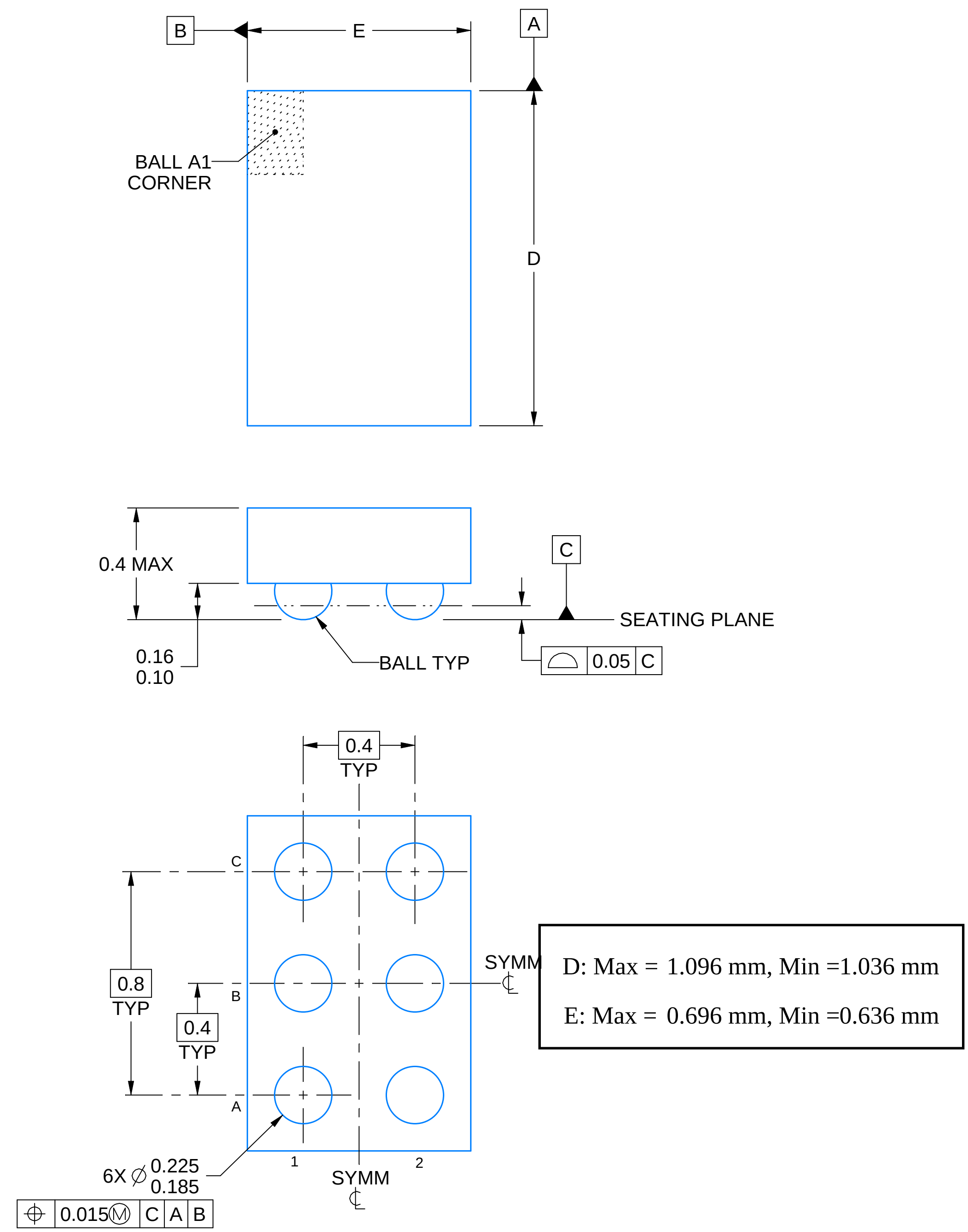
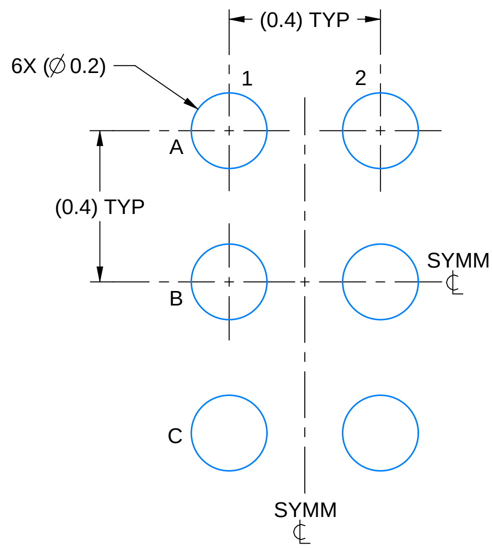
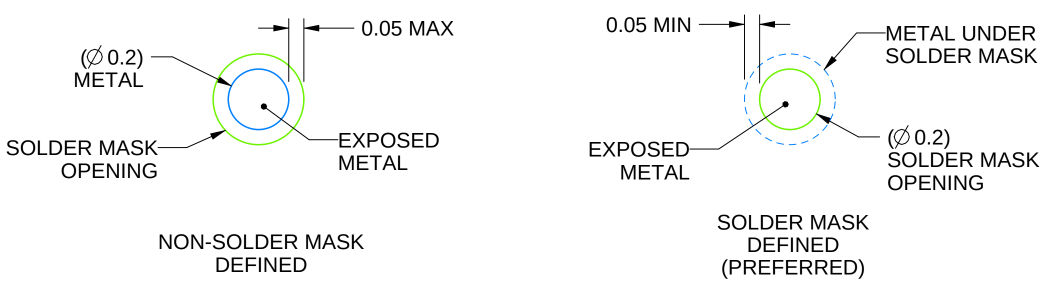


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

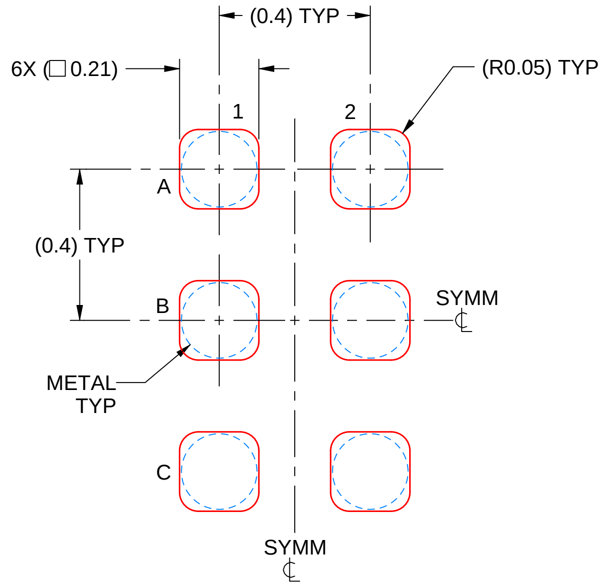


SOLDER MASK DETAILS
NOT TO SCALE

4224514/A 08/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4224514/A 08/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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