TEXAS INSTRUMENTS

具有使能功能的 **TPS3431**标准可编程监视器计时器

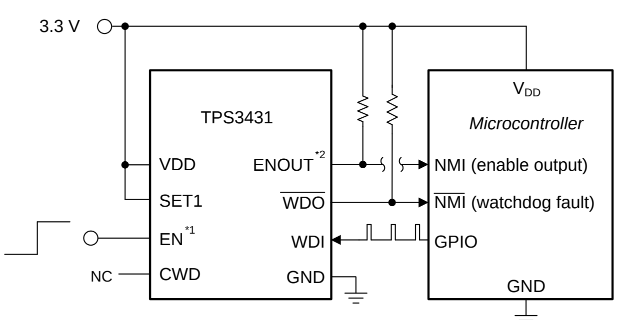
1 特性

- 出厂编程的精密监视器计时器：
  - 可在工作温度范围内实现 ±15% 的监视器超时 (WDT) 精度
  - 可在 25°C 条件下实现 ±2.5% 的监视器超时 (WDT) 精度（典型值）
- 看门狗禁用功能
- 用户可通过编程设定的看门狗超时
- 输入电压范围：V_{DD} = 1.8V 至 6.5V
- 低静态电流：I_{DD} = 10µA（典型值）
- 低电平有效的开漏输出
- 使能输入 (EN) 和使能输出 (ENOUT)
- 采用 3mm x 3mm、8 引脚晶圆级超小外形无引线 (VSON) 封装
- 工作结温范围：-40°C 至 +125°C

2 应用

- 视频监控
- 传感器变送器
- HVAC（恒温器）
- 防火安全（热量和烟雾探测器）
- 医疗（个人护理和健身）
- 现场可编程门阵列 (FPGA) 和专用集成电路 (ASIC) 通用电源
- 微控制器和信号处理器 (DSP) 传感器

标准监视器计时器电路



(1) 也可以将 EN 保持浮动并将其从内部上拉至 VDD

(2) 也可以将 ENOUT 保持浮动或将其连接至 WDO

3 说明

TPS3431 是一款具有使能功能的标准可编程监视器计时器，适用于各种 应用。计时器超时特性 可实现 15% 精度的高精度计时（–40°C 至 +125°C）和 2.5% 的典型精度（25ºC 条件下）。计时器超时可通过外部电容器或通过出厂时编程的默认延迟设置进行编程。在开发过程中，可以通过 Enable 引脚或 SET 逻辑引脚将监视器禁用，从而避免出现不必要的监视器超时。

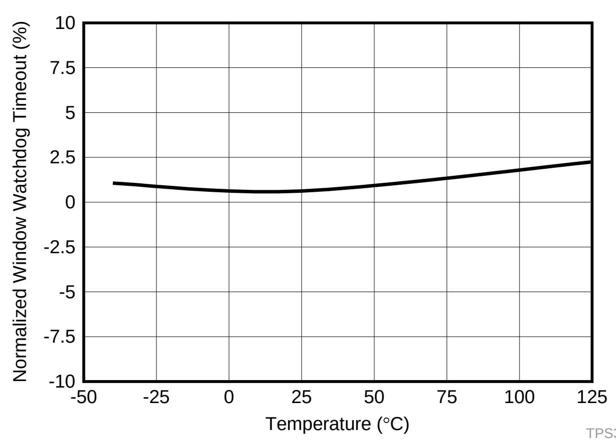
TPS3431 可提供小型 3.00mm × 3.00mm 8 引脚 VSON 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS3431	VSON (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

标准化监视器超时 **(t_{WD})** 精度（**SET1 = 1**，**CWD = NC**）



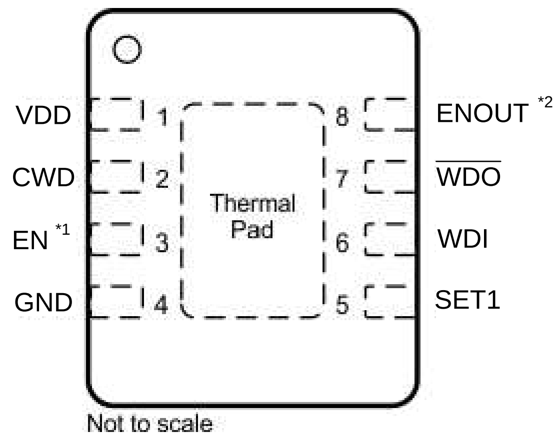
目录

4 修订历史记录

日期	修订版本	说明
2018 年 7 月	*	初始发行版。

5 Pin Configuration and Functions

DRB Package: TPS3431
3-mm × 3-mm VSON-8
Top View



(1) EN can also be left floating and is internally pulled-up to VDD
(2) ENOUT can also be left floating or tied to $\overline{\text{WDO}}$

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	Supply voltage pin. For noisy systems, connecting a 0.1-µF bypass capacitor is recommended.
CWD	2	I	Programmable watchdog timeout input. The watchdog timeout is set by connecting a capacitor between this pin and ground. Connecting via a 10-kΩ resistor to V_{DD} or leaving unconnected further enables the selection of the preset watchdog timeouts; see the *CWD Functionality* section. TheTPS3431 determines the watchdog timeout using Equation 1
EN	3	I	Enable input pin. This pin is internally pulled up to V_{DD} and must be logic high or left floating. When EN goes logic low, ENOUT goes logic low and WDI is ignored and $\overline{\text{WDO}}$ remains logic high. When EN goes logic high, ENOUT goes high (asserts) after the watchdog reset delay time (t_{RST}). This pin can also be driven with an external push-button, transistor, or microcontroller.
GND	4	—	Ground pin
SET1	5	I	Logic input. Grounding the SET1 pin disables the watchdog timer. SET1 and CWD select the watchdog timeouts; see the *SET1* section.
WDI	6	I	Watchdog input. A falling edge must occur at WDI before the timeout (t_{WD}) expires. When the watchdog is not in use, the SET1 pin can be used to disable the watchdog. WDI is ignored when $\overline{\text{WDO}}$ is low (asserted) and when the watchdog is disabled. If the watchdog is disabled, WDI cannot be left unconnected and must be driven to either VDD or GND.
$\overline{\text{WDO}}$	7	O	Watchdog open-drain active-low output. Connect $\overline{\text{WDO}}$ with a 1-kΩ to 100-kΩ resistor to the correct pull-up voltage rail (V_{PU}). $\overline{\text{WDO}}$ goes low (asserts) when a watchdog timeout occurs. When a watchdog timeout occurs, $\overline{\text{WDO}}$ goes low (asserts) for the watchdog reset delay time (t_{RST}). When EN goes low, $\overline{\text{WDO}}$ is in a high-impedance state and will be pulled to logic high.
ENOUT	8	O	Enable open-drain active-high output. Connect ENOUT with a 1-kΩ to 100-kΩ resistor to the correct pull-up voltage rail (V_{PU}). When EN goes logic high, ENOUT goes high impedance and pulls logic high (asserts) due to the external pull-up resistor after the watchdog reset delay time (t_{RST}). When EN is forced logic low, ENOUT goes low after 200 ns and remains logic low as long as EN is logic low.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	7	V
Output voltage range	ENOUT, $\overline{WDO}$	–0.3	7	V
Voltage ranges	SET1, WDI, EN	–0.3	7	V
	CWD	–0.3	VDD + 0.3(2)	
Output pin current	ENOUT, $\overline{WDO}$		±20	mA
Input current (all pins)			±20	mA
Continuous total power dissipation		See	See	
Temperature	Operating junction, T_J (3)	–40	150	°C
	Operating free-air temperature, T_A (3)	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{DD} + 0.3 V or 7.0 V, whichever is smaller.
(3) $T_J = T_A$ as a result of the low dissipated power in this device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply pin voltage	1.8		6.5	V
V_{SET1}	SET1 pin voltage	0		6.5	V
C_{CWD}	Watchdog timing capacitor	0.1(1)		1000(1)	nF
CWD	Pullup resistor to VDD	9	10	11	kΩ
R_{PU}	Pullup resistor, ENOUT and $\overline{WDO}$	1	10	100	kΩ
I_{EN}	EN pin current			10	mA
$I_{\overline{WDO}}$	Watchdog output current			10	mA
T_J	Junction Temperature	–40		125	°C

(1) Using a C_{CWD} capacitor of 0.1 nF or 1000 nF gives a $t_{WDU(typ)}$ of 62.74 ms or 77.45 seconds, respectively.

6.4 Thermal Information

THERMAL METRIC[1]		TPS3431 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at 1.8 V ≤ V_{DD} ≤ 6.5 V over the operating temperature range of –40°C ≤ T_J ≤ +125°C (unless otherwise noted); the open-drain pullup resistors are 10 kΩ; typical values are at T_J = 25°C

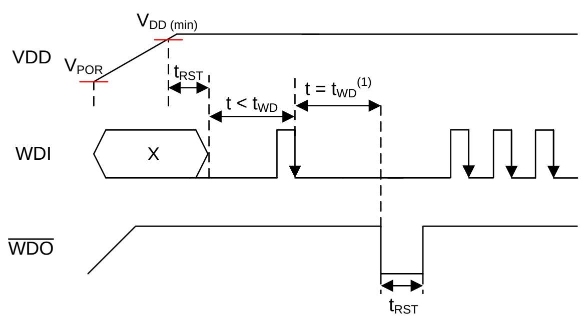
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
V_{DD} [1] [2]	Supply voltage		1.8		6.5	V
I_{DD}	Supply current			10	19	µA
V_{POR} [3]	Power-on reset voltage	$V_{OL(MAX)}$ = 0.25 V			0.8	V
WINDOW WATCHDOG FUNCTION						
I_{EN}	EN pin internal pullup current	V_{EN} = 0V	500	620	700	nA
I_{CWD}	CWD pin charge current	CWD = 0.5 V	337	375	413	nA
V_{CWD}	CWD pin threshold voltage		1.192	1.21	1.228	V
V_{OL}	ENOUT, $\overline{WDO}$ output low	VDD = 5 V, I_{SINK} = 3 mA			0.4	V
I_D	ENOUT, $\overline{WDO}$ output leakage current	VDD = 1.8 V, $V_{\overline{WDO}}$ = 6.5 V			1	µA
V_{IL}	Low-level input voltage (EN, SET1)				0.25	V
V_{IH}	High-level input voltage (EN, SET1)		0.8			V
$V_{IL(WDI)}$	Low-level input voltage (WDI)				0.3 × V_{DD}	V
$V_{IH(WDI)}$	High-level input voltage (WDI)		0.8 × V_{DD}			V

(1) When V_{DD} falls below VDD_{MIN}, WDI is ignored and ENOUT is driven low
(2) During power-on, V_{DD} must be a minimum 1.8 V for at least 300 µs before WDI is active and ENOUT is high impedance.
(3) When V_{DD} falls below V_{POR}, WDI and ENOUT is undefined.

6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
GENERAL						
t_{INIT}	CWD, CRST pin evaluation period			381		µs
	EN, SET1 pin setup time			1		µs
	Startup delay(1)			300		µs
DELAY FUNCTION						
t_{EN_ENOUT}	EN to ENOUT delay			200		ns
t_{RST}	Watchdog reset delay		170	200	230	ms
WINDOW WATCHDOG FUNCTION						
t_{WD}	Watchdog timeout	CWD = NC, SET1 = 1	1360	1600	1840	ms
		CWD = 10 kΩ to VDD, SET1 = 1	170	200	230	ms
		CWD = NC, SET1 = 0		Watchdog disabled		
		CWD = 10 kΩ to VDD, SET1 = 0		Watchdog disabled		
$t_{WD\text{-}setup}$	Setup time required for device to respond to changes on WDI after being enabled			150		µs
	Minimum WDI pulse duration			50		ns
$t_{WD\text{-}del}$	WDI to $\overline{WDO}$ delay			50		ns

(1) During power-on, V_{DD} must be a minimum 1.8 V for at least 300 µs before WDI is active and ENOUT is high impedance.



(1) See 图 2 for WDI timing requirements.

图 1. Timing Diagram

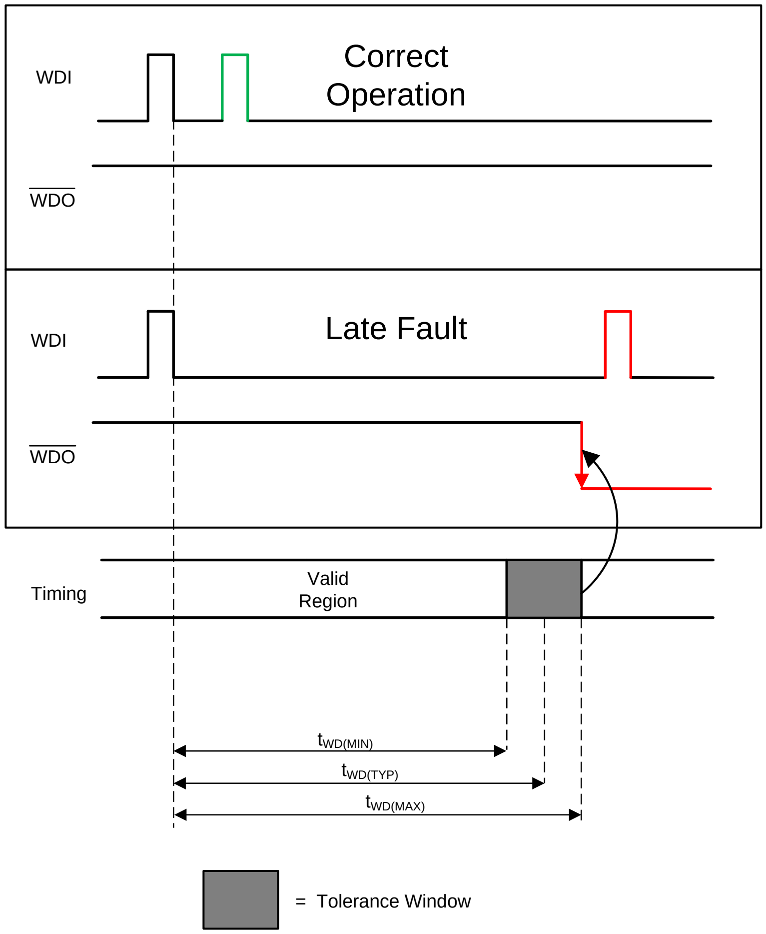


图 2. Watchdog Timing Diagram

6.7 Typical Characteristics

all typical characteristics curves are taken at 25°C with 1.8 V ≤ VDD ≤ 6.5 V (unless other wise noted)

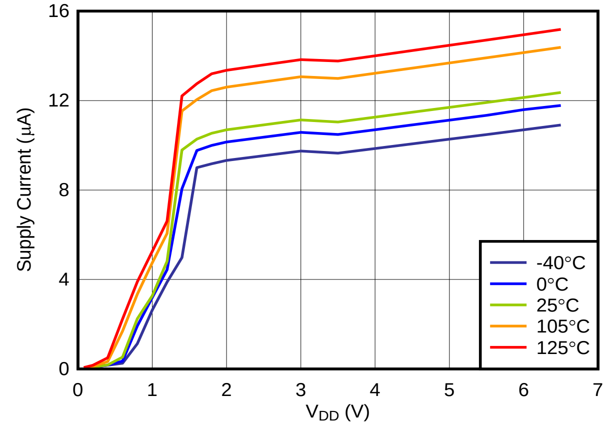
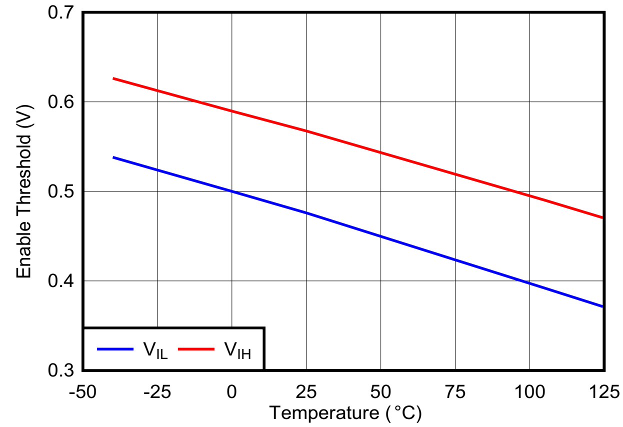


图 3. Supply Current vs V_{DD}



VDD = 1.8 V

图 4. EN Threshold vs Temperature

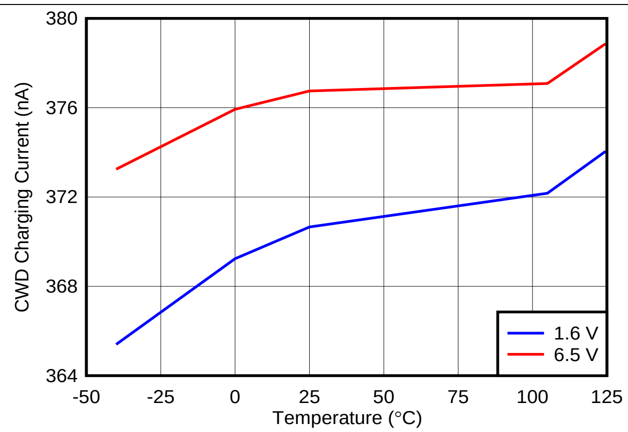


图 5. CWD Charging Current vs Temperature

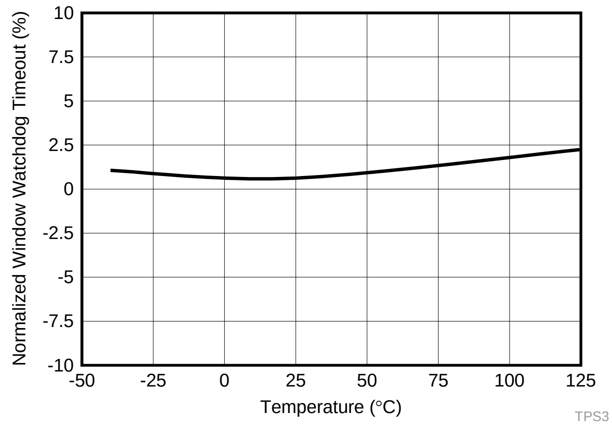


图 6. Normalized Watchdog Timeout (t_{WD}) Accuracy (SET1 = 1, CWD = NC)

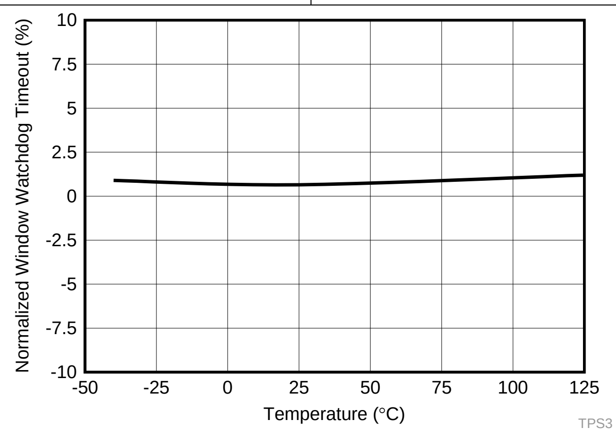


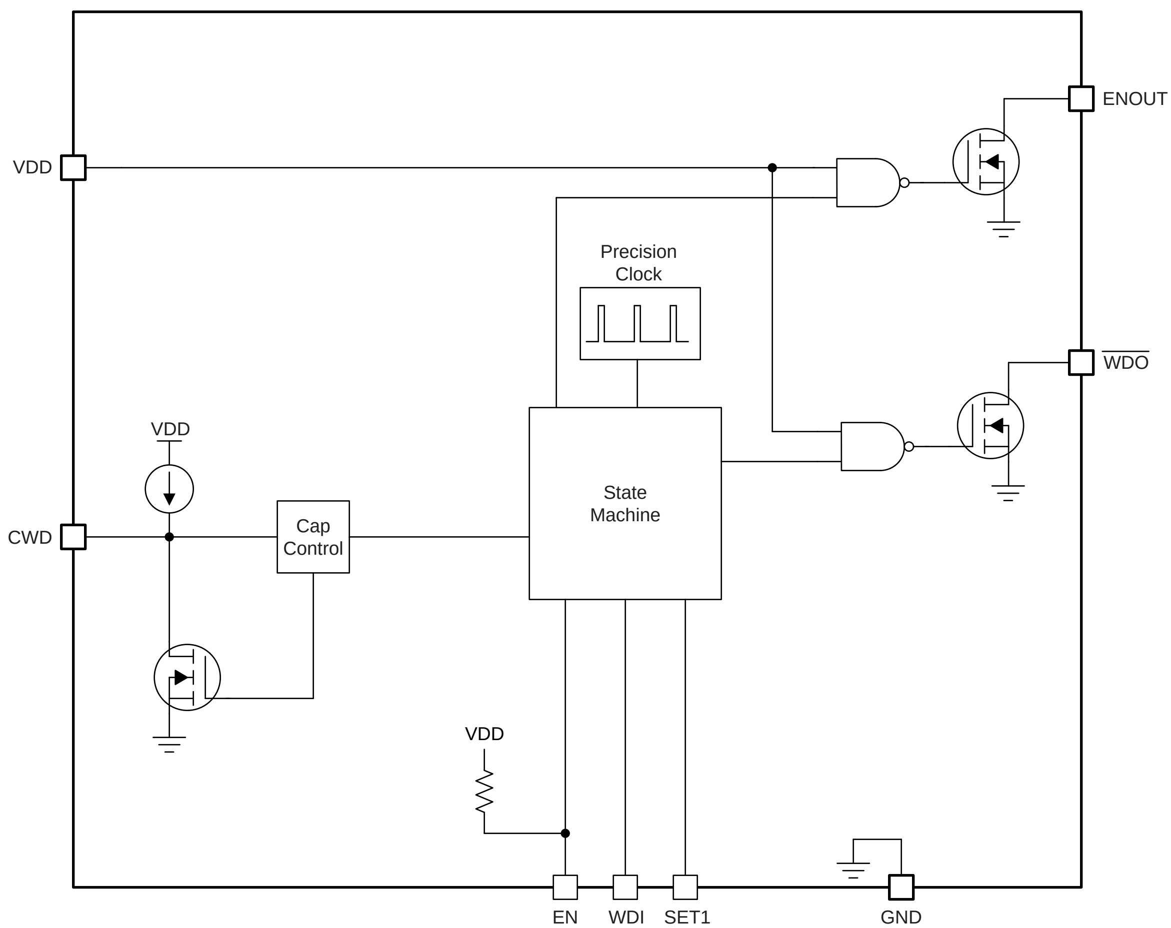
图 7. Normalized Watchdog Timeout (t_{WD}) Accuracy (SET1 = 1, CWD = 10kΩ)

7 Detailed Description

7.1 Overview

The TPS3431 is a standard programmable watchdog timer with enable/disable feature. This device includes a precision watchdog timer that achieves 15% timing accuracy over the specified temperature range of –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable Input (EN) and Enable Output (ENOUT)

The Enable (EN) input allows a processor or other logic circuits to initiate a single cycle watchdog reset by momentarily bringing Enable low, or a permanent disable by keeping Enable low. After EN goes to a logic high and V_{DD} is above $V_{DD\ (min)}$, ENOUT and $\overline{WDO}$ go logic high after the watchdog reset delay time (t_{RST}). If EN is not controlled externally, then EN can either be connected to V_{DD} or left floating because the EN pin is internally pulled up to VDD. When EN is forced logic low, ENOUT goes low after a propagation delay of 200 ns and $\overline{WDO}$ goes high impedance and pulls to logic high due to the external pull-up resistor. Because $\overline{WDO}$ and ENOUT are both open-drain outputs, these outputs can be tied together to create an OR logic function so that if either output pulls down to logic low, the other will also pull down logic low.

7.3.2 Watchdog Mode

This section provides information for the watchdog mode of operation.

Feature Description (接下页)

7.3.2.1 CWD

The CWD pin provides the user the functionality of both high-precision, factory-programmed watchdog timing options and user-programmable watchdog timing. The TPS3431 features three options for setting the watchdog timer: connecting a capacitor to the CWD pin, connecting a pull-up resistor to VDD, and leaving the CWD pin unconnected. The configuration of the CWD pin is evaluated by the device every time V_{DD} rises above $V_{DD\ (min)}$. The pin evaluation is controlled by an internal state machine that determines which option is connected to the CWD pin. The sequence of events typically takes 381 µs (t_{INIT}) to determine if the CWD pin is left unconnected, pulled-up through a resistor, or connected to a capacitor. If the CWD pin is being pulled up to VDD, a 10-kΩ resistor is required.

7.3.2.2 Watchdog Input WDI

WDI is the watchdog timer input that controls the $\overline{\text{WDO}}$ output. The WDI input is triggered by the falling edge of the input signal. To ensure proper functionality of the watchdog timer, always issue the WDI pulse before $t_{WD(min)}$. If the pulse is issued in this region, then $\overline{\text{WDO}}$ remains unasserted. Otherwise, the device asserts $\overline{\text{WDO}}$, putting the $\overline{\text{WDO}}$ pin into a low-impedance state therefore $\overline{\text{WDO}}$ will be logic low.

The watchdog input (WDI) is a digital pin. To ensure there is no increase in I_{DD}, drive the WDI pin to either VDD or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current (I_{DD}) because of the architecture of the digital logic gates. When EN is logic low, the watchdog is disabled and all signals input to WDI are ignored. When EN is logic high, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either VDD or GND. 图 8 shows the valid region for a WDI pulse to be issued to prevent $\overline{\text{WDO}}$ from being triggered and pulled low.

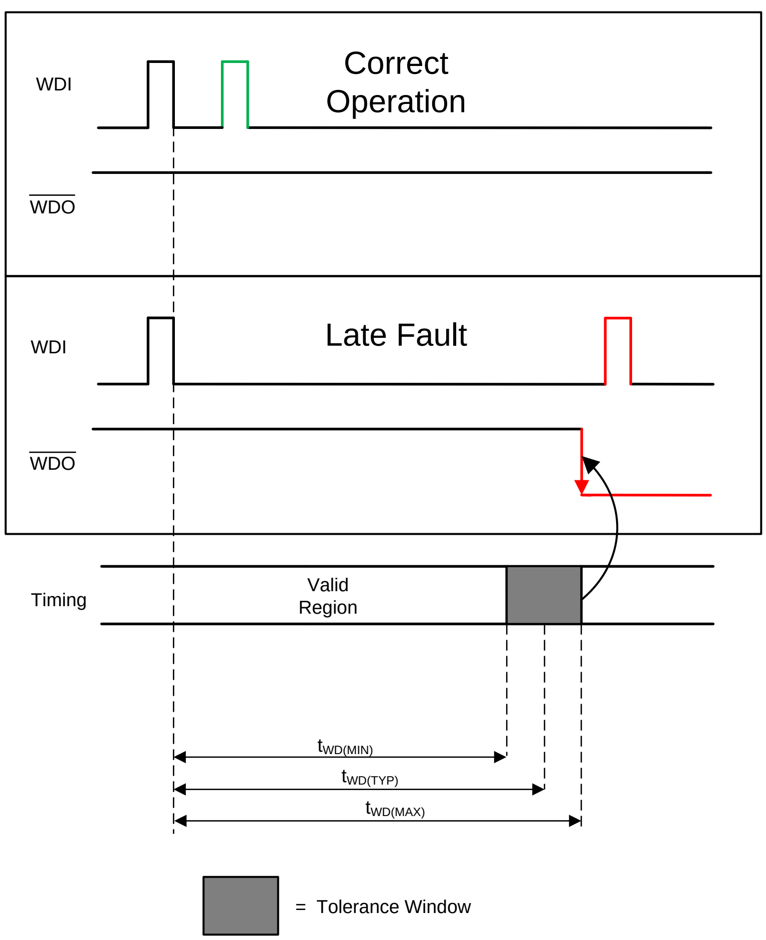


图 8. Watchdog Timing Diagram

Feature Description (接下页)

7.3.2.3 Watchdog Output $\overline{\text{WDO}}$

The TPS3431 features an active-low open-drain watchdog output that asserts when a pulse on WDI fails to arrive within the watchdog timeout. When EN is logic high, the $\overline{\text{WDO}}$ signal maintains normal operation. When the EN pin is logic low, the $\overline{\text{WDO}}$ pin goes to a high-impedance state and pulls logic high due to the external pull-up resistor. Because $\overline{\text{WDO}}$ and ENOUT are both open-drain outputs, these outputs can be tied together to create an OR logic function so that if either output pulls down to logic low, the other will also pull down logic low.

7.3.2.4 SET1

The SET1 pin can enable and disable the watchdog timer and should be used when disabling the watchdog timer for longer than one watchdog reset cycle. If SET1 is set to GND, the watchdog timer is disabled and WDI is ignored. If the watchdog timer is disabled, drive the WDI pin to either GND or VDD to ensure that there is no increase in I_{DD}. When SET1 is logic high, the watchdog operates normally. The SET1 pin can be changed dynamically; however, if the watchdog is going from disabled to enabled there is a 150 µs setup time where the watchdog does not respond to changes on WDI, as shown in 图 9. Note: disabling using SET1 pin causes a delay defined by the fixed 150-us setup time when enabling again.

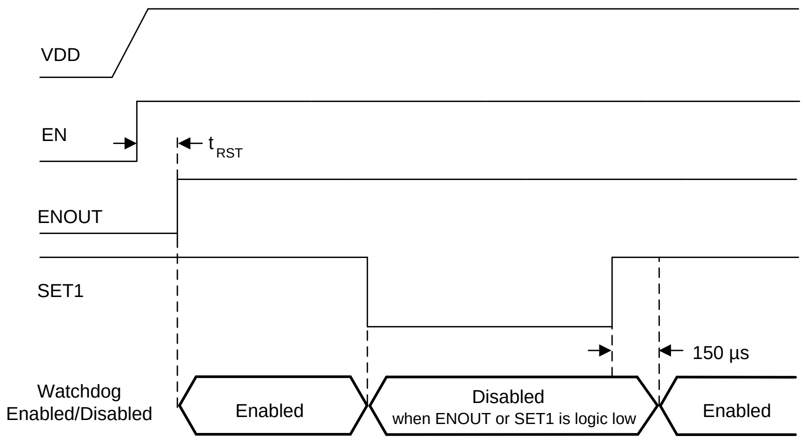


图 9. Enabling and Disabling the Watchdog

7.4 Device Functional Modes

表 1 summarizes the functional modes of the TPS3431.

表 1. Device Functional Modes

V_{DD}	EN	ENOUT	WDI	$\overline{\text{WDO}}$
$V_{DD} < V_{POR}$	---	---	---	---
$V_{POR} \leq V_{DD} < V_{DD(min)}$	---	Low	Ignored	High
$V_{DD} > V_{DD\ (min)}$ [1]	High	High	$t_{PULSE} < t_{WD(min)}$ [2]	High
$V_{DD} > V_{DD\ (min)}$ [1]	High	High	$t_{PULSE} > t_{WD(min)}$ [2]	Low
$V_{DD} > V_{DD\ (min)}$ [1]	Low	Low	Ignored	High

(1) V_{DD} must be above $V_{DD\ (min)}$ for longer than 300 µs.
(2) Where t_{pulse} is the time between the falling edges on WDI.

7.4.1 V_{DD} is Below V_{POR} ($V_{DD} < V_{POR}$)

When V_{DD} is less than V_{POR}, $\overline{WDO}$ is undefined and can be either high or low. The state of $\overline{WDO}$ largely depends on the load that the $\overline{WDO}$ pin is experiencing.

7.4.2 Above Power-On-Reset, But Less Than $V_{DD(min)}$ ($V_{POR} \leq V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than $V_{DD(min)}$, and greater than or equal to V_{POR}, the $\overline{WDO}$ signal is asserted (logic low). When EN is logic low, the watchdog output $\overline{WDO}$ is in a high-impedance state and logic low regardless of the WDI signal that is input to the device.

7.4.3 Normal Operation ($V_{DD} \geq V_{DD(min)}$)

When V_{DD} is greater than or equal to $V_{DD(min)}$ and EN is logic high, the $\overline{WDO}$ signal is determined by WDI. When WDI is within the watchdog timeout, the internal MOSFET turns off and $\overline{WDO}$ is pulled high through external pull-up resistor. When WDI is not within the watchdog timeout, the internal MOSFET turns on and $\overline{WDO}$ is pulled to logic low. When EN is logic low, ENOUT goes to logic low and $\overline{WDO}$ goes to a high-impedance state and pulls to logic high due to the external pull-up resistor.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.1.1 CWD Functionality

The TPS3431 features three options for setting the watchdog timeout: connecting a capacitor to the CWD pin, connecting a pull-up resistor to VDD, and leaving the CWD pin unconnected. 图 10 shows a schematic drawing of all three options. If this pin is connected to VDD through a 10-kΩ pullup resistor or left unconnected (high impedance), then the factory-programmed watchdog timeouts are enabled; see the *Factory-Programmed Timing Options* section. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.

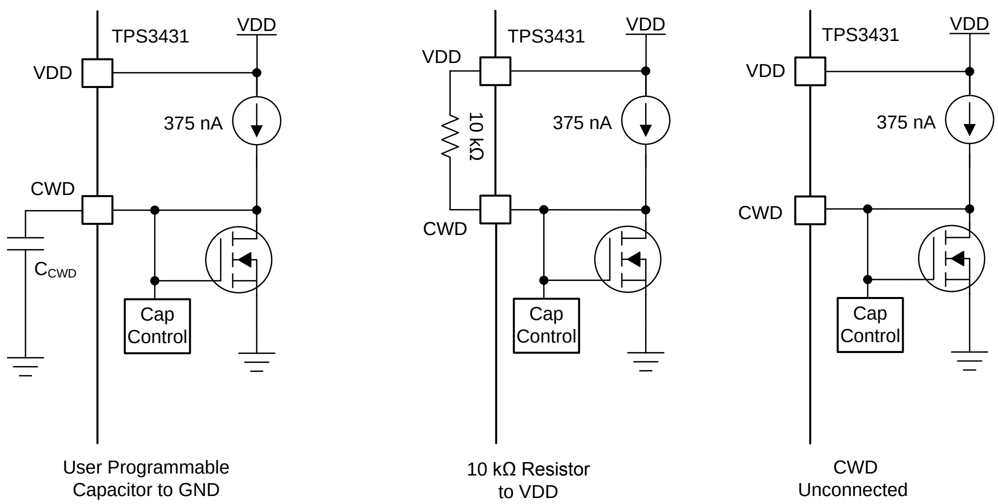


图 10. CWD Charging Circuit

8.1.1.1 Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in 表 2), the CWD pin must either be unconnected or pulled up to VDD through a 10-kΩ pull-up resistor. Using these options enables high-precision, 15% accurate watchdog timing.

表 2. Factory Programmed Watchdog Timing

INPUT		STANDARD WATCHDOG TIMEOUT WDT (t_{WD})			UNIT
CWD	SET1	MIN	TYP	MAX	
NC	0	Watchdog disabled			
NC	1	1360	1600	1840	ms
10 kΩ to VDD	0	Watchdog disabled			
10 kΩ to VDD	1	170	200	230	ms

Application Information (接下页)

8.1.1.2 CWD Adjustable Capacitor Watchdog Timeout

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375-nA, constant-current source charges C_{CWD} until V_{CWD} = 1.21 V. 表 3 shows how to calculate t_{WD} using 公式 1 and the SET1 pin. The TPS3431 determines the watchdog timeout with the formulas given in 公式 1, where C_{CWD} is in nanofarads and t_{WD} is in milliseconds.

$$t_{WD}(ms) = 77.4 \times C_{CWD}(nF) + 55\ (ms) \quad (1)$$

The TPS3431 is designed and tested using C_{CWD} capacitors between 100 pF and 1 µF. Note that 公式 1 is for ideal capacitors and capacitor tolerances vary the actual device timing. For the most accurate timing, use ceramic capacitors with COG dielectric material. If a C_{CWD} capacitor is used, 公式 1 can be used to set t_{WD} for the watchdog timeout. 表 4 shows the minimum and maximum calculated t_{WD} values using an ideal capacitor.

表 3. Programmable CWD Timing

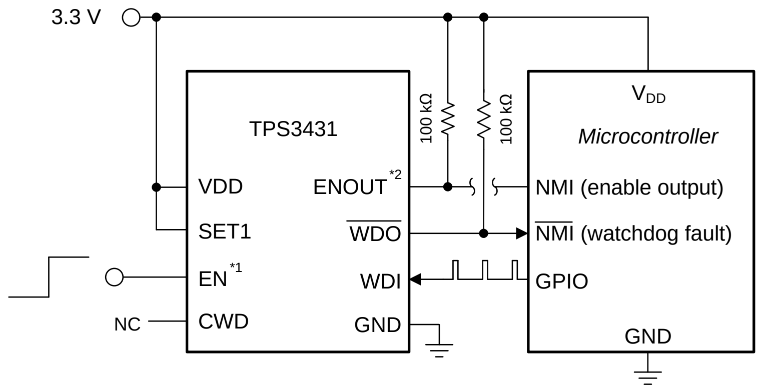
INPUT		WATCHDOG TIMEOUT WDT (t_{WD})			UNIT
CWD	SET1	MIN	TYP	MAX	
C_{CWD}	0	Watchdog disabled			
C_{CWD}	1	t_{WD} × 0.85	t_{WD} 公式 1	t_{WD} × 1.15	ms

表 4. t_{WD} Values for Common Ideal Capacitor Values

C_{CWD}	WATCHDOG TIMEOUT WDT (t_{WD})			UNIT
	MIN(1)	TYP	MAX(1)	
100 pF	53.33	62.74	72.15	ms
1 nF	112.5	132.4	152.3	ms
10 nF	704.7	829	953.4	ms
100 nF	6626	7795	8964	ms
1 µF	65837	77455	89073	ms

(1) The minimum and maximum values are calculated using an ideal capacitor.

8.2 Typical Application



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(1) EN can also be left floating and is internally pulled-up to VDD

(2) ENOUT can also be left floating or tied to WDO

图 11. Monitoring a Microcontroller with Standard Watchdog Timer

8.2.1 Design 1 Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Output logic voltage	3.3V Open-Drain	3.3V Open-Drain
Watchdog Timeout	Leave CWD disconnected: 1.6 seconds (typical)	$t_{WD(min)}$ = 1360 ms, $t_{WD(TYP)}$ = 1600 ms, $t_{WD(max)}$ = 1840 ms
Maximum device current consumption	35 µA	33 µA when WDO is asserted

8.2.2 Detailed Design 1 Procedure

8.2.2.1 Calculating WDO Pullup Resistor Design 1

The TPS3431 uses an open-drain configuration for the WDO circuit, as shown in 图 12. When the internal MOSFET is off, the external pull-up resistor pulls the drain of the transistor to VDD and when the MOSFET is turned on, the MOSFET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below the maximum value.

To choose the proper pull-up resistor, there are three key specifications to keep in mind: the pull-up voltage (V_{PU}), the recommended maximum WDO pin current ($I_{\overline{WDO}}$), and V_{OL}.

The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with $I_{\overline{WDO}}$ kept below 10 mA. For this example, with a V_{PU} of 3.3 V, a resistor must be chosen to keep $I_{\overline{WDO}}$ below 35 µA because this value is the maximum consumption current allowed. To ensure this specification is met, a pull-up resistor value of 100 kΩ was selected, which sinks a maximum of 33 µA when WDO is asserted.

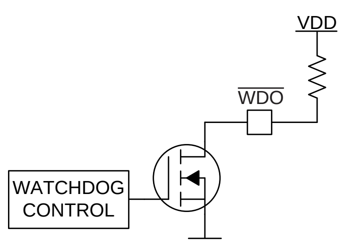


图 12. WDO Open-Drain Configuration

8.2.2.2 Setting the Watchdog Design 1

As illustrated in 图 10 there are three options for setting the watchdog timer. The design specifications in this application allow for a factory-programmed timing option by leaving CWD floating. To ensure proper functionality, a falling edge must be issued before $t_{WD(min)}$ with is set for 1.36 seconds when CWD is not connected. 图 17 illustrates that a WDI signal with a period of 1 second keeps $\overline{\text{WDO}}$ from asserting.

图 13 shows $\overline{\text{WDO}}$ asserting when the WDI signal has a period longer than $t_{WD(max)}$ which is 1.84 seconds when CWD is not connected. 图 14 shows a watchdog fault caused by missing WDI pulse followed by correct timing WDI pulses to deactivate $\overline{\text{WDO}}$.

8.2.3 Application Curves Design 1

Unless otherwise stated, application curves were taken at T_A = 25°C.

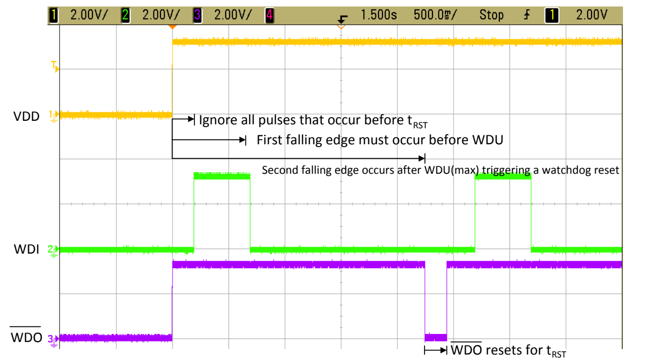


图 13. $\overline{\text{WDO}}$ Fault Caused by WDI Pulse Arriving Too Late (After $t_{WD(max)}$)

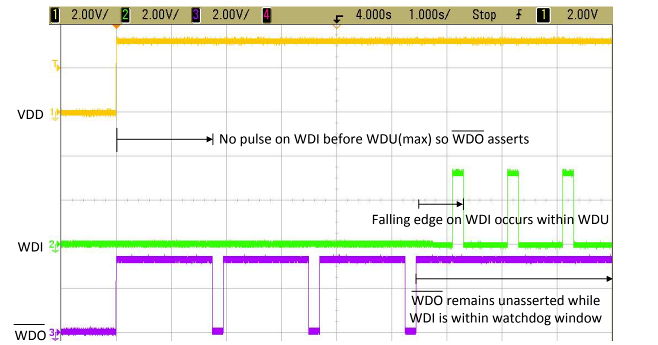


图 14. $\overline{\text{WDO}}$ Fault Caused by missing WDI Pulses Followed by Correct Timing WDI Pulses

8.3 Programmable Application

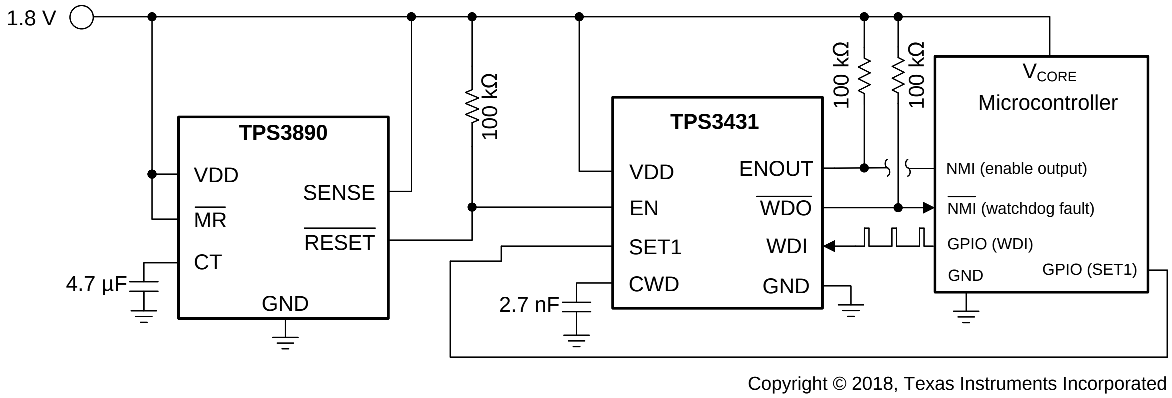


图 15. Monitoring the Supply Voltage and Watchdog Supervision of a Microcontroller

8.3.1 Design 2 Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog disable for initialization period	Watchdog must remain disabled for 5 seconds until logic enables the watchdog timer	5.02 seconds (typ)
Programmable disable feature	Microcontroller controls SET1 on TPS3431 via a GPIO	The Microcontroller can disable TPS3431 via SET1 and thus disable the watchdog for any reason.
Output logic voltage	1.8-V Open-Drain	1.8V Open-Drain
Monitored rail (TPS3890)	1.8 V with a 5% threshold and 1% accuracy	Worst-case V_{ITN} = 1.714 V – 4.7%
Watchdog timeout (TPS3431)	265 ms typical	$t_{WD(min)}$ = 213 ms, $t_{WD(TYP)}$ = 264 ms, $t_{WD(max)}$ = 319 ms
Maximum device current consumption	50 µA	37 µA when $\overline{WDO}$ is asserted

8.3.2 Detailed Design 2 Procedure

8.3.2.1 Calculating $\overline{WDO}$ Pullup Resistor Design 2

The TPS3431 uses an open-drain configuration for the $\overline{WDO}$ circuit. When the internal MOSFET is off, the external pull-up resistor pulls the drain of the transistor to VDD and when the MOSFET is turned on, the MOSFET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below the maximum value. To choose the proper pull-up resistor, there are three key specifications to keep in mind: the pull-up voltage (V_{PU}), the recommended maximum $\overline{WDO}$ pin current ($I_{\overline{WDO}}$), and V_{OL}. The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with $I_{\overline{WDO}}$ kept below 10 mA. For this example, with a V_{PU} of 1.8 V, a resistor must be chosen to keep $I_{\overline{WDO}}$ below 50 µA because this value is the maximum consumption current allowed. To ensure this specification is met, a pull-up resistor value of 100 kΩ was selected, which sinks a maximum of 18 µA when $\overline{WDO}$ is asserted.

8.3.2.2 Setting the Watchdog Design 2

As illustrated in 图 10 there are three options for setting the watchdog timer. The design specifications in this application require the programmable timing option (external capacitor connected to CWD). When a capacitor is connected to the CWD pin, the watchdog timer is governed by 公式 1. This equation estimation is only valid for ideal capacitors and any temperature or voltage derating must be accounted for separately.

$$C_{CWD}\ (nF) = (t_{WD}(ms) - 55) / 77.4 = (265 - 55) / 77.4 = 2.71\ nF \quad (2)$$

The nearest standard capacitor value is 2.7 nF. Selecting 2.7 nF for the C_{CWD} capacitor gives the following minimum and maximum timing parameters:

$$t_{WD(MIN)} = 0.85 \times t_{WD(TYP)} = 0.85 \times (77.4 \times 2.7 + 55) = 224.383\ ms \quad (3)$$

$$t_{WD(MAX)} = 1.15 \times t_{WD(TYP)} = 1.15 \times (77.4 \times 2.7 + 55) = 303.577\ ms \quad (4)$$

Capacitor tolerance also influences $t_{WD(MIN)}$ and $t_{WD(MAX)}$. Select a ceramic COG dielectric capacitor for high accuracy. For 2.7 nF, COG capacitors are readily available with 5% tolerances. This selection results in a 5% decrease in $t_{WD(MIN)}$ and a 5% increase in $t_{WD(MAX)}$, giving 213.16 ms and 318.75 ms, respectively. To ensure proper functionality, a falling edge must be issued before $t_{WD(min)}$. 图 17 illustrates that a WDI signal with a period of 260 ms keeps WDO from asserting.

8.3.2.3 Watchdog Disabled During Initialization Period Design 2

The watchdog is often needed to be disabled during startup to allow for an initialization period. When the initialization period is over, the watchdog timer is turned back on to allow the microcontroller to be monitored by the TPS3431. To achieve this setup, EN on TPS3431 is controlled by TPS3890 supervisor. In this application, the TPS3890 was chosen to monitor VDD as well, which means that the RESET on the TPS3890 stays low until V_{DD} rises above V_{ITN}. When VDD comes up, the delay time can be adjusted through the CT capacitor on the TPS3890. With this approach, the RESET delay can be adjusted from a minimum of 25 µs to a maximum of 30 seconds. For this design, a typical delay of 5 seconds is needed before the watchdog timer is enabled. The CT capacitor calculation (see the TPS3890 data sheet) yields an ideal capacitance of 4.67 µF, giving a closest standard ceramic capacitor value of 4.7 µF. When connecting a 4.7 µF capacitor from CT to GND, the typical delay time is 5 seconds. 图 16 shows that when the watchdog is disabled, the WDO output remains high. However when SET1 goes high and there is no WDI signal, WDO begins to assert. See the TPS3890 datasheet for detailed information on the TPS3890. The ENOUT pin on the TPS3431 reflects the status of the EN pin and can be connected to the microcontroller for monitoring or can be left floating if not being used. When the TPS3431 is disabled, ENOUT is logic low and WDO is logic high so the user can also tie ENOUT to WDO to force WDO to logic low when TPS3431 is disabled.

8.3.2.4 Programmable Disable Feature Design 2

The watchdog is often needed to be disabled during operation to prevent false watchdog faults. When the watchdog is disabled, all pulses or lack of pulses on WDI are ignored and WDO is high impedance as shown in 图 18. When the watchdog is re-enabled, the watchdog timer is turned back on after a watchdog start-up delay of 150 µs to allow the microcontroller to be monitored by the TPS3431. To achieve this setup, SET1 on TPS3431 is controlled by a GPIO on the microcontroller and must be logic high to enable to watchdog. To disable the watchdog, the microcontroller sets the GPIO connected to SET1 to logic low. To re-enable the watchdog, the microcontroller sets the GPIO connected to SET1 back to logic high. This configuration is useful when another device or signal is already using the EN pin on TPS3431, and a programmable disable feature with minimal delay upon enable is still required. When the watchdog is disabled using SET1 instead of EN, ENOUT remains unaffected which is useful when needing to disable the watchdog but not causing another device connected to ENOUT to be disabled.

8.3.3 Application Curves Design 2

Unless otherwise stated, application curves were taken at T_A = 25°C.

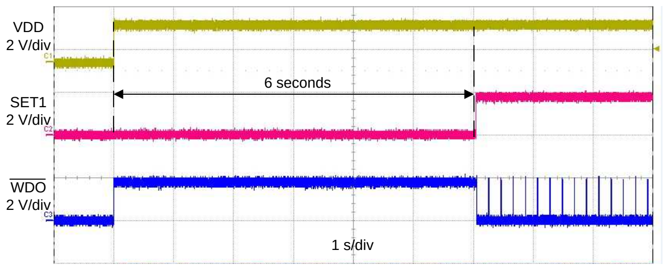


图 16. Startup Without a WDI Signal

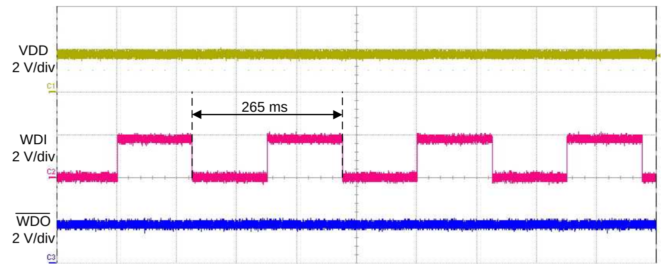


图 17. Typical WDI Signal

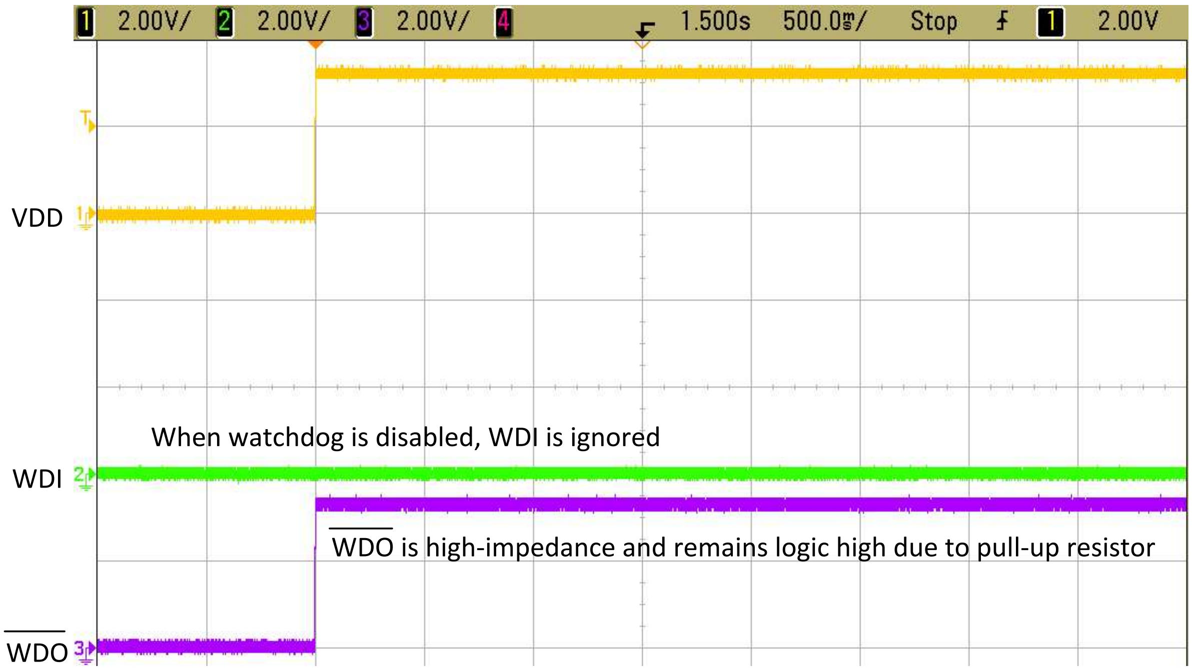


图 18. Watchdog Disabled With Missing WDI Pulse

9 Power Supply Recommendations

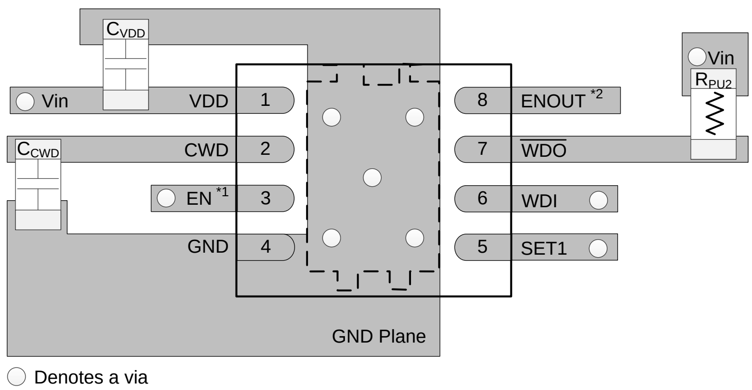
This device is designed to operate from an input supply with a voltage range between 1.8 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin.

10 Layout

10.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CWD} capacitor or pull-up resistor is used, place these components as close as possible to the CWD pin. If the CWD pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- Place the pull-up resistor on $\overline{\text{WDO}}$ as close to the pin as possible.

10.2 Layout Example



(1) EN can also be left floating and is internally pulled-up to VDD

(2) ENOUT can also be left floating or tied to $\overline{\text{WDO}}$

图 19. TPS3431 Recommended Layout

11 器件和文档支持

11.1 器件支持

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- *《TPS3890 延迟可编程的低静态电流、1% 精密监控器》*（文献编号：SLVSD65）
- *《TPS3431EVM-780 评估模块》*（文献编号：SBVU033）

11.3 接收文档更新通知

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3431SDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	431DD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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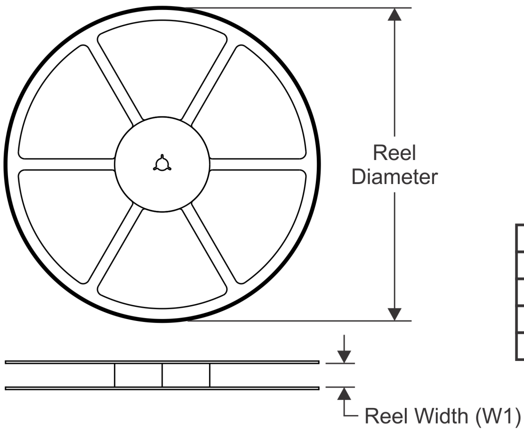
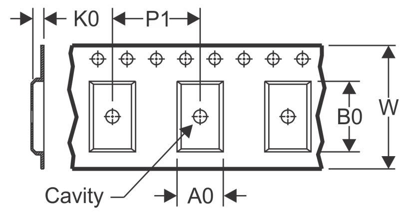
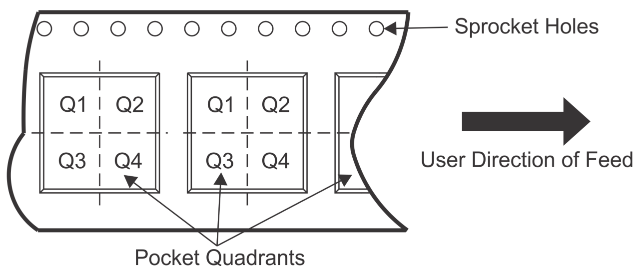
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

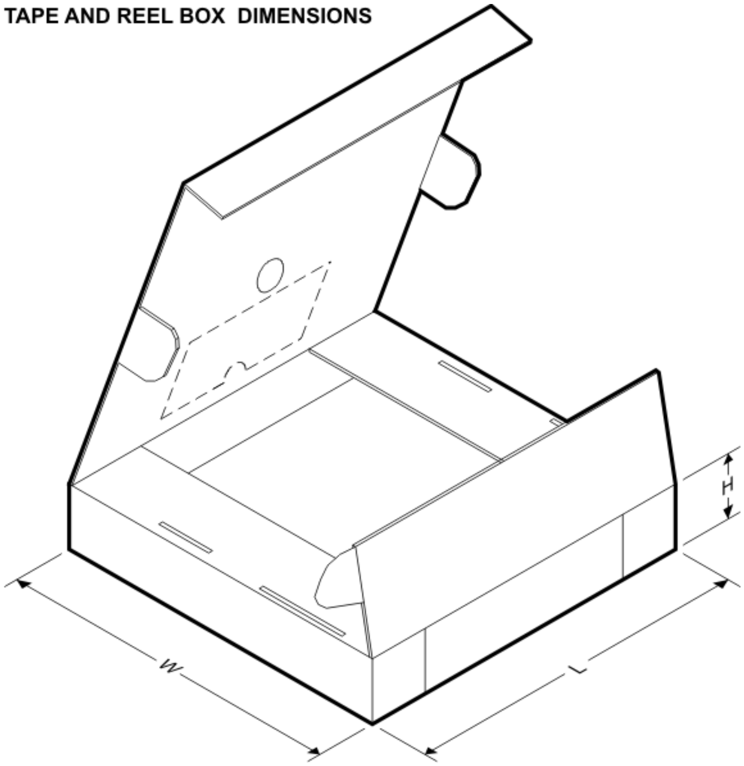
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3431SDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

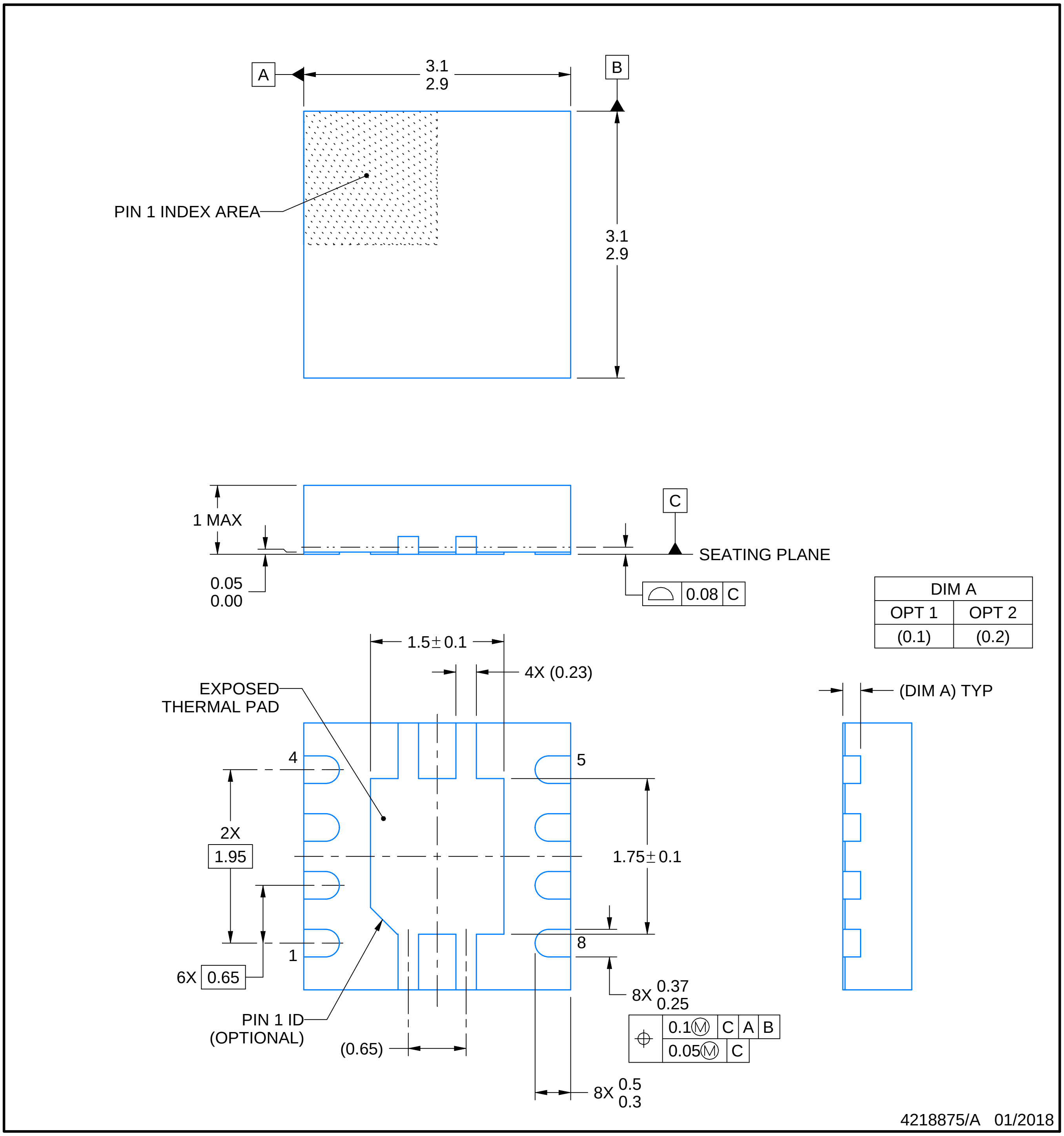
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

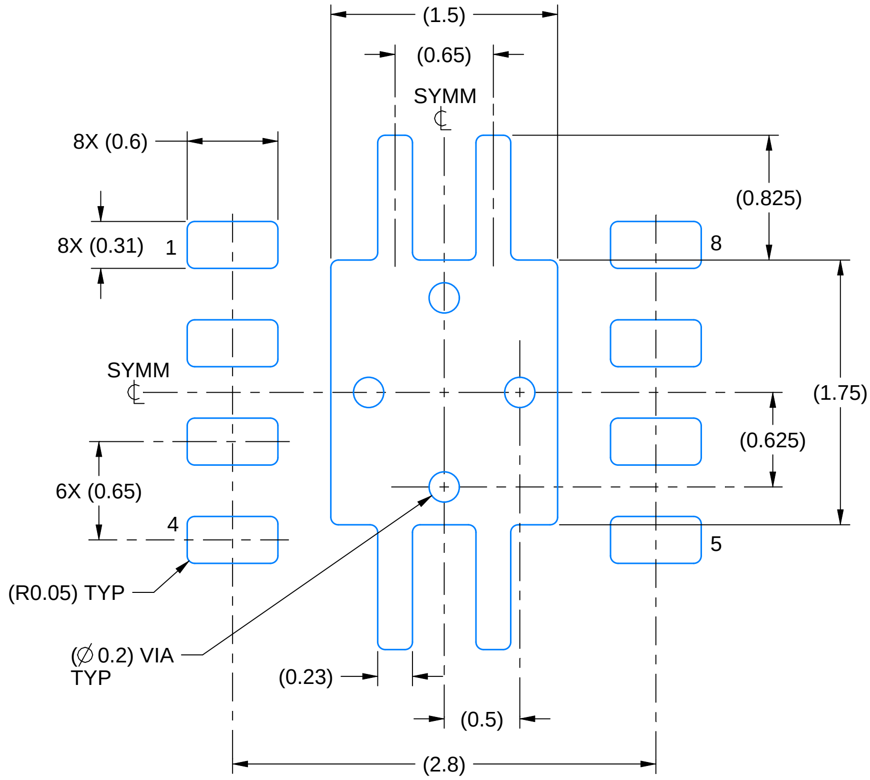
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3431SDRBR	SON	DRB	8	3000	367.0	367.0	35.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

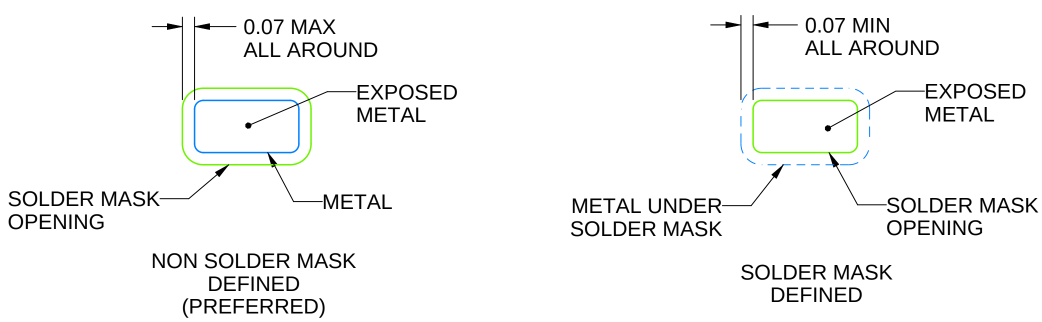


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

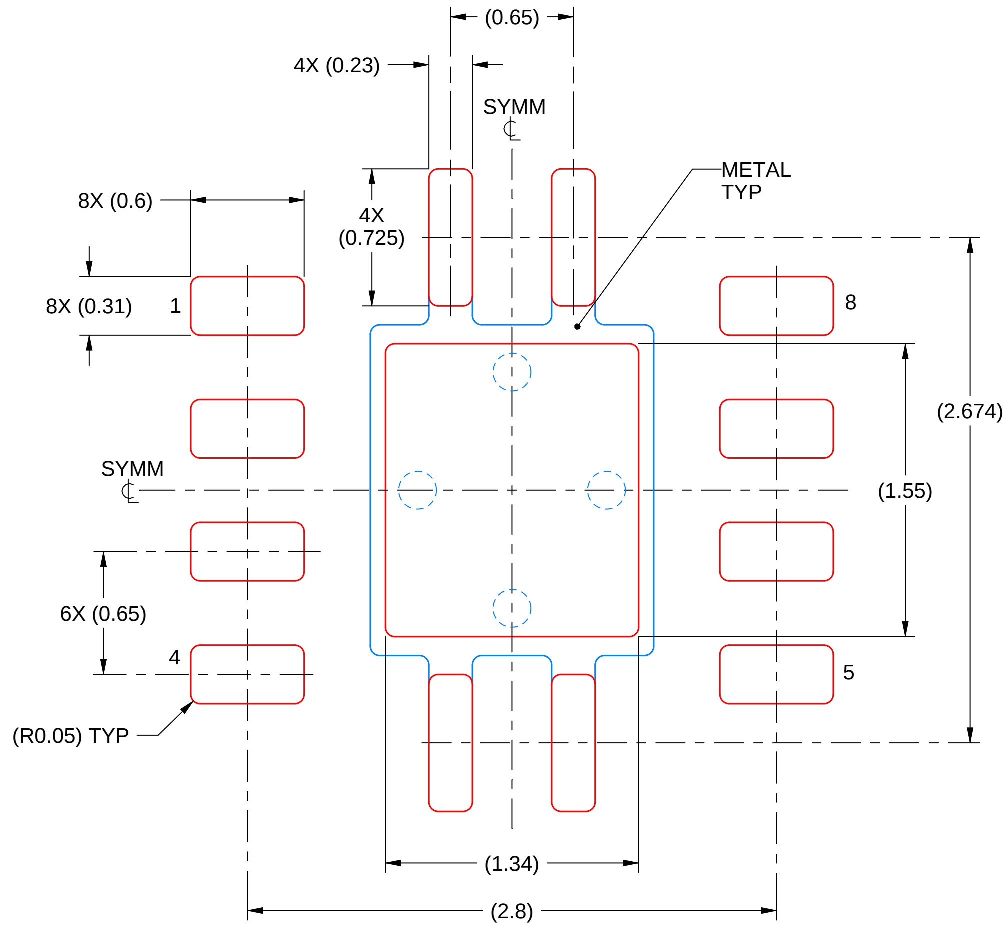


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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