低压双路 ½H 桥驱动器集成电路 (IC)

查询样片: DRV8839

特性

- 双路 **½H** 桥接电机驱动器
  - 驱动一个直流电机或者一个步进电机的绕组，或其它负载
  - 低金属氧化物半导体场效应晶体管 **(MOSFET)** 导通电阻：
    高侧 **+** 低侧 **(HS + LS) 280mΩ**
- **1.8A** 最大驱动电流
- 单独的电机和逻辑电源引脚：
  - **0V** 至 **11V** 电机运行电源电压范围
  - **1.8V** 至 **7V** 逻辑电源电压范围
- 独立的电机和逻辑电源引脚
- 单独的 **½H** 桥控制输入接口
- 具有 **120nA** 最大组合电源电流的低功耗睡眠模式
- **2mm x 3mm 12** 引脚超薄型小外形尺寸无引线 **(WSON)** 封装

应用范围

- 由电池供电的设备：
  - 数字单镜头反光 **(DSLR)** 镜头
  - 消费类产品
  - 玩具
  - 机器人技术
  - 摄像机
  - 医疗设备

说明

DRV8839 为照相机、消费类产品、玩具和其它 低压或电池供电类应用提供多用途功率驱动器解决方案。此器件有两个独立的 ½H 桥驱动器，并且能够驱动一个直流电机或者一个步进电机的绕组，以及其它诸如螺线管等其它器件。 使用 N 通道功率 MOSFET 的输出级被配置为 ½H 桥。 一个内部电荷泵生成所需的栅极驱动电压。

DRV8839 能够提供高达 1.8A 的输出电流。 它在 0V 至 11V 的电机电源电压范围，以及 1.8V 至 7V 的器件电源电压范围内运行。

DRV8839 具有针对每个 ½H 桥的单独输入和启用引脚，这样可实现对每个输出的单独控制。

内部关断功能支持过流保护、短路保护、欠压闭锁以及过温保护。

DRV8839 采用具有 PowerPAD™ 的 12 引脚 2mm x 3mm WSON 封装（环保型：符合 RoHS 标准且不含 Sb/Br）。

ORDERING INFORMATION(1)

PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
PowerPAD™ (WSON) - DSS	Reel of 3000	DRV8839DSSR	8839

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM

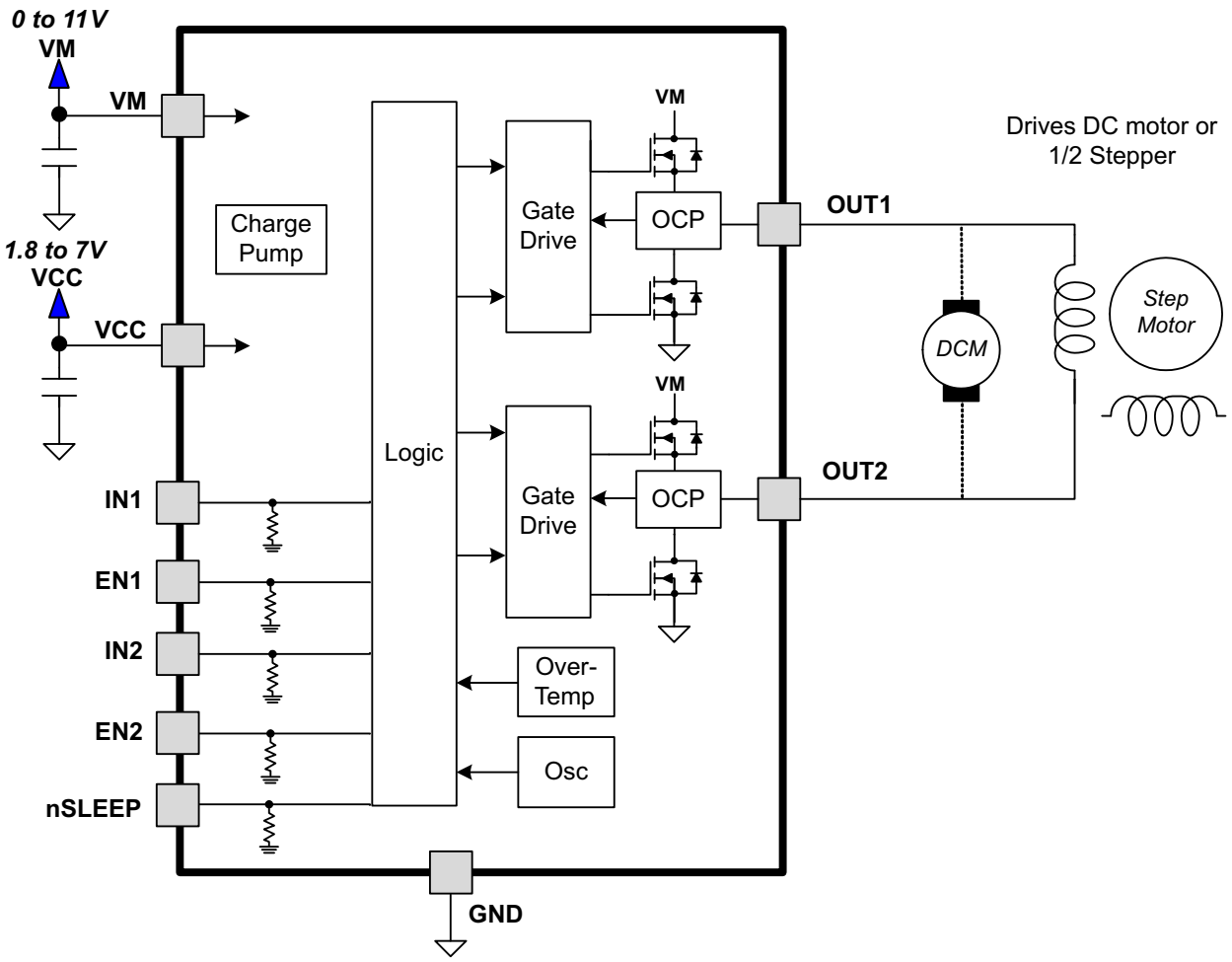
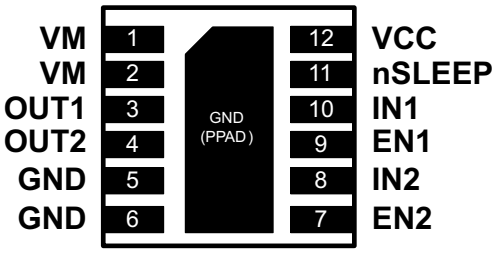


Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	5, 6	-	Device ground	
VM	1, 2	-	Motor supply	Bypass to GND with a 0.1-µF, 16-V ceramic capacitor.
VCC	12	-	Device supply	Bypass to GND with a 0.1-µF, 6.3-V ceramic capacitor.
CONTROL				
nSLEEP	11	I	Sleep mode input	Logic low puts device in low-power sleep mode Logic high for normal operation Internal pulldown resistor
IN1	10	I	Input 1	Logic input controls OUT1 Internal pulldown resistor
EN1	9	I	Enable 1	Logic high enables OUT1 Internal pulldown resistor
IN2	8	I	Input 2	Logic input controls OUT2 Internal pulldown resistor
EN2	7	I	Enable 2	Logic high enables OUT2 Internal pulldown resistor
OUTPUT				
OUT1	3	O	Output 1	Connect to motor winding
OUT2	4	O	Output 2	
NO CONNECT				
NC	2, 5	-	No connection	No connection to these pins

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

DSS PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE	UNIT
VM	Power supply voltage range	-0.3 to 12	V
VCC	Power supply voltage range	-0.3 to 7	V
	Digital input pin voltage range	-0.5 to 7	V
	Peak motor drive output current	Internally limited	A
T_J	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8839 DSS 12 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	50.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	58	
θ_{JB}	Junction-to-board thermal resistance(4)	19.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	20	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	6.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device power supply voltage range	1.8		7	V
V_M	Motor power supply voltage range	0		11	V
I_{OUT}	H-bridge output current(1)	0		1.8	A
f_{PWM}	Externally applied PWM frequency	0		250	kHz
V_{IN}	Logic level input voltage	0		5.5	V

(1) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V (unless otherwise noted)

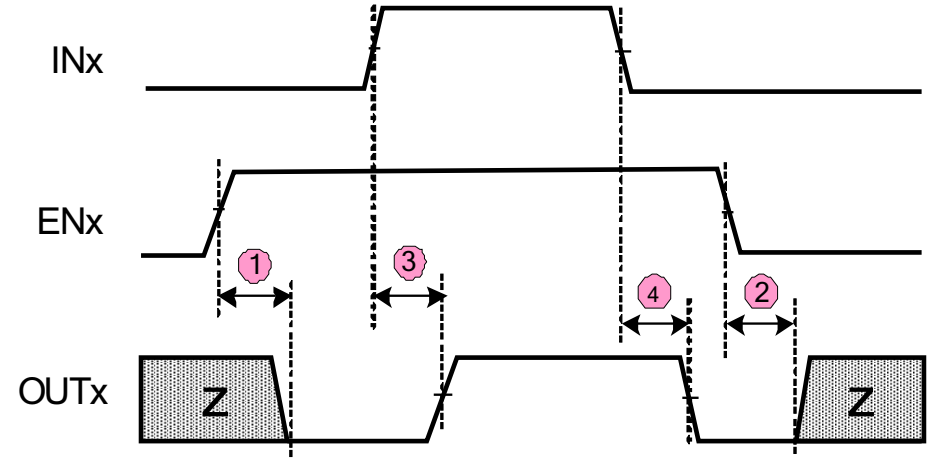
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	No PWM		40	100	µA
		50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0 V		30	95	nA
I_{VCC}	VCC operating supply current	No PWM		300	500	µA
		50 kHz PWM		0.7	1.5	mA
I_{CCQ}	VCC sleep mode supply current	nSLEEP = 0 V		5	25	nA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			1.8	V
		V_{CC} falling			1.7	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage		0.31 x V_{CC}	0.34 x V_{CC}		V
V_{IH}	Input high voltage			0.39 x V_{CC}	0.43 x V_{CC}	V
V_{HYS}	Input hysteresis			0.08 x V_{CC}		V
I_{IL}	Input low current	V_{IN} = 0	-5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS + LS FET on resistance	I_O = 800 mA, T_J = 25°C		280	330	mΩ
I_{OFF}	Off-state leakage current				±200	nA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{OCR}	Overcurrent protection retry time			1		ms
t_{DEAD}	Output dead time			100		ns
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

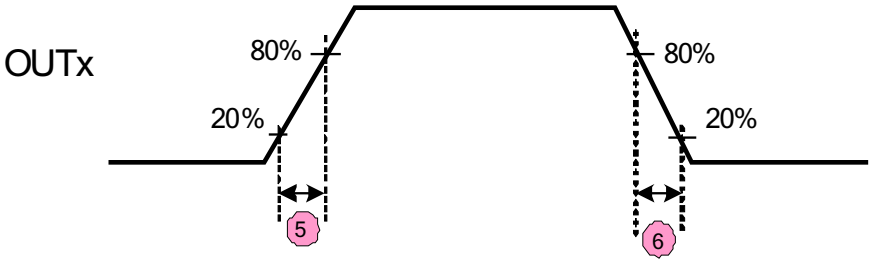
TIMING REQUIREMENTS(1)

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V, R_L = 20 Ω

NO.	PARAMETER	CONDITIONS	MIN	MAX	UNIT
1	t_1	Output enable time		120	ns
2	t_2	Output disable time		120	ns
3	t_3	Delay time, INx high to OUTx high		120	ns
4	t_4	Delay time, INx low to OUTx low		120	ns
5	t_5	Output rise time	50	150	ns
6	t_6	Output fall time	50	150	ns

(1) Not production tested – ensured by design





FUNCTIONAL DESCRIPTION

Bridge Control

The DRV8839 is controlled using separate enable and input pins for each ½-H-bridge.

The following table shows the logic for the DRV8839:

ENx	INx	OUTx
0	X	Z
1	0	L
1	1	H

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV8839 will enter a low-power sleep mode. In this state all unnecessary internal circuitry is powered down.

Power Supplies and Input Pins

The input pins may be driven within their recommended operating conditions with or without the VCC and VM power supplies present. No leakage current path will exist to the supply. There is a weak pulldown resistor (approximately 100 kΩ) to ground on each input pin.

VCC and VM may be applied and removed in any order. When VCC is removed, the device will enter a low power state and draw very little current from VM. If the supply voltage is between 1.8 V and 7 V, VCC and VM may be connected together.

The VM voltage supply does not have any undervoltage lockout protection (UVLO), so as long as VCC > 1.8 V, the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

Protection Circuits

The DRV8839 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled. After approximately 1 ms, the bridge will be re-enabled automatically.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled and internal logic is reset. Operation resumes when VCC rises above the UVLO threshold.

APPLICATIONS INFORMATION

Motor Connections

If a single DC motor is connected to the DRV8839, it is connected between the OUT1 and OUT2 pins as shown below:

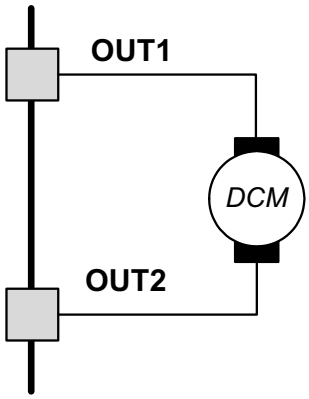


Figure 1. Single DC Motor Connection

Motor operation is controlled as follows:

EN1	EN2	IN1	IN2	OUT1	OUT2	MOTOR OPERATION
0	X	X	X	Z	See (1)	Off (coast)
X	0	X	X	See (2)	Z	Off (coast)
1	1	0	0	L	L	Brake
1	1	0	1	L	H	Reverse
1	1	1	0	H	L	Forward
1	1	1	1	H	H	Brake

(1) State depends on EN2 and IN2, but does not affect motor operation because OUT1 is tri-stated.
(2) State depends on EN1 and IN1, but does not affect motor operation because OUT2 is tri-stated.

Two DC motors may be connected to the DRV8839. In this mode, it is not possible to reverse the direction of the motors; they will turn only in one direction. The connections are shown below:

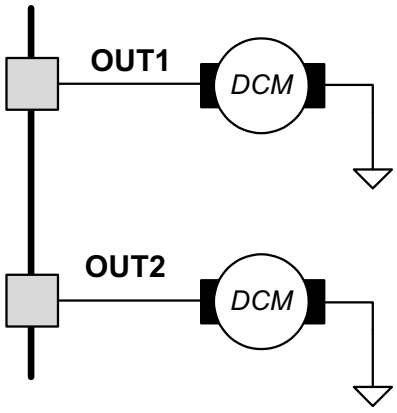


Figure 2. Dual DC Motor Connection

Motor operation is controlled as follows:

ENx	INx	OUTx	MOTOR OPERATION
0	X	Z	Off (coast)
1	0	L	Brake
1	1	H	Forward

THERMAL INFORMATION

Thermal Protection

The DRV8839 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8839 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (1)$$

Where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of the HS plus LS FETs, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

修订历史记录

Changes from Original (January 2013) to Revision A **Page**

- Changed 特性着重号 1
- Changed 说明部分中的电机电源电压范围 1
- Changed Motor power supply voltage range in RECOMMENDED OPERATING CONDITIONS 4
- Added t_{OCR} and t_{DEAD} parameters to ELECTRICAL CHARACTERISTICS 5
- Added paragraph to Power Supplies and Input Pins section 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8839DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8839	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

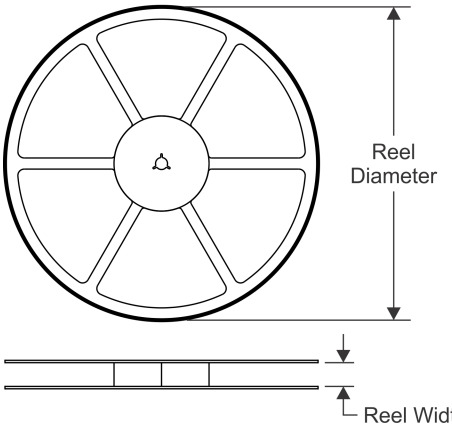
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

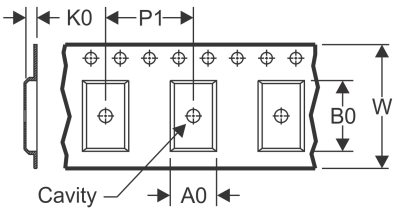
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

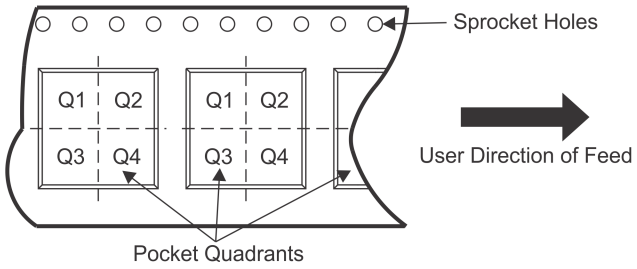


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

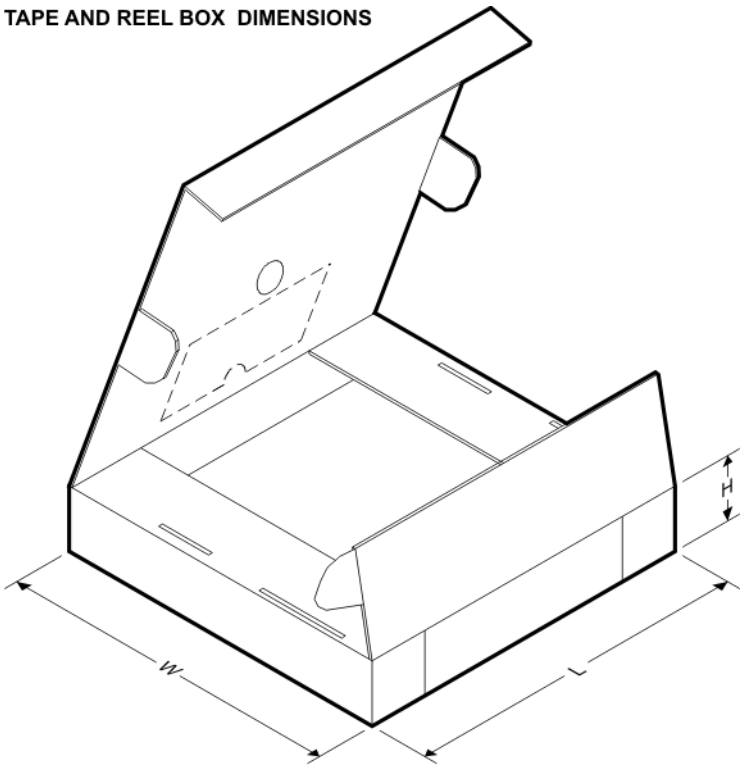
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8839DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



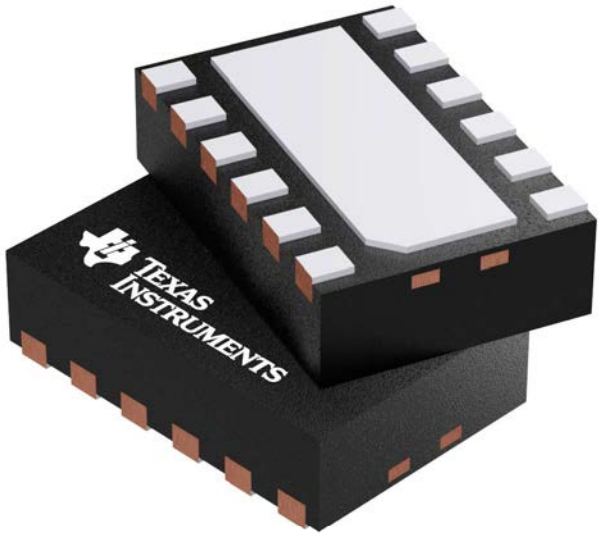
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8839DSSR	WSON	DSS	12	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DSS 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



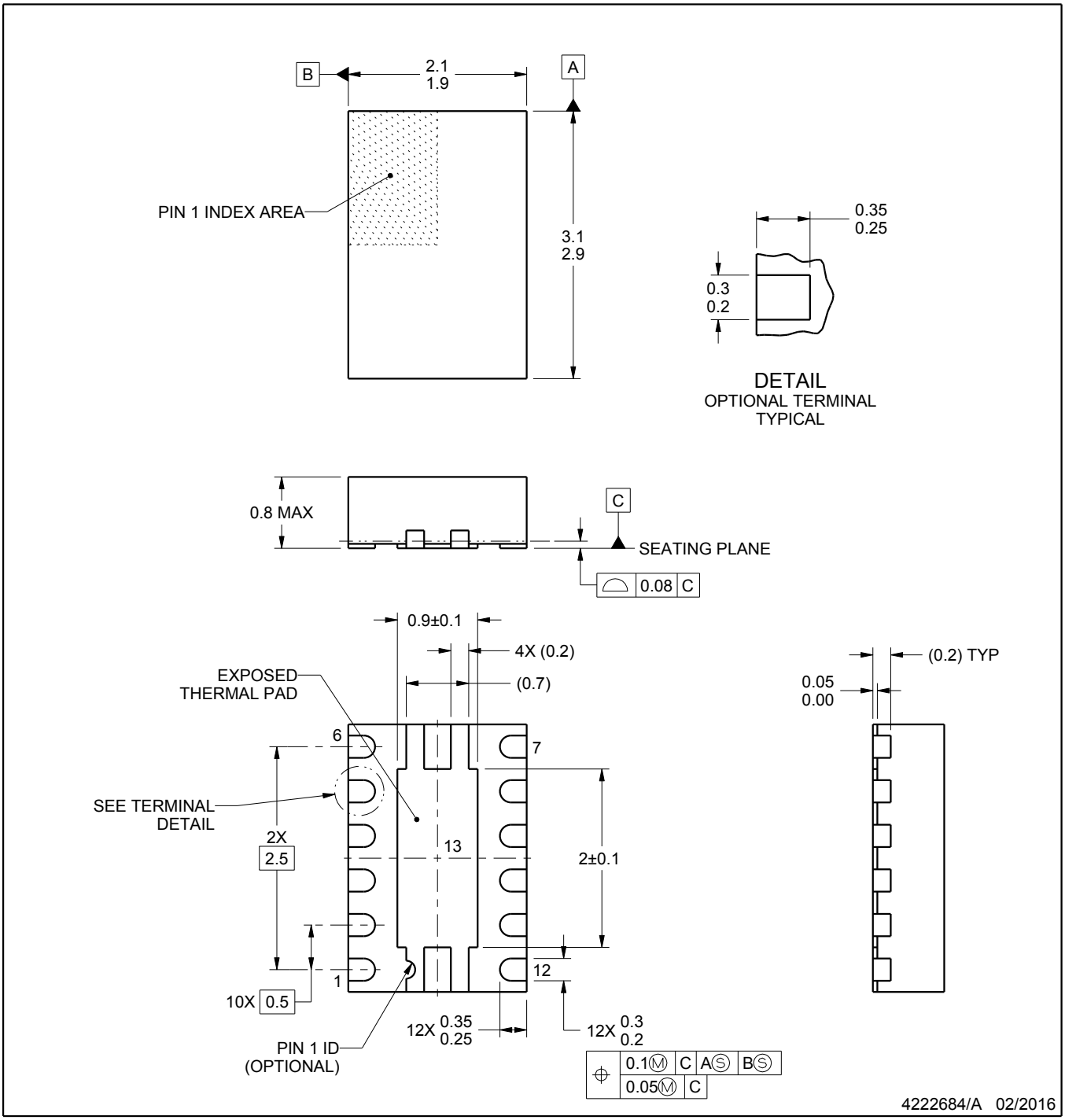
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSS0012A

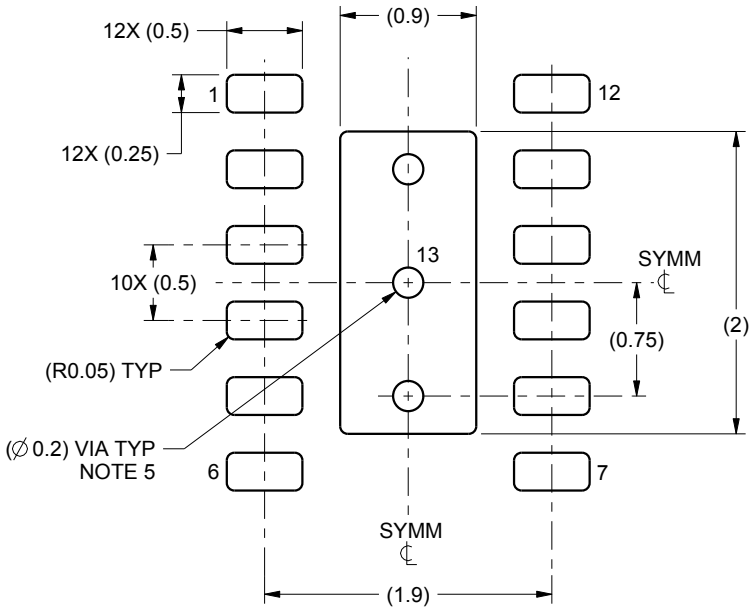
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

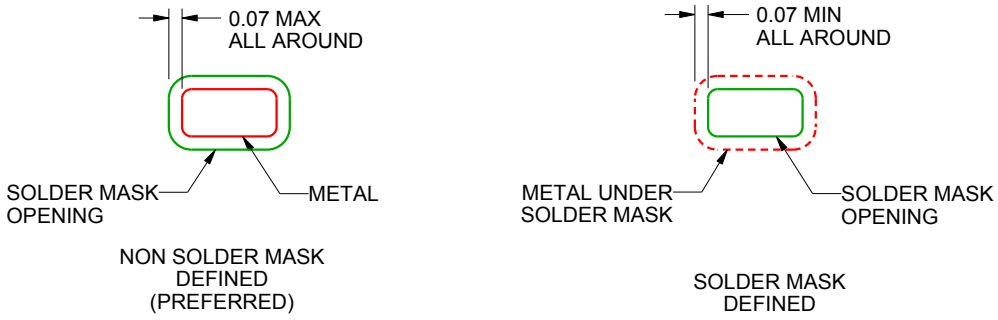


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

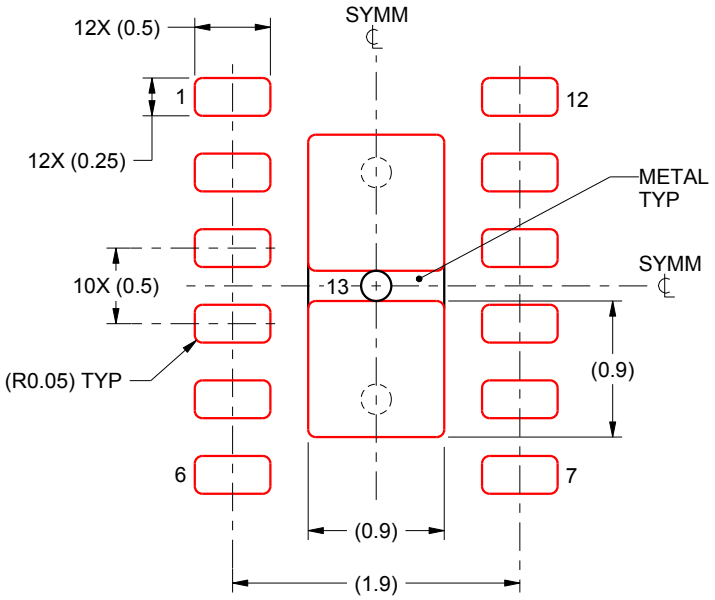


SOLDER MASK DETAILS

4222684/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown. It is recommended that vias located under solder paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222684/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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