# DRV8860 8 通道串行接口低边驱动器

## 1 特性

- 8 通道受保护低边驱动器
  - 8 个具有过流保护功能的 NMOS 场效应晶体管 (FET)
  - 集成型感应集流二极管
  - 串行接口
  - 开路/短路负载检测
  - 可配置 100% 占空比输出时间
  - 可配置脉宽调制 (PWM) 占空比
- 持续电流驱动能力
  - 560 mA（单通道打开）PW 和 PWP
  - 200 mA（八通道打开）PW
  - 330 mA（八通道打开）PWP
  - 支持并联配置
- 8V 至 38V 电源电压范围
- 数字输入滤波器
- 内部数据回读功能
- 保护和诊断特性
  - 过流保护 (OCP)
  - 开路负载检测 (OL)
  - 过热关断 (OTS)
  - 欠压闭锁 (UVLO)
  - 独立通道状态报告
  - 故障情况警报

## 2 应用范围

- 继电器、单极步进电机
- 螺线管，电磁驱动器
- 常见低边开关应用

## 3 说明

DRV8860 是一款 8 通道低边驱动器，此驱动器具有过流保护和开路/短路负载检测功能。 它具有内置的用来钳制由电感负载生成的关闭瞬态的二极管，可被用于驱动单极步进电机、直流电机、继电器、螺线管、或者其它负载。

DRV8860PWP 可提供最高 330mA（8 通道打开）的连续输出电流，DRV8860PW 则可提供最高 200mA（8 通道打开）的连续输出电流。 此电流驱动能力随着 PWM 占空比的降低而增加。 单一通道打开时能够驱动高达 560mA 的持续输出电流。 细节请参考*输出电流建议*部分。

提供了一个串口来控制 DRV8860 输出驱动器、配置内部设置寄存器以及读取每条通道的故障状态。 多个 DRV8860 器件可采用菊花链连在一起以共同使用一个单一串口。 也可通过串口来配置加电时间和保持 PWM 占空比。 利用这些功能，可实现比传统的始终开启解决方案更低的运行温度。

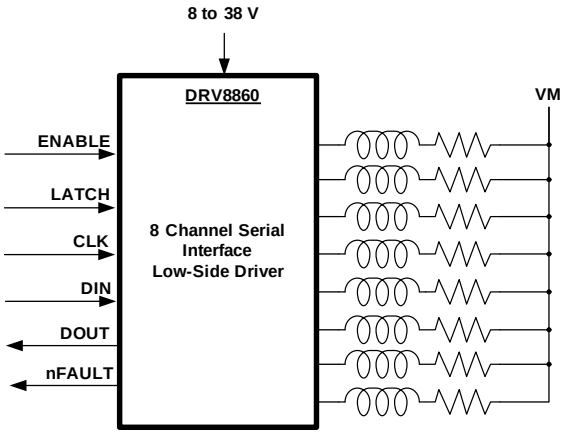
还提供用于过流保护、短路保护、欠压闭锁和过热保护的内部关断功能。 DRV8860 能够诊断开路负载情况。 每条通道的故障信息可由串口读取，并且有一个外部故障引脚指示。

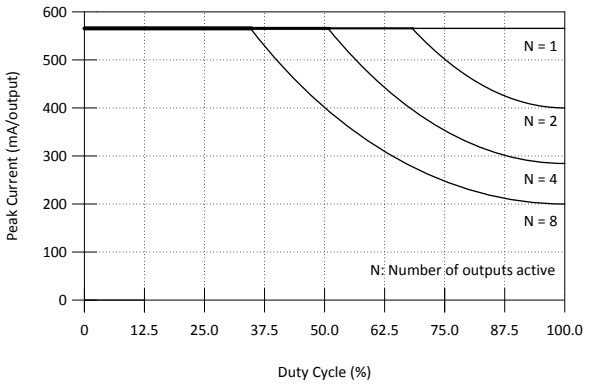
器件信息(1)

| 部件号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| DRV8860 | TSSOP (16) | 5.00mm x 6.40mm |
| | HTSSOP (16) | |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

## 4 简化电路原理图




PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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- Deleted the Example Output Configuration section. ..... 11
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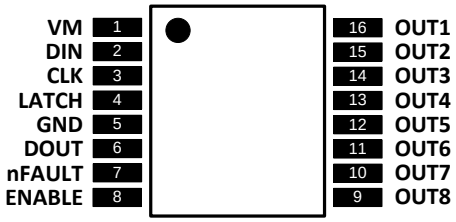
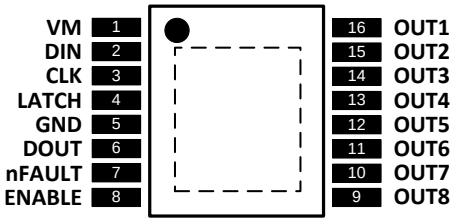
# 6 Pin Configuration and Functions

**PW (TSSOP) PACKAGE**
**(TOP VIEW)**




**PWP (HTSSOP) PACKAGE**
**(TOP VIEW)**




**Pin Functions**

| NAME | PIN | I/O(1) | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|
| GND | 5 | — | Device ground | All pins must be connected to ground |
| VM | 1 | — | Motor power supply | Connect to motor supply voltage. Bypass to GND with a 0.1 µF ceramic capacitor plus a 10 µF electrolytic capacitor. |
| ENABLE | 8 | I | Output stage enable control input | Logic high to enable outputs, logic low to disable outputs. Internal logic and registers can be read and written to when ENABLE is logic low. Internal pulldown. |
| LATCH | 4 | I | Serial latch signal | Refer to serial communication waveforms. Internal pulldown. |
| CLK | 3 | I | Serial clock input | Rising edge clocks data into part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown. |
| DIN | 2 | I | Serial data input | Serial data input from controller. Internal pulldown. |
| DOUT | 6 | O | Serial data output | Serial data output to controller. Open-drain output with internal pullup. |
| nFAULT | 7 | OD | Fault | Logic low when in fault condition. Open-drain output requires external pullup. Faults: OCP, OL, OTS, UVLO |
| OUT1 | 16 | O | Low-side output 1 | NFET output driver. Connect external load between this pin and VM |
| OUT2 | 15 | O | Low-side output 2 | NFET output driver. Connect external load between this pin and VM |
| OUT3 | 14 | O | Low-side output 3 | NFET output driver. Connect external load between this pin and VM |
| OUT4 | 13 | O | Low-side output 4 | NFET output driver. Connect external load between this pin and VM |
| OUT5 | 12 | O | Low-side output 5 | NFET output driver. Connect external load between this pin and VM |
| OUT6 | 11 | O | Low-side output 6 | NFET output driver. Connect external load between this pin and VM |
| OUT7 | 10 | O | Low-side output 7 | NFET output driver. Connect external load between this pin and VM |
| OUT8 | 9 | O | Low-side output 8 | NFET output driver. Connect external load between this pin and VM |

(1) Directions: I = input, O = output, OD = open-drain output

**Table 1. External Components**

| COMPONENT | PIN 1 | PIN 2 | RECOMMENDED |
|---|---|---|---|
| $C_{(VM1)}$ | VM | GND | 0.1 µF ceramic capacitor rated for VM |
| | | | 10 µF electrolytic capacitor rated for VM |
| $R_{(nFAULT)}$ | V3P3(1) | nFAULT | > 4.7 kΩ |

(1) V3P3 is not a pin on the DRV8860, but a V3P3 supply voltage pullup is required for open-drain output nFAULT.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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power supply voltage range | VM | –0.3 | 40 | V |
| Digital input pin current range | ENABLE, LATCH, CLK, DIN | 0 | 20 | mA |
| Digital output pin voltage range | DOUT, nFAULT | –0.5 | 7 | V |
| Digital output pin current | DOUT, nFAULT | –0.5 | 7 | V |
| Output voltage range | OUTx | –0.3 | 40 | V |
| Output current range | OUTx | Internally limited | | A |
| Operating virtual junction temperature range, $T_J$ | | –40 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –60 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | –2 | 2 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | –500 | 500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VM | Motor power supply voltage range | 8 | | 38 | V |
| $I_{OUT}$ | Low-side driver current capability | | | 560 | mA |
| $T_A$ | Operating ambient temperature range | –40 | | 85 | °C |

## 7.4 Thermal Information(1)

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC | | TSSOP | HTSSOP | UNIT |
|---|---|---|---|---|
| | | PW (16 PINS) | PWP (16 PINS) | |
| $\Theta_{JA}$ | Junction-to-ambient thermal resistance | 103 | 40.9 | °C/W |
| $R_{\theta JC(TOP)}$ | Junction-to-case (top) thermal resistance | 37.9 | 28.5 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 48 | 23.2 | |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 3 | 0.9 | |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 47.4 | 23.0 | |
| $R_{\theta JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance | N/A | 3.0 | |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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## 7.5 Electrical Characteristics

$T_A$ = 25°C, over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $I_{(VM)}$ | VM operating supply current | VM = 24 V | | 3 | | mA |
| $V_{(UVLO)}$ | VM undervoltage lockout voltage | VM rising | | | 8.2 | V |
| **LOGIC-LEVEL INPUTS (DIN, CLK, LATCH, ENABLE)** | | | | | | |
| $V_{IL}$ | Input low voltage | | 0 | | 0.7 | V |
| $V_{IH}$ | Input high voltage | | 1.5 | | 5.3 | V |
| $V_{HYS}$ | Input hysteresis | | 100 | | | mV |
| $I_{IL}$ | Input low current | $V_{IN}$ = 0 | –20 | | 20 | µA |
| $I_{IH}$ | Input high current | $V_{IN}$ = 3.3 V | | | 100 | µA |
| $R_{PD}$ | Input pulldown resistance | | | 100 | | kΩ |
| **nFAULT, DOUT OUTPUTS (OPEN-DRAIN OUTPUTS)** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_O$ = 5 mA | | | 0.5 | V |
| $I_{OH}$ | Output high leakage current | $V_O$ = 3.3 V, nFAULT | –1 | | 1 | µA |
| $R_{PU}$ | Input pullup resistance | DOUT only (Pull up to internal 5.7 V) | | 1.4 | | kΩ |
| **LOW-SIDE FET DRIVERS** | | | | | | |
| $R_{ds(on)}$ | FET on resistance | VM = 24 V, $I_O$ = 150 mA, $T_J$ = 25°C | | 1.5 | | Ω |
| | | VM = 24 V, $I_O$ = 150 mA, $T_J$ = 85°C | | 1.8 | | |
| $I_{OFF}$ | Off-state leakage current | VM = 24 V, $T_J$ = 25°C | 0 | 30 | | µA |
| **HIGH-SIDE FREE-WHEELING DIODES** | | | | | | |
| $V_F$ | Diode forward voltage | VM = 2 4V, $I_O$ = 150 mA, $T_J$ = 25°C | | 0.9 | | V |
| **PROTECTION CIRCUITS** | | | | | | |
| $I_{OCP}$ | Overcurrent protection trip level | Each channel separately monitored | | 620 | | mA |
| $I_{OL}$ | Open load detect pull-down current | Each channel separately monitored | | 30 | | µA |
| $V_{OL}$ | Open load detect threshold voltage | Each channel separately monitored | | 1.2 | | V |
| $T_{TSD}$ | Thermal shutdown temperature | Die temperature | 150 | 160 | 180 | °C |
| $T_{HYS}$ | Thermal shutdown hysteresis | Die temperature | | 35 | | °C |
| **PWM CHOPPING FREQUENCY** | | | | | | |
| $f_{PWM}$ | PWM chopping frequency | Duty cycle is > 25% | 45 | 50 | 55 | kHz |
| | | Duty cycle is 25% | 22 | 25 | 28 | |
| | | Duty cycle is 12.5% | 11 | 12.5 | 14 | |

## 7.6 Timing Requirements

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PD}$ | Propagation delay | STEP to current change | | | 150 | ns |
| $t_R$ | Rise time | $I_O$ = 150 mA, VM = 24 V, resistive load | 50 | | 300 | ns |
| $t_F$ | Fall time | | 50 | | 300 | ns |
| $t_{OCP}$ | Overcurrent protection deglitch time | VM = 24 V | 2.7 | 3.5 | 3.85 | µs |
| $t_{OL}$ | Open load detect deglitch time | Each channel separately monitored | 14 | 17 | 20 | µs |


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## 7.7 Typical Characteristics

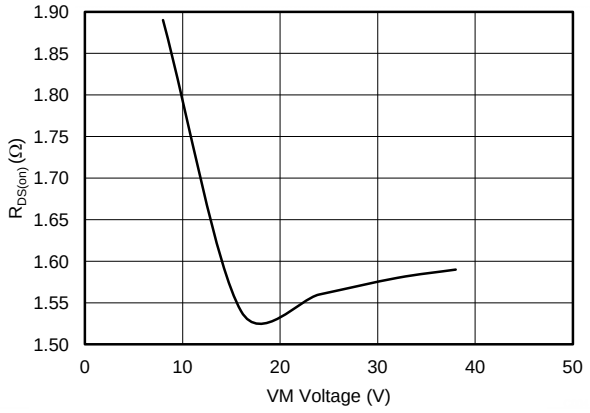


**Figure 1. Output ON Resistance**

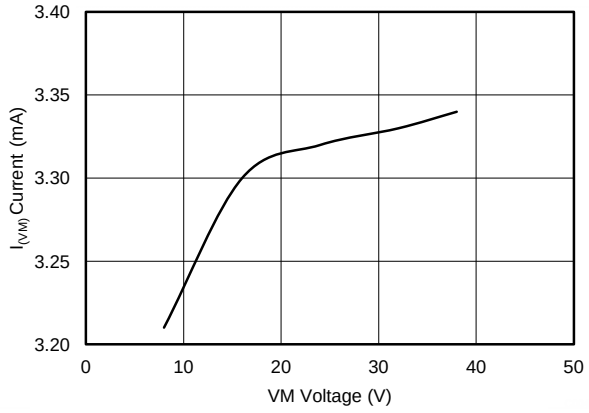


**Figure 2. VM Operating Supply Current**

# 8 Detailed Description

## 8.1 Overview

The DRV8860 is an integrated 8-channel low side driver with overcurrent protection and open/short detection. It has built-in diodes to clamp turn-off transients generated by inductive loads, and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

DRV8860 can supply up to 200 mA x 8 channel continuous output current. The current driving capability increases with lower PWM duty cycle. A single channel can deliver up to 560 mA continuous output current. Refer to the current capability table for details.

A serial interface is provided to control the DRV8860 output drivers, configure internal register settings, and read the fault status of each channel. Multiple DRV8860 devices can be daisy-chained together to use a single serial interface. Energizing-time and holding-PWM-duty cycle are configurable through the serial interface as well. These functions allow for cooler running than traditional always-on solutions.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, unde voltage lockout and over temperature. DRV8860 can diagnosis an open load condition. Fault information for each channel can be read out through serial interface and is indicated by an external fault pin.

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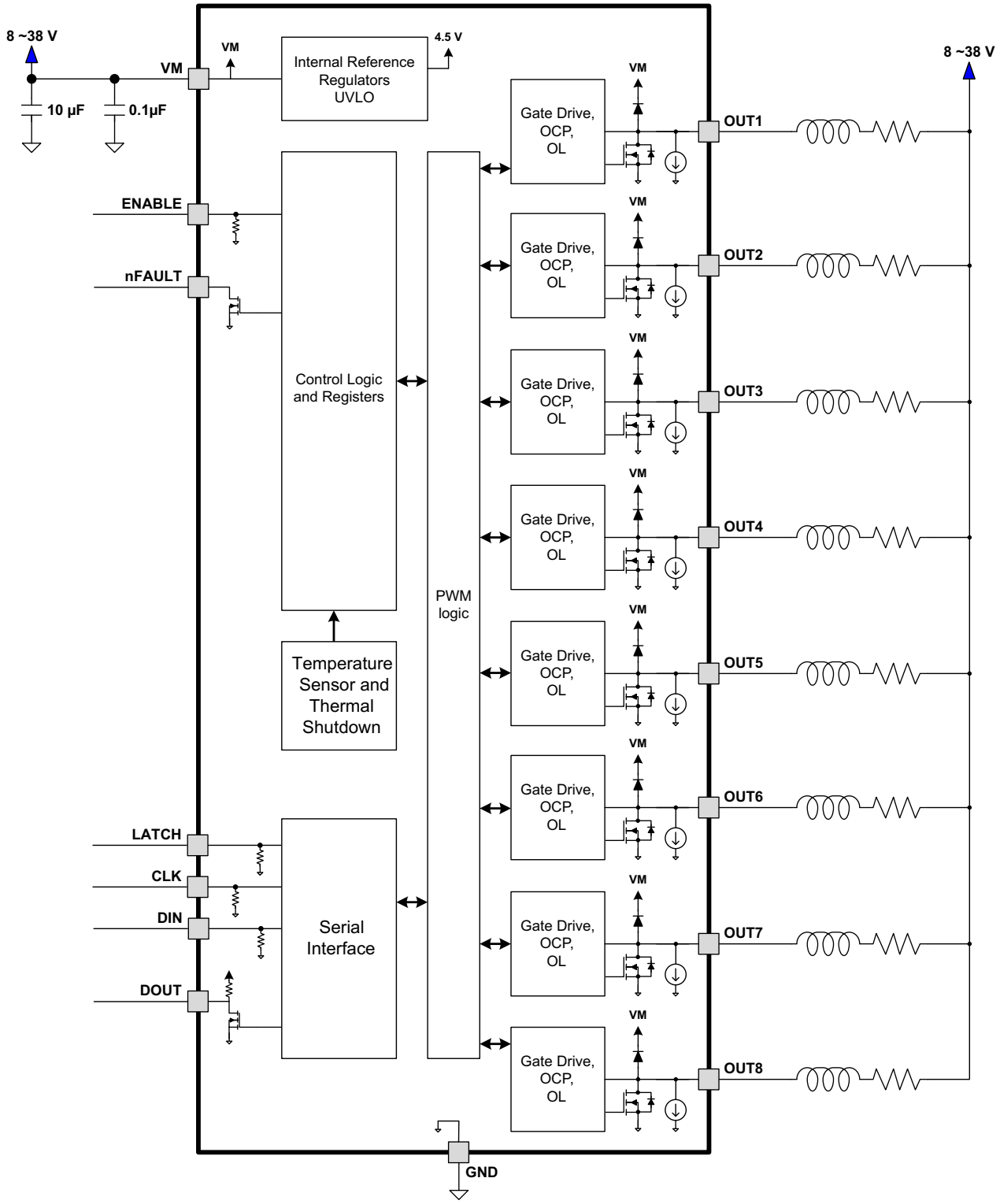
## 8.2 Functional Block Diagram





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## 8.3 Feature Description

### 8.3.1 Recommended Output Current

DRV8860 current capability will depend on several system application parameters such as system ambient temperature, maximum case temperature, and overall output duty cycle. The PWP package provides a better heatsinking capability through the PowerPAD™; and therefore, is cable of driving higher output current or operating at a slightly lower temperature than the device in PW package.

| OUTPUT CURRENT RECOMMENDATION (PW PACKAGE) $T_A$ = 25°C | |
|---|---|
| **CONFIGURATION** | **OUTPUT CURRENT CAPACITY** |
| 1x output on (100% duty cycle) | 566 mA |
| 2x outputs on (100% duty cycle) | 400 mA per output |
| 4x outputs on (100% duty cycle) | 283 mA per output |
| 8x outputs on (100% duty cycle) | 200 mA per output |

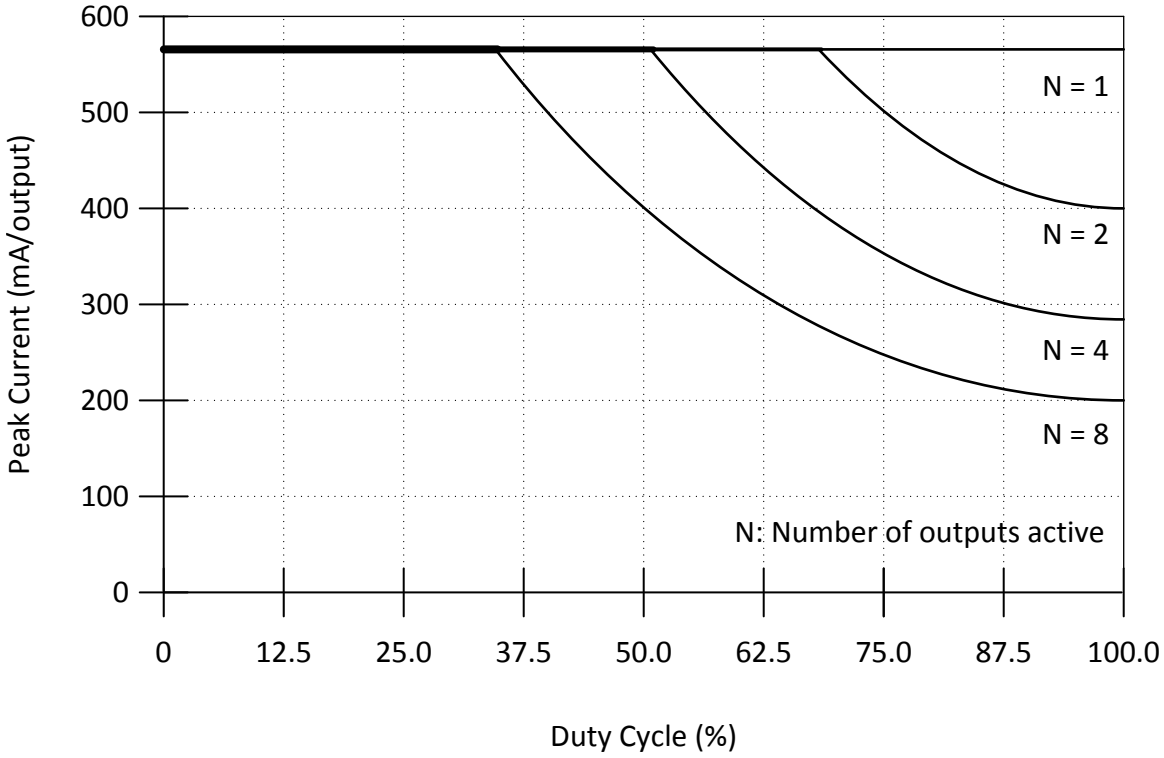


**Figure 3. Output Current Capacity vs Duty Cycle for PW Package**

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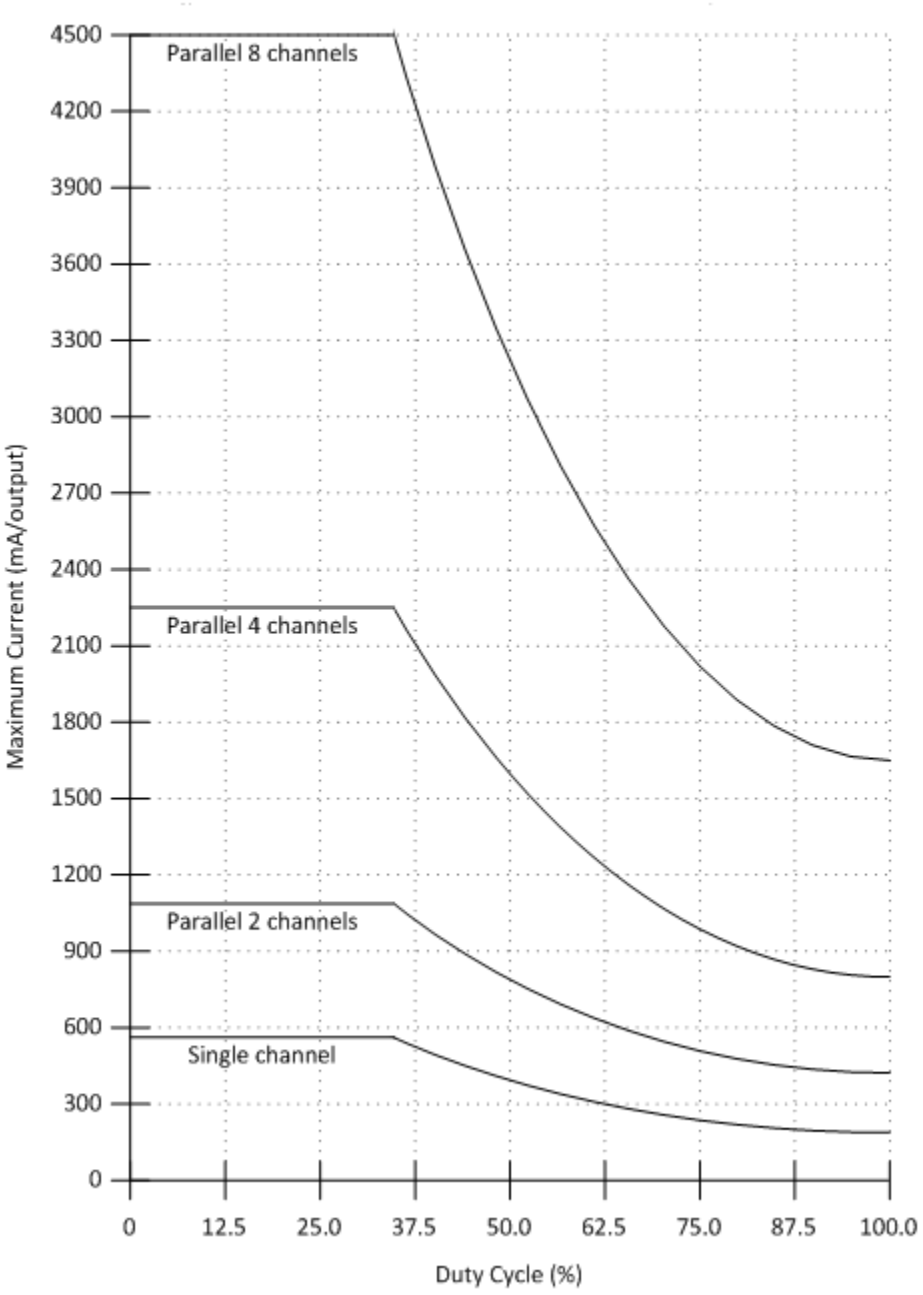


**Figure 4. Maximum Current Capacity vs Duty Cycle when Paralleling Outputs for DRV8860PW**


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### 8.3.2 Daisy Chain Connection

Two or more DRV8860 devices may be connected together to use a single serial interface. The SDATOUT pin of the first device in the chain is connected to the SDATIN pin of the next device. The SCLK, LATCH, RESET, and nFAULT pins are connected together.

Timing diagrams are shown in Figure 5 and Figure 6 for the configuration of single devices, as well as two devices in daisy-chain connection.

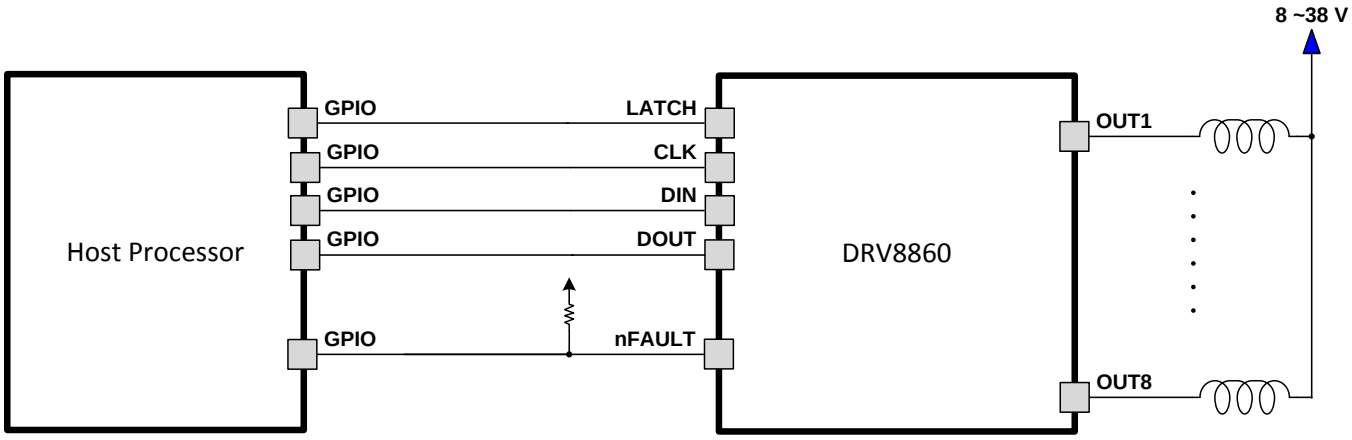


**Figure 5. Single Device Connection**

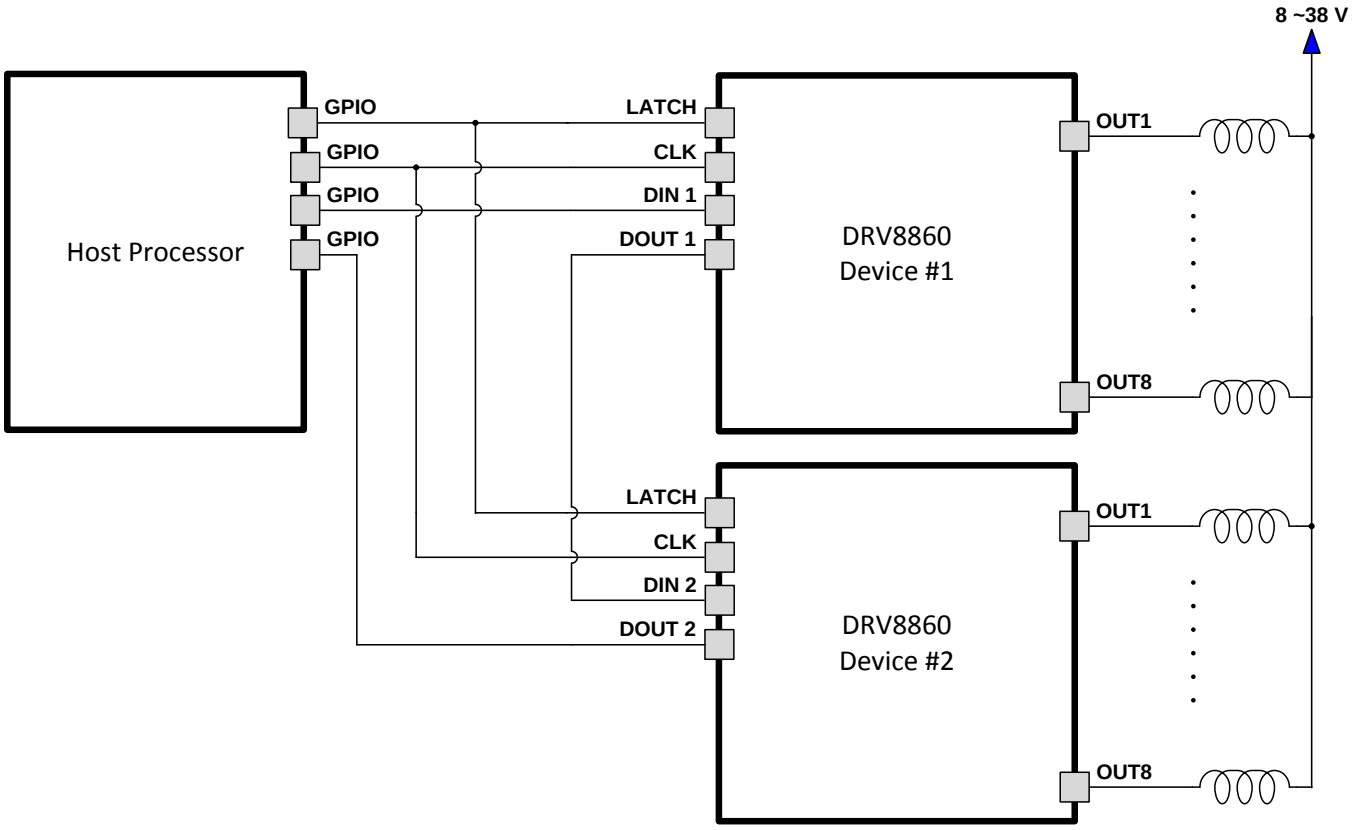


**Figure 6. Daisy-Chain Connection**

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### 8.3.3 Protection Circuits

The DRV8860 is fully protected against undervoltage, overcurrent and overtemperature events.

#### *8.3.3.1 Overcurrent Protection (OCP)*

When output current exceeds OCP trigger level, corresponding channel will be automatically turned off. nFault pin will be set low and corresponding OCP flag in fault register will be set to 1.

Over current faults are automatically cleared whenever the corresponding output is turned off by setting the Data register bit to '0'. Alternatively, a Fault Reset special command will also clear this value. In either case, once all bits in the Fault register are clear, nFAULT is released.

#### *8.3.3.2 Open Load Detection (OL)*

When any output is in off status (the corresponding Data Register bit is set to '0'), a current sink pulls the node down with approximately 30 μA. If the voltage on the pin is sensed to be less than 1.2 V, then an open load condition is reported. nFAULT is driven low and the OL bit of the fault register (F8:F1) corresponding to the specific channel is set.

Open load faults are automatically cleared whenever the corresponding output is turned on by setting the Data register bit to '1'. Alternatively, a Fault Reset special command will also clear this value. In either case, once all bits in the Fault register are clear, nFAULT is released.

#### *8.3.3.3 Thermal Shutdown (TSD)*

If the die temperature exceeds safe limits, all outputs will be disabled, and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume. The nFAULT pin will be released after operation has resumed.

#### *8.3.3.4 Undervoltage Lockout (UVLO)*

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold. nFAULT will not be asserted in this condition.

#### *8.3.3.5 Digital Noise Filter*

The DRV8860 features an internal noise filter on all digital inputs. In a noisy system, noise may disturb the serial daisy-chain interface. Without an input filter, this noise may result in an unexpected behavior or output state. The digital input filter is capable of removing unwanted noise frequencies while allowing fast communication over the serial interface.


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## 8.4 Device Functional Modes

### 8.4.1 Internal Registers

The DRV8860 is controlled with a simple serial interface. There are three register banks that are used during operation: the Data register, the Control register, and the Fault register.

Register data movement flow and direction will be affected by special command.

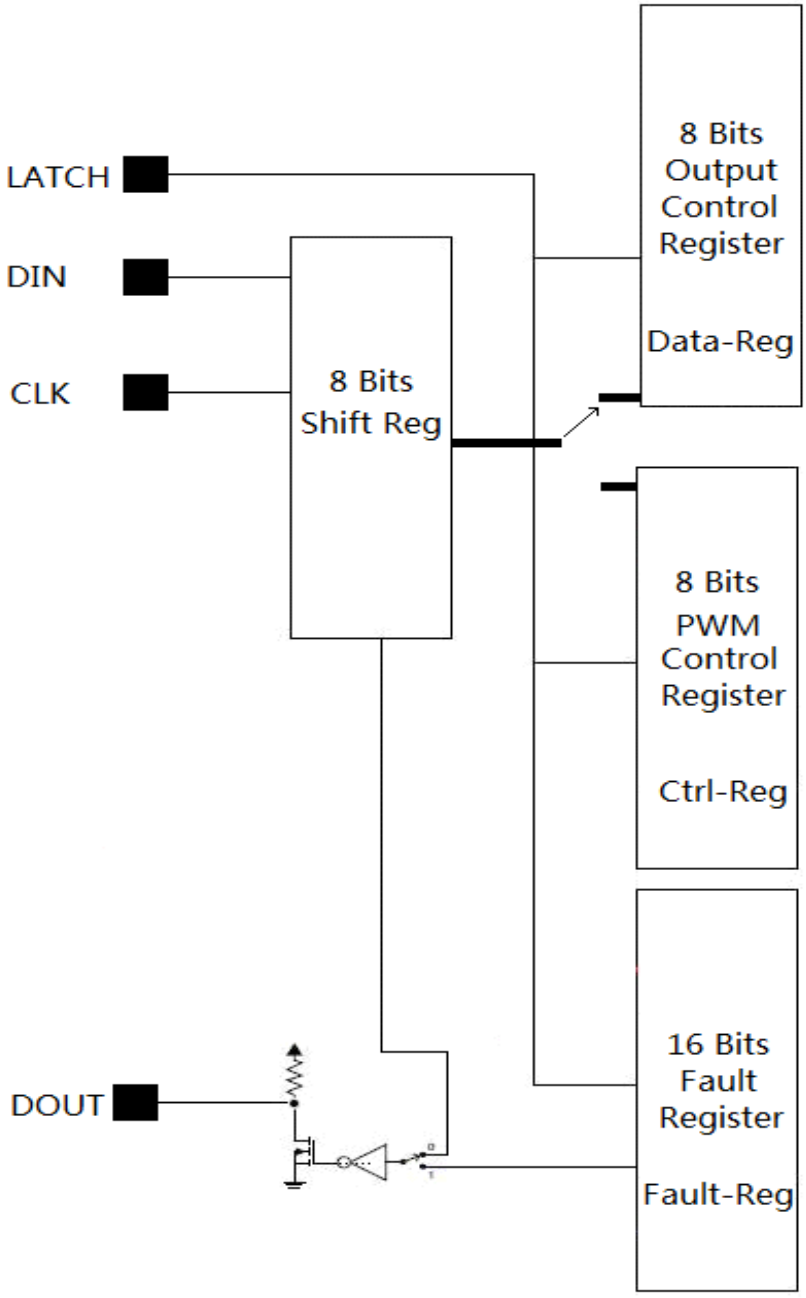


**Figure 7. Register Data Movement**

In default condition, 8 Bit shift register data moves into output control register DATA-REG.

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## Device Functional Modes (continued)

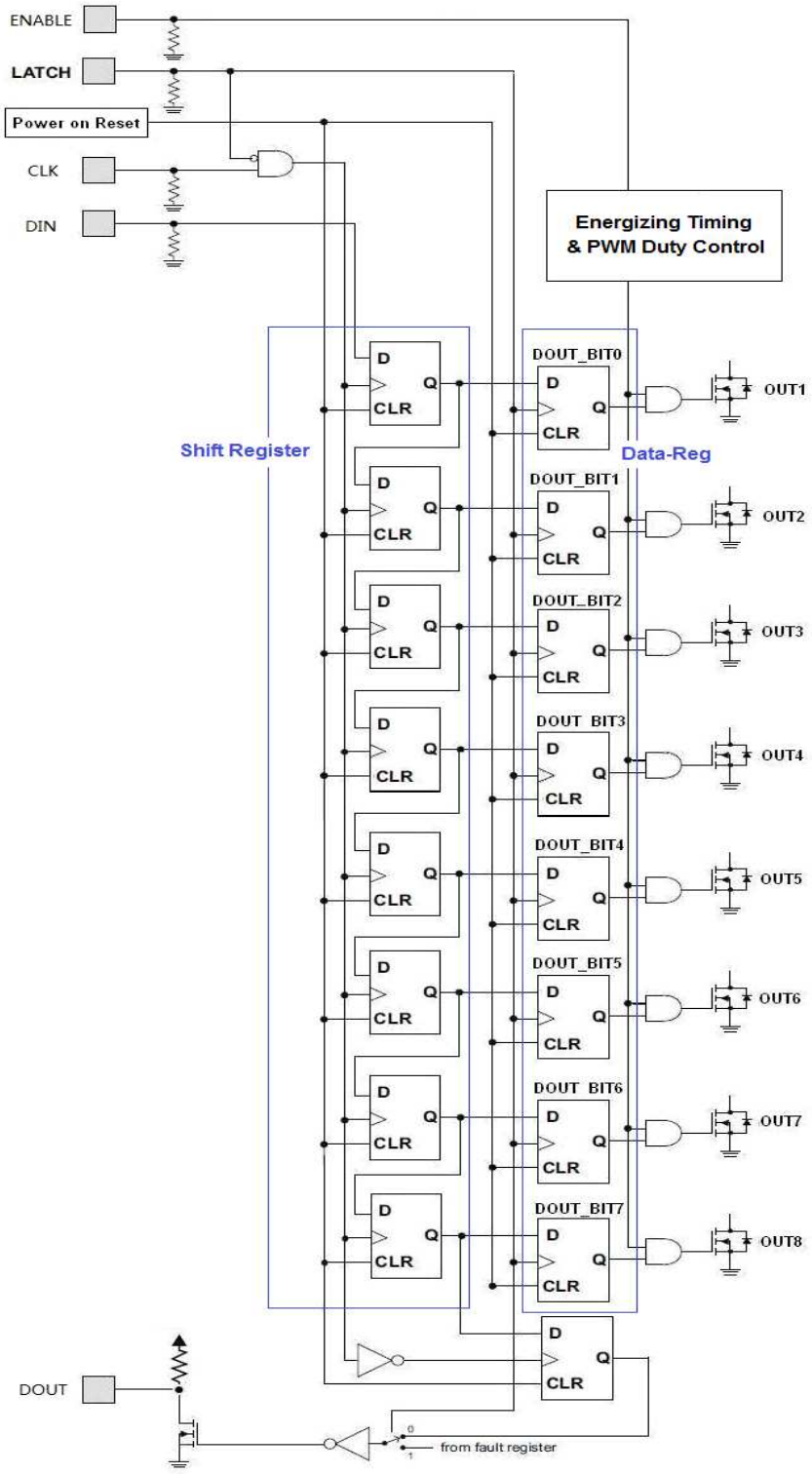


**Figure 8. 8 Bit Shift Register Data Movement**


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## 8.5 Programming

### 8.5.1 Serial Control Interface

DRV8860 is using a daisy chain serial interface. Data is latched into the register on the rising edge of the LATCH pin. Data is clocked in on the rising edge of CLK when writing, and data is clocked out on the falling edge of CLK when reading.

#### *8.5.1.1 Data Writing Waveform*

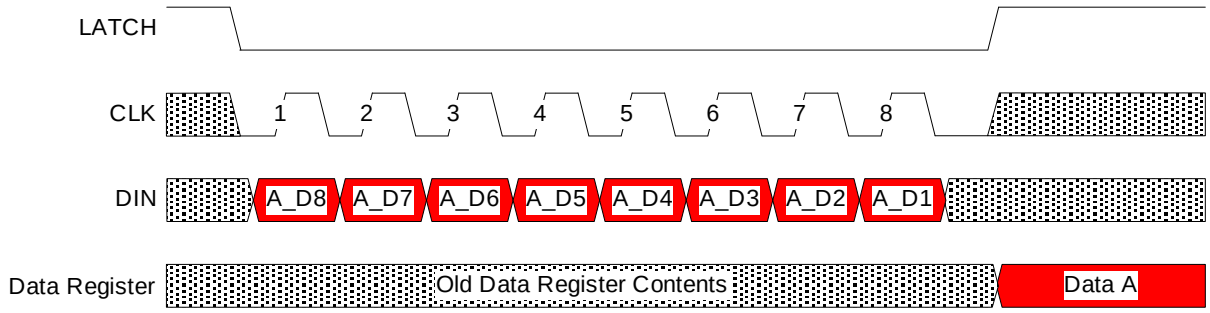


**Figure 9. Writing Data Register – Single Device**

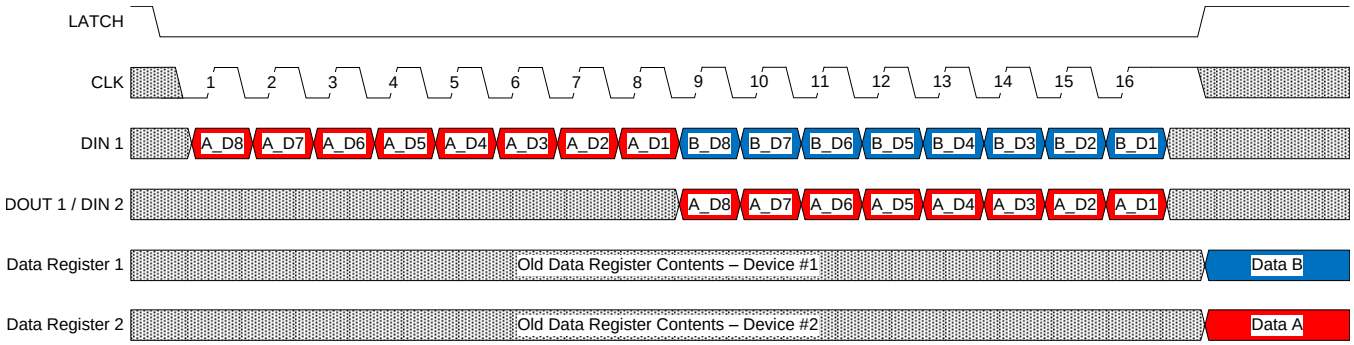


**Figure 10. Writing Data Register – Daisy Chan**

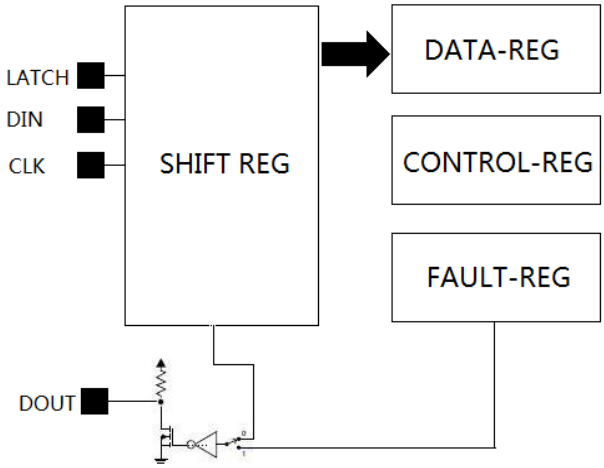


**Figure 11. Writing Data Register – Data Flow**

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## Programming (continued)

### 8.5.1.2 Fault Register Reading Waveform

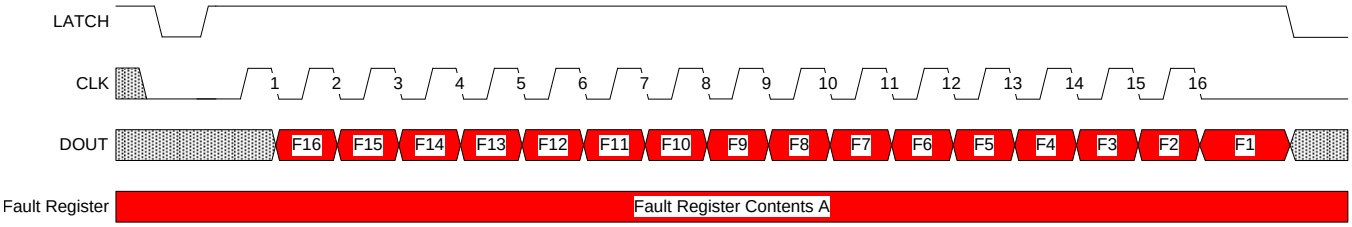


**Figure 12. Reading Fault Register – Single Device**

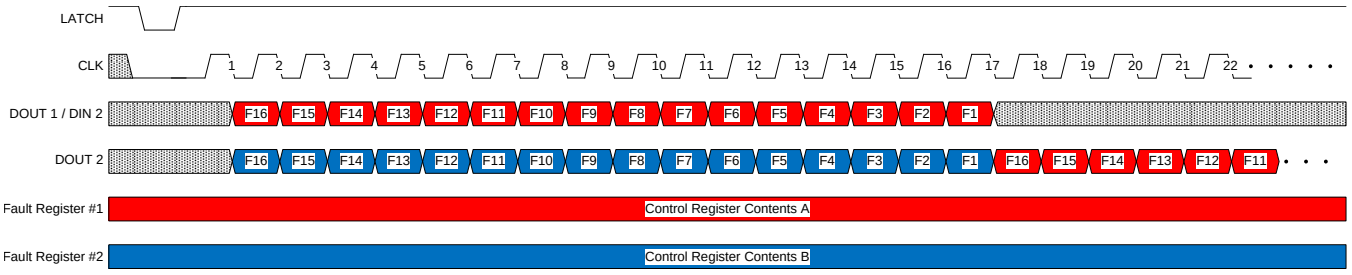


**Figure 13. Reading Fault Register – Daisy Chain**

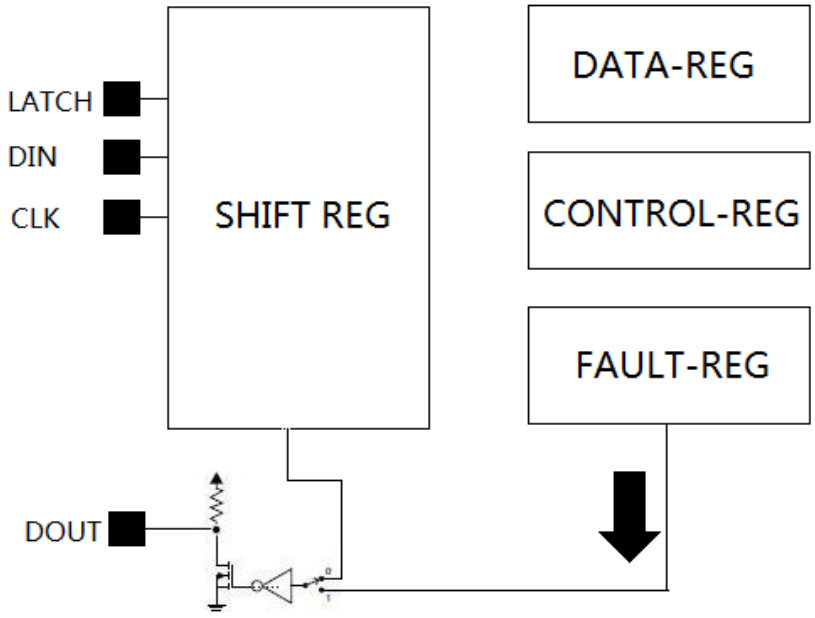


**Figure 14. Reading Fault Register – Data Flow**


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## Programming (continued)

### *8.5.1.3 Special Command*

Besides output ON/OFF control and fault status reading back, DRV8860 has special functions to make system more robust or power efficient. These functions will need special command to initiate the device or configure the internal registers.

There are 5 Special Commands:

1. Write Control Register command
2. Read Control Register command
3. Read Data Register command
4. Fault Register Reset command
5. PWM Start command

Special wave form pattern on CLK and LATCH pin will issue the special command, as below

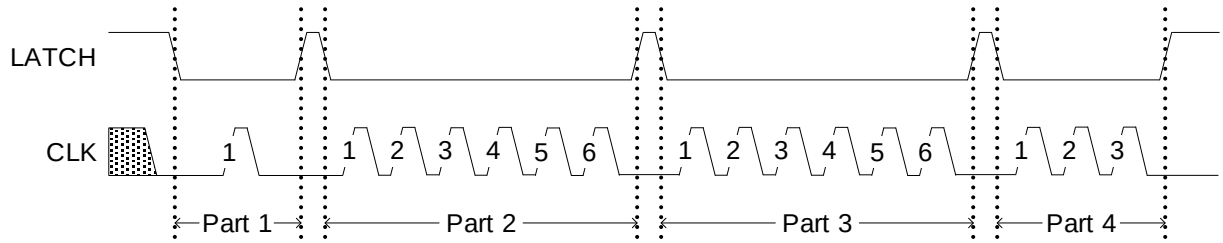


**Figure 15. Special Command**

| SPECIAL COMMAND | CLK CYCLES IN EACH PART | | | |
|---|---|---|---|---|
| | Part 1 | Part 2 | Part 3 | Part 4 |
| Write Control Register | 1 | 2 | 2 | 3 |
| Read Control Register | 1 | 4 | 2 | 3 |
| Read Data Register | 1 | 4 | 4 | 3 |
| Fault Register Reset | 1 | 2 | 4 | 3 |
| PWM Start | 1 | 6 | 6 | 3 |

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#### 8.5.1.3.1 Special command: Write Control Register

When Write-Control-Register command is issued, the following serial data will be latched into timing and duty control register.

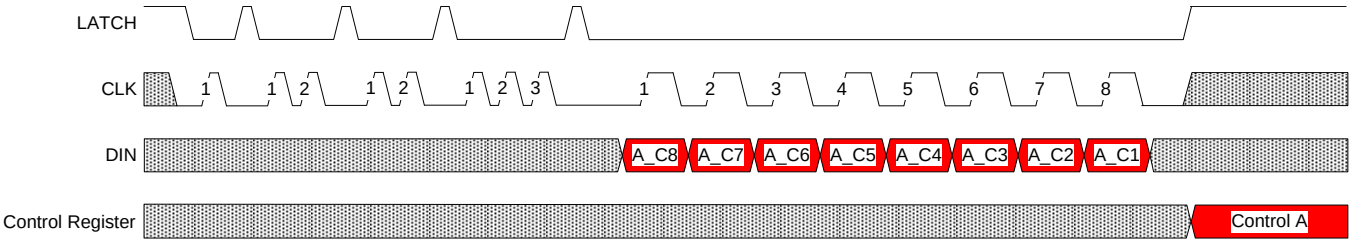


**Figure 16. Writing Control Register – Single Device**

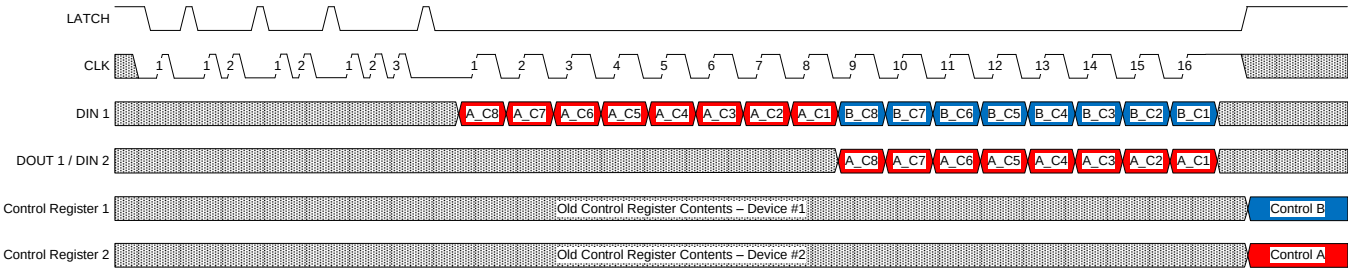


**Figure 17. Writing Control Register – Daisy Chain**

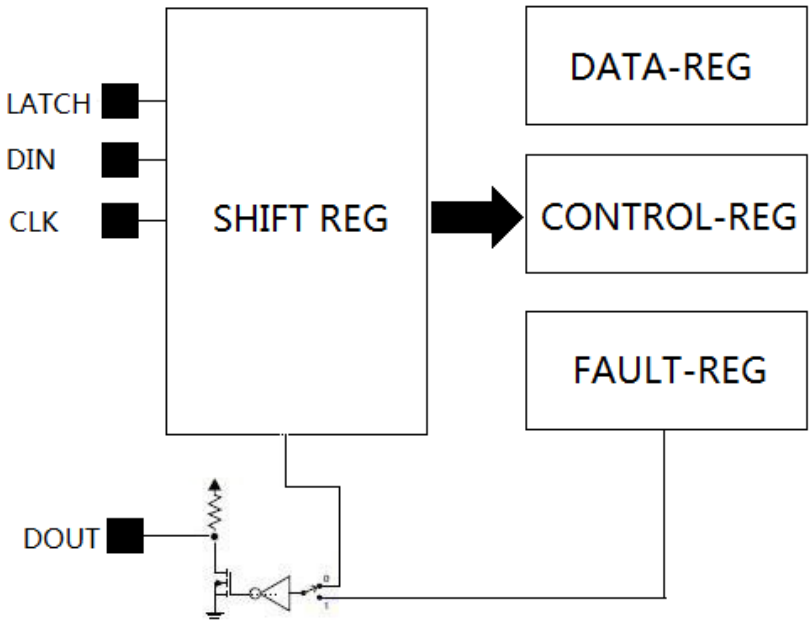


**Figure 18. Writing Control Register – Data Flow**


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#### 8.5.1.3.2 Special command: Read Control Register

When Read-Control-Register command is issued, control register content will be copied to internal shift register and following CLK will shift this content out from DOUT pin. This provides a mechanism for system to verify the control register is correctly programmed.

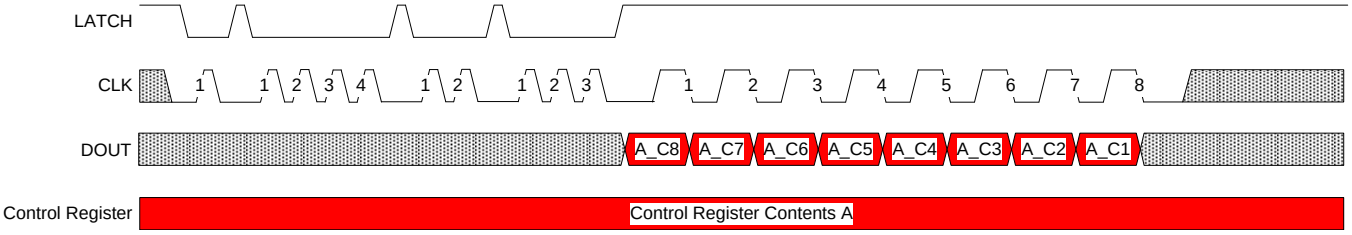


**Figure 19. Read Control Register – Single Device**

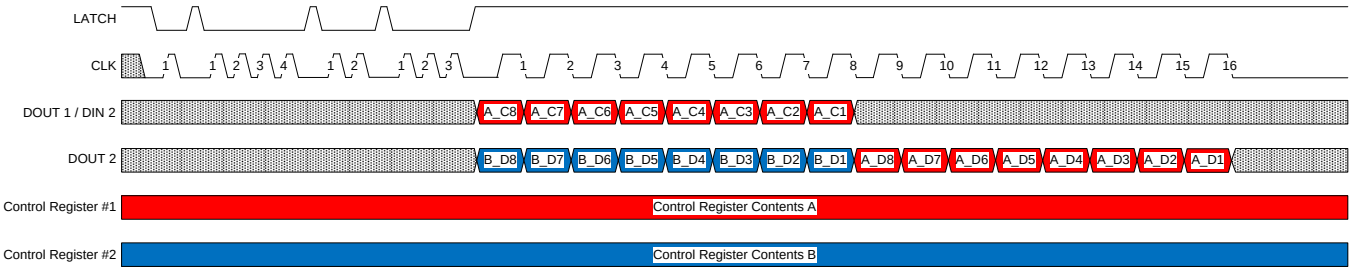


**Figure 20. Read Control Register – Daisy Chain**

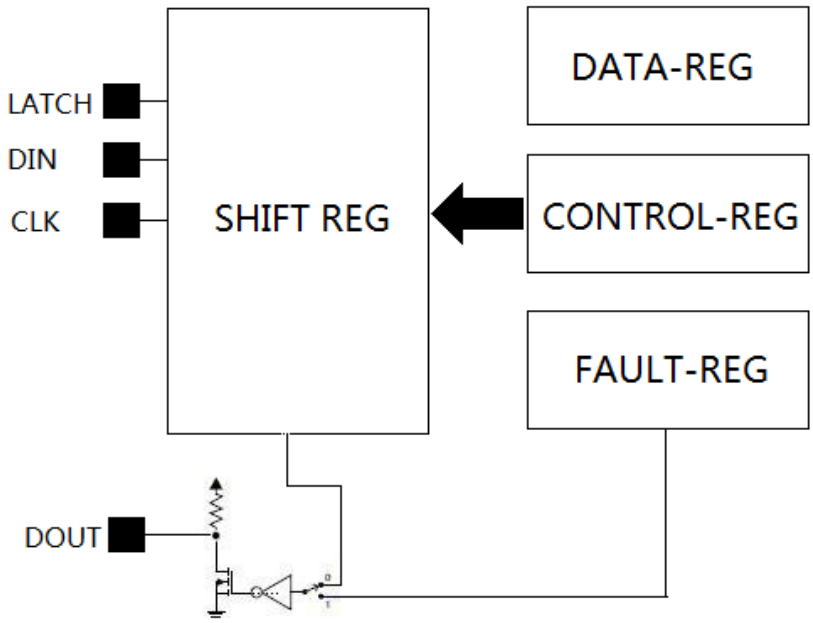


**Figure 21. Read Control Register – Data Flow**

#### 8.5.1.3.3 Special command: Read Data Register

When Read-Data-Register command is issued, internal output data register content will be copied to internal shift register and following CLK will shift this content out from DOUT pin. This provides a mechanism for system to verify the output data is correctly programmed. It makes system more robust in noisy system.

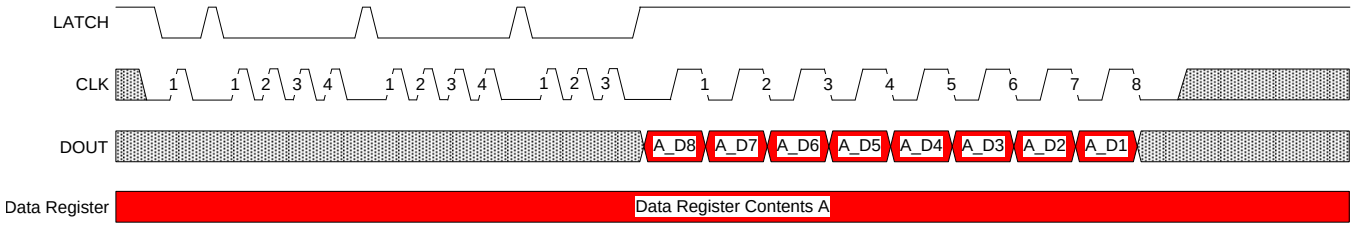


**Figure 22. Reading Data Register – Single Device**

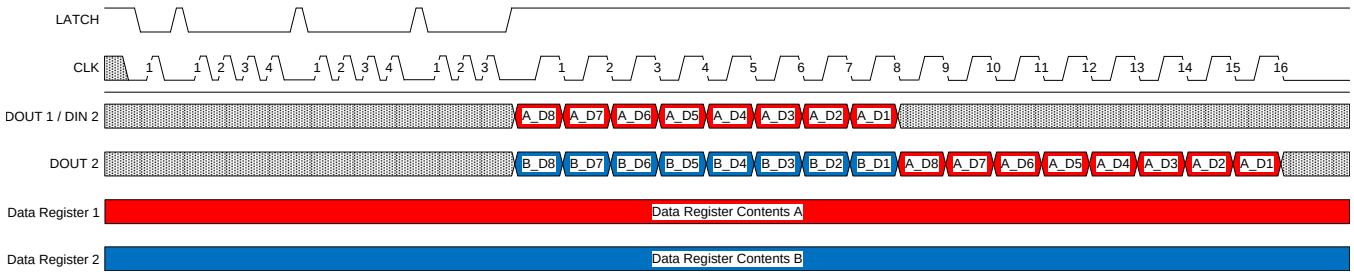


**Figure 23. Reading Data Register – Daisy Chain**

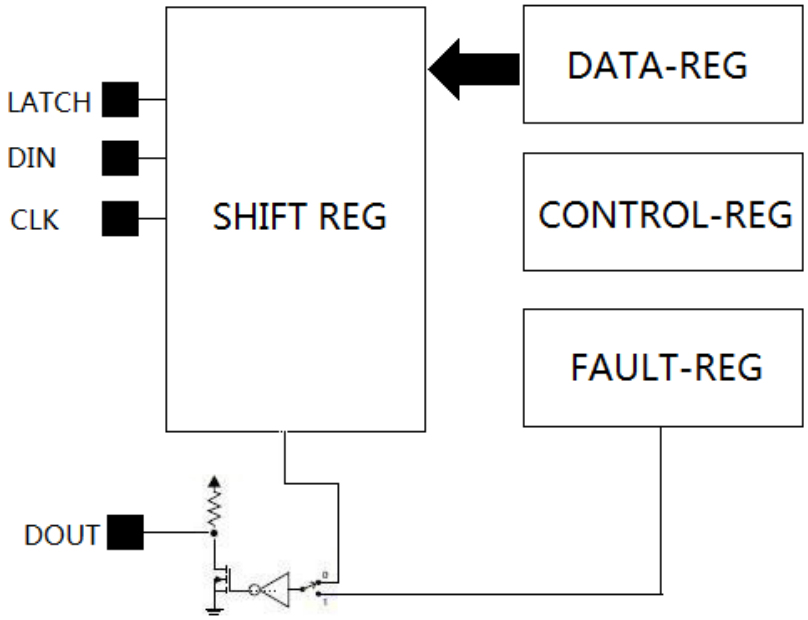


**Figure 24. Reading Data Register – Data Flow**


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#### 8.5.1.3.4 Special command: Fault Register Reset

When Fault-Register-Reset command is issued, internal 16bit fault register will be cleared. System can use this method to clear out all fault condition in every chained device at once.

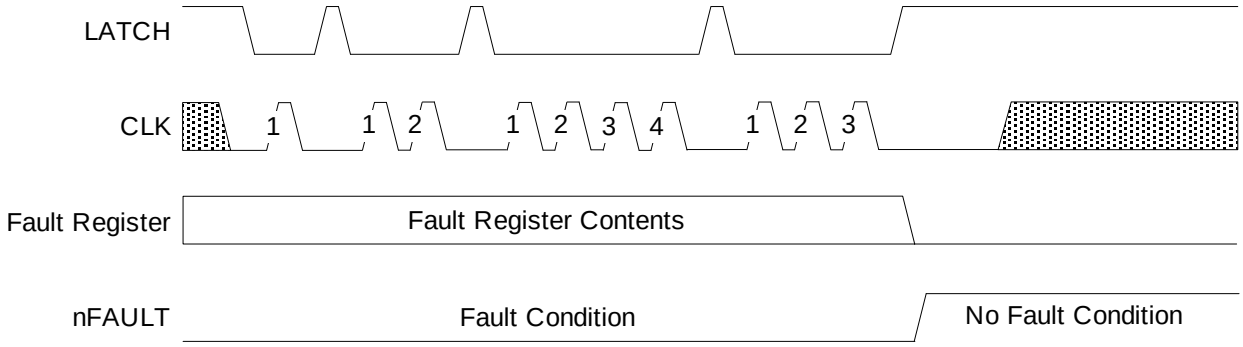


**Figure 25. Fault Register Reset**

#### 8.5.1.3.5 Special command: PWM Start

When Fault-Register-Reset command is issued, output channel will ignore energizing time and directly enter into PWM mode following the setting in control register.

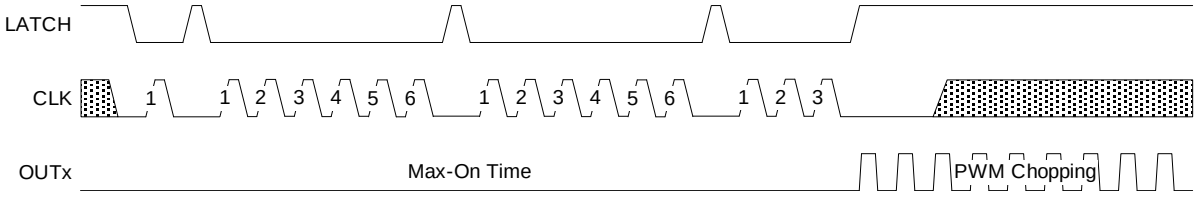


**Figure 26. PWM Start Command**

#### 8.5.1.4 Output Energizing and PWM Control

The device output is defined by two stages: Energizing Phase and PWM Phase.

During the Energizing phase, the channel is turned on with 100% duty cycle for a duration set by Control register bits C4:C1.

In PWM chopping phase, with the PWM Duty Cycle defined by Control register bits C7:C5.

The behavior of each bit in the Control Register is described in Table 2.

**Table 2. Control Register Settings**

| C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | Value | DESCRIPTION | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | X | X | N/A | Outputs always in Energizing mode | |
| 1 | X | X | X | 0 | 0 | 0 | 0 | 0 ms | No Energizing, starts in PWM chopping | |
| 1 | X | X | X | 0 | 0 | 0 | 1 | 3 ms | Sets the Energizing Time (100% duty cycle) before switching to PWM Phase | |
| 1 | X | X | X | 0 | 0 | 1 | 0 | 5 ms | | |
| 1 | X | X | X | 0 | 0 | 1 | 1 | 10 ms | | |
| 1 | X | X | X | 0 | 1 | 0 | 0 | 15 ms | | |
| 1 | X | X | X | 0 | 1 | 0 | 1 | 20 ms | | |
| 1 | X | X | X | 0 | 1 | 1 | 0 | 30 ms | | |
| 1 | X | X | X | 0 | 1 | 1 | 1 | 50 ms | | |
| 1 | X | X | X | 1 | 0 | 0 | 0 | 80 ms | | |
| 1 | X | X | X | 1 | 0 | 0 | 1 | 110 ms | | |
| 1 | X | X | X | 1 | 0 | 1 | 0 | 140 ms | | |
| 1 | X | X | X | 1 | 0 | 1 | 1 | 170 ms | | |
| 1 | X | X | X | 1 | 1 | 0 | 0 | 200 ms | | |
| 1 | X | X | X | 1 | 1 | 0 | 1 | 230 ms | | |
| 1 | X | X | X | 1 | 1 | 1 | 0 | 260 ms | | |
| 1 | X | X | X | 1 | 1 | 1 | 1 | 300 ms | | |
| 1 | 0 | 0 | 0 | X | X | X | X | 0% | Output is off after Energizing Phase | |
| 1 | 0 | 0 | 1 | X | X | X | X | 12.50% | 12.5 kHz | Sets PWM chopping duty cycle. DC is the duty cycle that the low-side FET is on. |
| 1 | 0 | 1 | 0 | X | X | X | X | 25.00% | 25 kHz | |
| 1 | 0 | 1 | 1 | X | X | X | X | 37.50% | 50 kHz | |
| 1 | 1 | 0 | 0 | X | X | X | X | 50.00% | | |
| 1 | 1 | 0 | 1 | X | X | X | X | 62.50% | | |
| 1 | 1 | 1 | 0 | X | X | X | X | 75.00% | | |
| 1 | 1 | 1 | 1 | X | X | X | X | 87.50% | | |


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There are five operation cases as described in Figure 27 through Figure 31.

The output is turned on with 100% duty cycle.

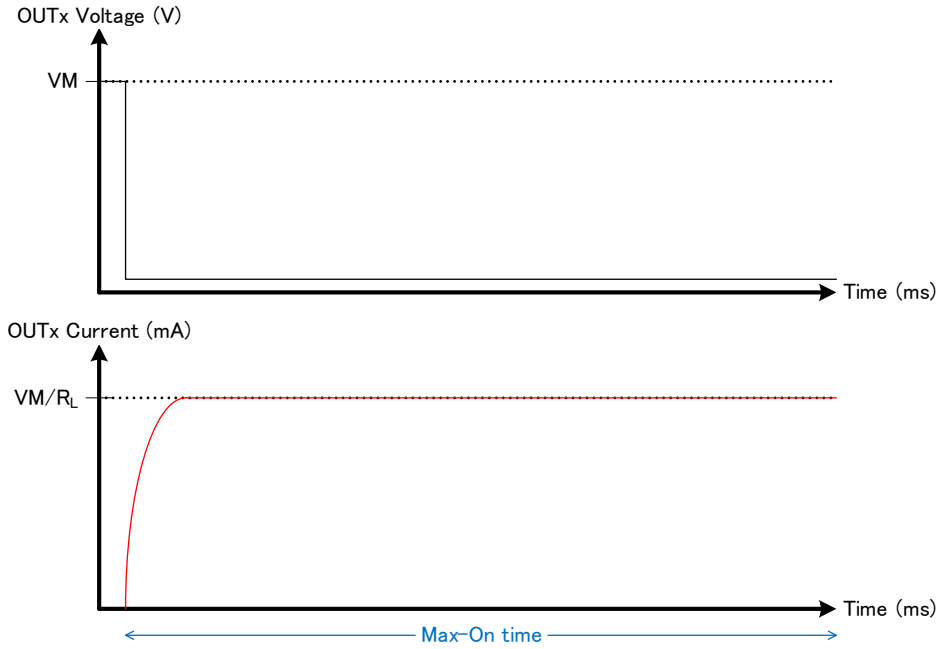


**Figure 27. Case 1: Timer Enable Bit (C8) is 0 (Default Value)**

The output is turned on in PWM chopping mode with duty cycle defined by Control register bits C7:C5.

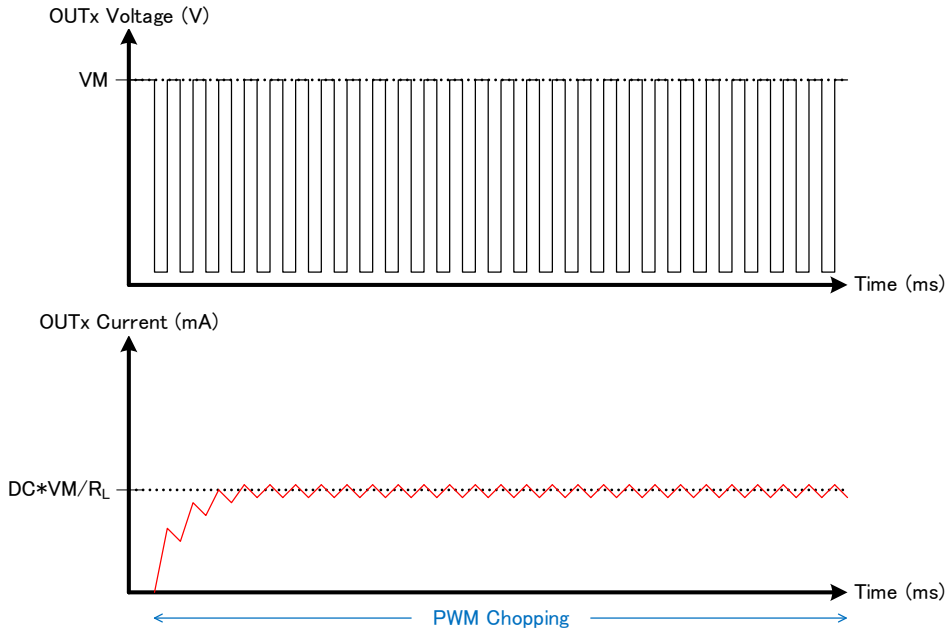


**Figure 28. Case 2: Timer Enable Bit (C8) is 1 and Energizing Timing Bits (C4:C1) are 0000**

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The output is turned on in Energizing mode with 100% duty cycle for a duration set by Control register bits C4:C1. After the timer expires, the output switches to PWM chopping mode with PWM Duty Cycle defined by Control register bits C7:C5.

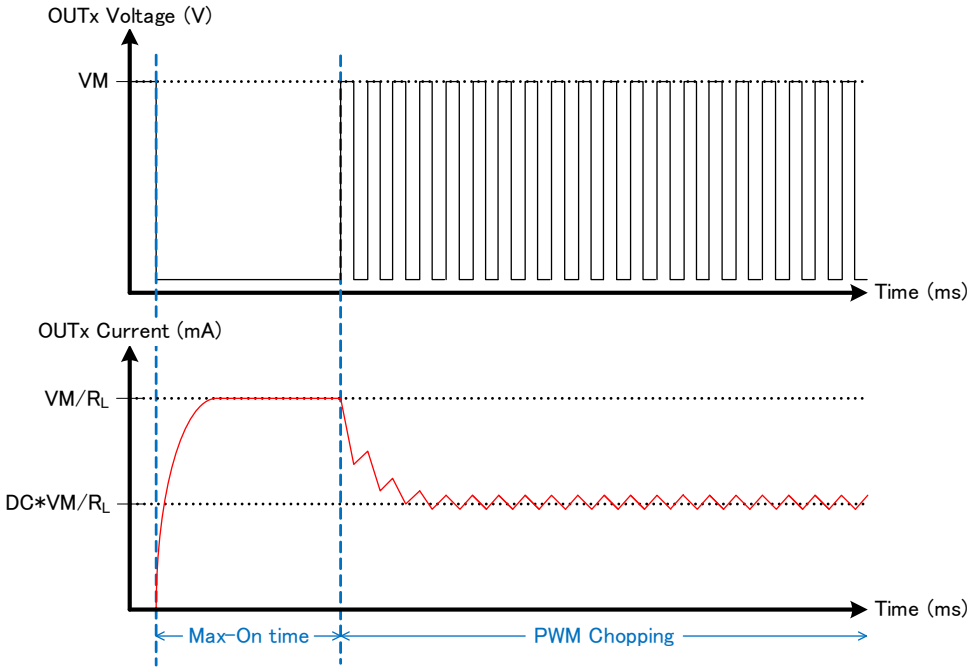


**Figure 29. Case 3: Timer Enable Bit (C8) is 1, Energizing Timing Bits (C4:C1) are NOT 0000, and PWM Duty Bits (C7:C5) are NOT 000**

The output is turned on in Energizing mode with 100% duty cycle for a duration set by Control register bits C4:C1. After the timer expires, the output is turned off.

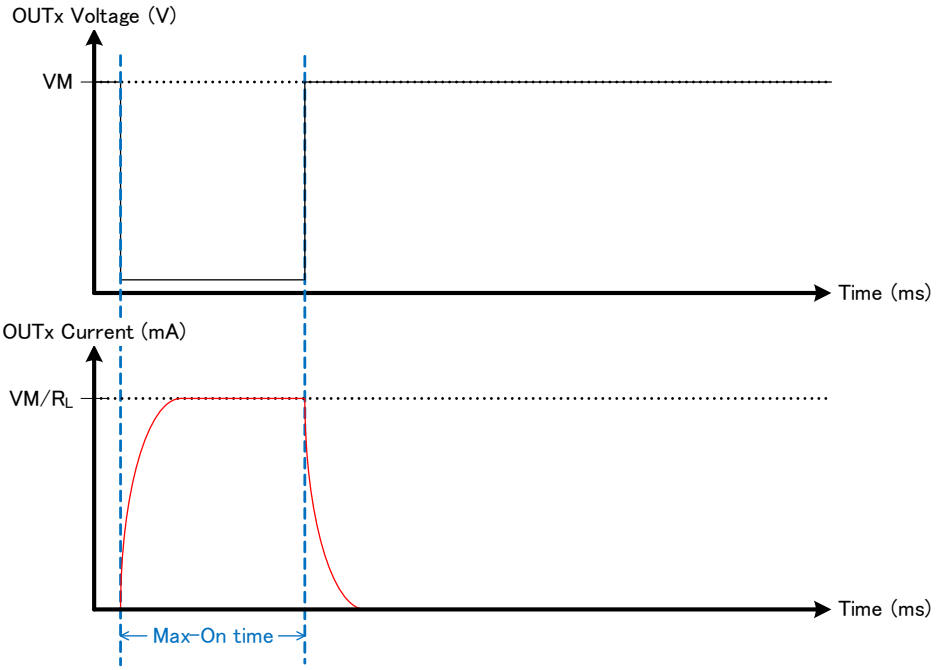


**Figure 30. Case 4: Timer Enable Bit (C8) is 1, Energizing Timing Bits (C4:C1) are NOT 0000, and PWM Duty Bits (C7:C5) are 00**


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#### 8.5.1.4.1 PWM Start Special Command Used

The output is turned on in Energizing mode with 100% duty cycle, and a timer is enabled with duration set by Control register bits C4:C1. If the PWM Start special command is received before the timer expires, then the output switches to PWM chopping mode with PWM Duty Cycle defined by Control register bits C7:C5. If the timer expires and no PWM Start is received, then the device will stay in Energizing mode regardless of other PWM Start commands.

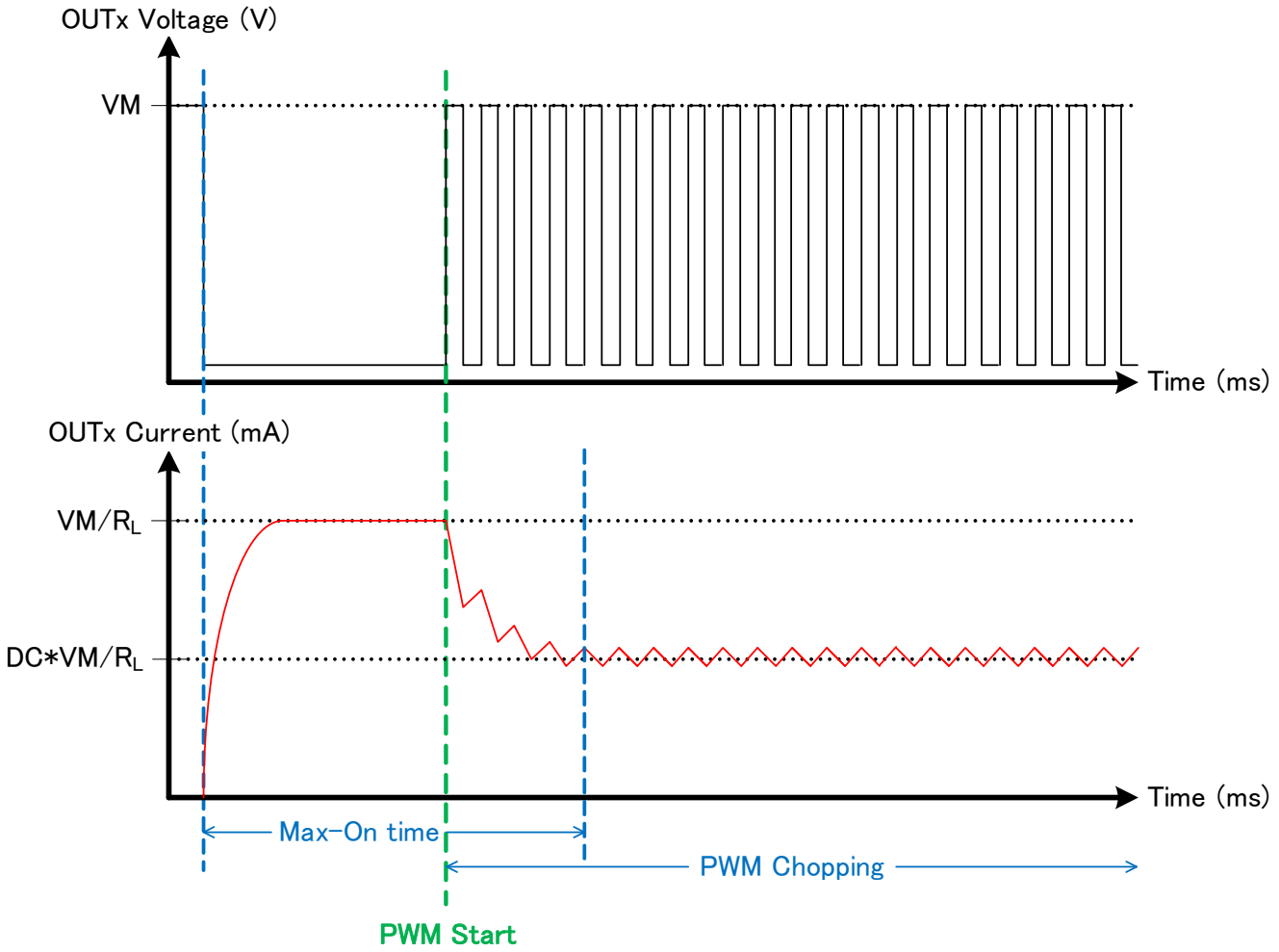


**Figure 31. Case 5: Timer Enable Bit (C8) is 0, Energizing Timing Bits (C4:C1) are NOT 0000, and PWM Duty Bits (C7:C5) are NOT 000**

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## 8.6 Register Maps

### 8.6.1 Data Register

The Data register is used to control the status of each of the eight outputs:

**Figure 32. Data Rester**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 |
|---|---|---|---|---|---|---|---|
| OUT8 | OUT7 | OUT6 | OUT5 | OUT4 | OUT3 | OUT2 | OUT1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When any bit is ‘1’, the corresponding output will be active. When any bit is ‘0’, the output will be inactive.

The data register is the default write location for the serial interface. In order to read back data from this register, the Data Register Readout special command is used.

### 8.6.2 Fault Register

The Fault register can be read to determine if any channel exist fault condition. OCP is an overcurrent fault and OLD is an open load fault.

**Figure 33. Fault Register**

| F16 | F15 | F14 | F13 | F12 | F11 | F10 | F9 |
|---|---|---|---|---|---|---|---|
| OUT8 OCP | OUT7 OCP | OUT6 OCP | OUT5 OCP | OUT4 OCP | OUT3 OCP | OUT2 OCP | OUT1 OCP |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 |
| OUT8 OL | OUT7 OL | OUT6 OL | OUT5 OL | OUT4 OL | OUT3 OL | OUT2 OL | OUT1 OL |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When any fault occurs, nFAULT pin will be driven low and corresponding Fault register bit will be set up as ‘1’. OCP is a flag indicating overcurrent fault. ODP is a flag indicating open load fault.

Fault bits can be reset by two approaches:

1. Special command ‘FAULT RESET’ clear all fault bits.
2. Setting Data register to ON will clear corresponding OLD bits.
   Setting Data register to OFF will clear corresponding OCP bits.

### 8.6.3 Control Register

The Control register is used to adjust the Energizing Time and PWM Duty Cycle of outputs:

**Figure 34. Control Rester**

| C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 |
|---|---|---|---|---|---|---|---|
| Over All Enable | PWM Duty Cycle control | | | Energizing Time control | | | |
| R/W | R/W | | | R/W | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Special command ‘WRITE CONTROL REGISTER’ is used to program control register.

Special command ‘READ CONTROL REGISTER’ is used to read back control register content.


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# 9 Application and Implementation

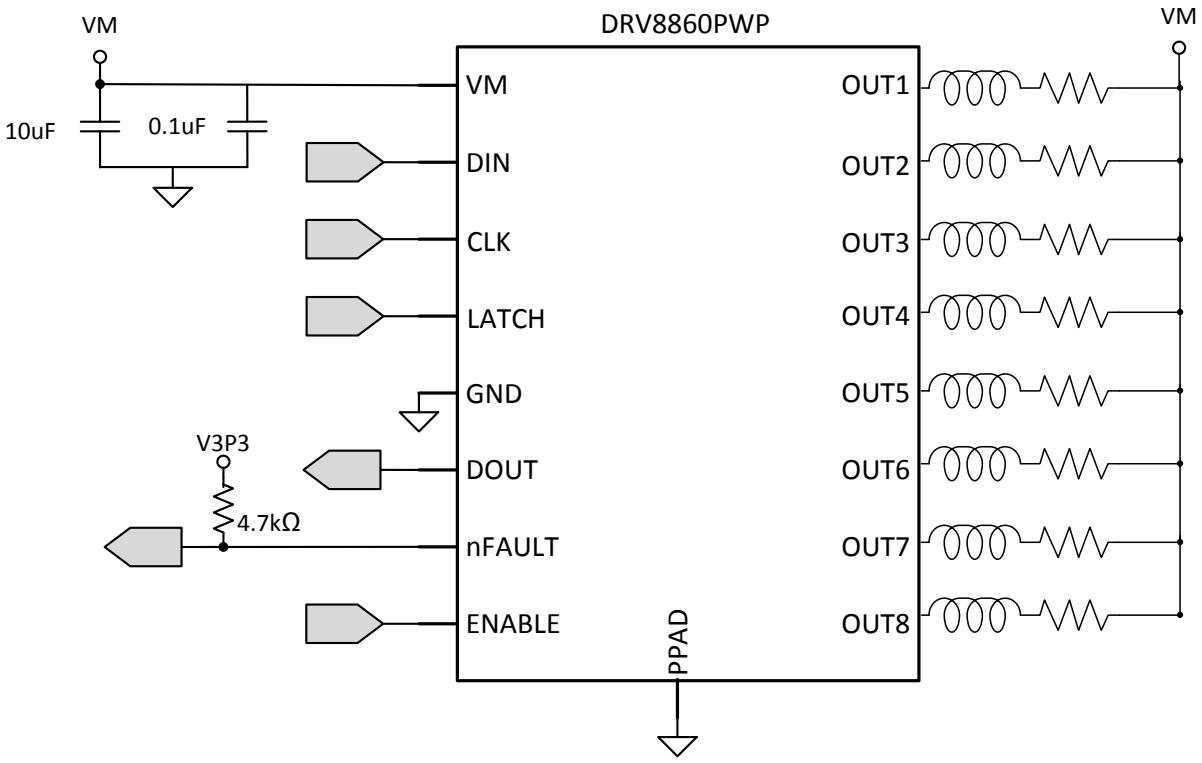
**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The DRV8860 is an eight channel low side driver with protection features. The following design is a common application of the DRV8860.

## 9.2 Typical Application




### 9.2.1 Design Requirements

**Table 3. Design Parameters**

| Parameter | Value |
|---|---|
| Input voltage range | 8 V – 38 V |
| Current | 330 mA per channel |

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### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Drive Current*

The current path is from VM, through the load, into the low-side sinking driver. Power dissipation $I^2R$ losses in one sink are calculated using Equation 1.

$$P_D = I^2 \times R_{DS(on)} \quad (1)$$

### 9.2.3 Application Curves

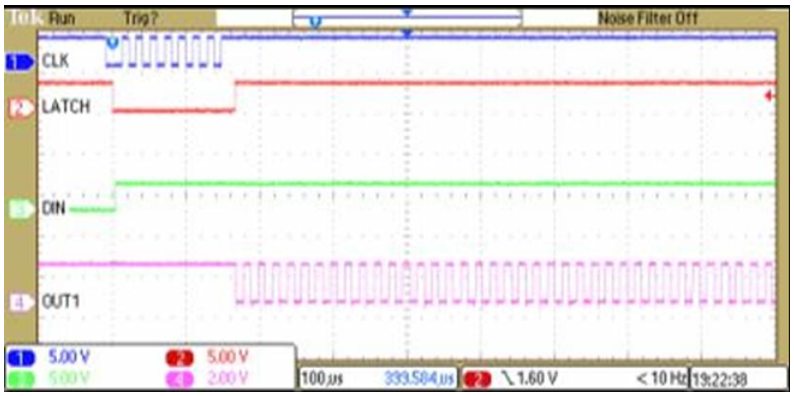


**Figure 35. PWM Operation**


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# 10 Power Supply Recommendations

The DRV8860 is designed to operate from an input voltage supply (VM) range between 8 and 38 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close as possible to the VM pin. In addition to the local decoupling cap, additional bulk capacitance is required and must be sized accordingly to the application requirements.

Bulk capacitance sizing is an important factor in motor drive system design. It is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of load
- Load startup current

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. The user should size the bulk capacitance to meet acceptable voltage ripple levels.

The datasheet generally provides a recommended value but system level testing is required to determine the appropriate sized bulk capacitor.

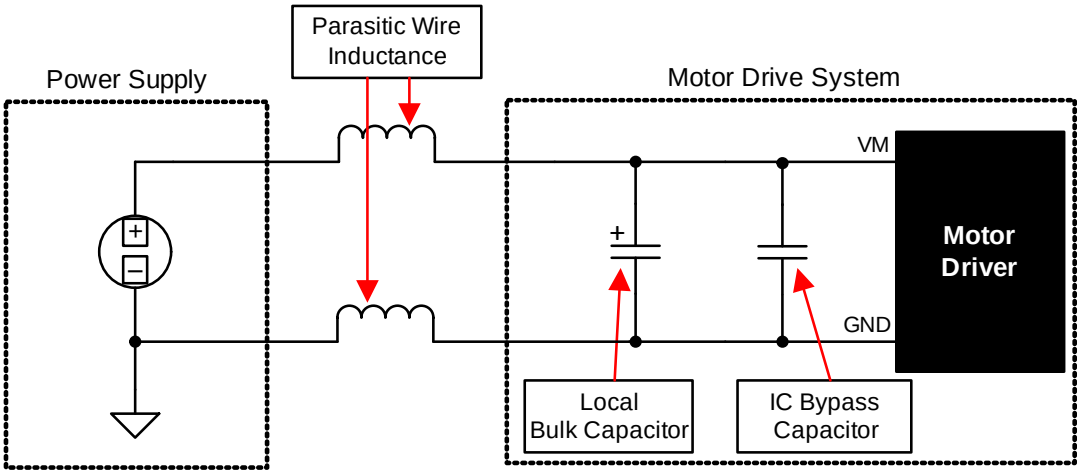


**Figure 36. Example Setup of Motor Drive System with External Power Supply**

## 10.1 Power Supply and Logic Sequencing

There is no specific sequence for powering-up the DRV8860. It is okay for digital input signals to be present before VM is applied. After VM is applied to the DRV8860, it begins operation based on the status of the control pins.

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# 11 Layout

## 11.1 Layout Guidelines

- The VM pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.1-µF rated for VM.
- This capacitor should be placed as close as possible to the VM pin on the device with a thick trace or ground plane connection to the device GND pin.
- The VM pin must be bypassed to ground using and appropriate bulk capacitor. This component must be located close to the DRV8860.

## 11.2 Layout Example

Where the pull-up voltage (V3P3) is an external supply in the range of the recommended operating conditions for the digital open-drain outputs.

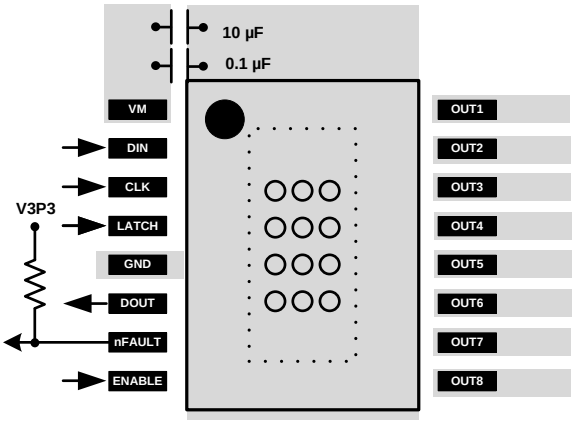


**Figure 37. DRV8860 Layout**


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## 11.3 Thermal Consideration

The DRV8860 device has thermal shutdown (TSD) as described in the *Thermal Shutdown (TSD)* section. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

### 11.3.1 Power Dissipation

Power dissipation in the DRV8860 device is dominated by the power dissipated in the output FET resistance, $R_{DS(on)}$. Use the following equation to calculate the estimated average power dissipation of each output when running a driving a load.

$$P_D = R_{DS(on)} \times I_O^2 \quad (2)$$

where:

- $P_D$ is the power dissipation of one channel
- $R_{DS(on)}$ is the resistance of each FET
- $I_O$ is the RMS output current being applied to each channel

$I_O$ is equal to the average current into the channel. Note that at startup, this current is much higher than normal running current; these peak currents and their duration must be also be considered.

The total device dissipation is the power dissipated in each channel added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

**NOTE**

$R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.

### 11.3.2 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to the TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and the TI application brief, *PowerPAD Made Easy™* (SLMA004), available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.

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# 12 器件和文档支持

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## 12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

# 13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。


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| | 产品 | | 应用 |
|---|---|---|---|
| 数字音频 | www.ti.com.cn/audio | 通信与电信 | www.ti.com.cn/telecom |
| 放大器和线性器件 | www.ti.com.cn/amplifiers | 计算机及周边 | www.ti.com.cn/computer |
| 数据转换器 | www.ti.com.cn/dataconverters | 消费电子 | www.ti.com/consumer-apps |
| DLP® 产品 | www.dlp.com | 能源 | www.ti.com/energy |
| DSP - 数字信号处理器 | www.ti.com.cn/dsp | 工业应用 | www.ti.com.cn/industrial |
| 时钟和计时器 | www.ti.com.cn/clockandtimers | 医疗电子 | www.ti.com.cn/medical |
| 接口 | www.ti.com.cn/interface | 安防应用 | www.ti.com.cn/security |
| 逻辑 | www.ti.com.cn/logic | 汽车电子 | www.ti.com.cn/automotive |
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| RFID 系统 | www.ti.com.cn/rfidsys | | |
| OMAP应用处理器 | www.ti.com/omap | | |
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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8860APW | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 8860A | Samples |
| DRV8860APWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 8860A | Samples |
| DRV8860PW | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 8860 | Samples |
| DRV8860PWPR | ACTIVE | HTSSOP | PWP | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | 8860PWP | Samples |
| DRV8860PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 8860 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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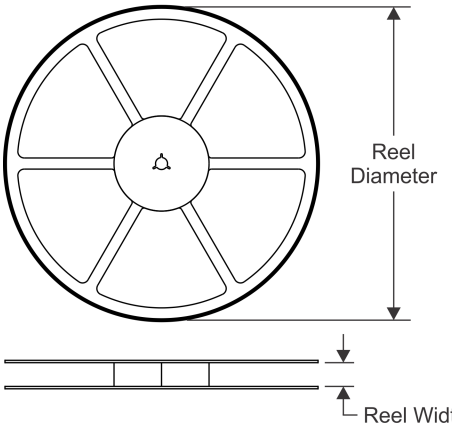
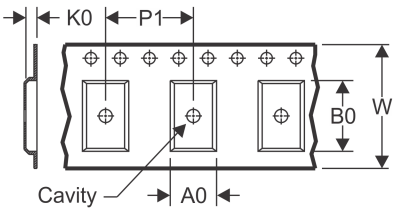
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

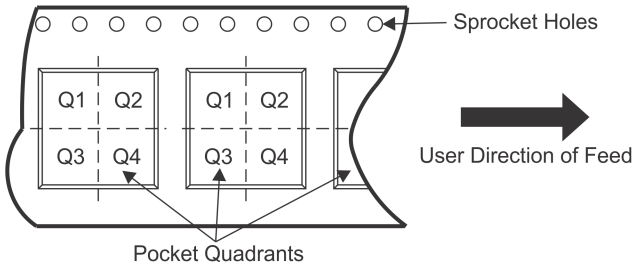



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

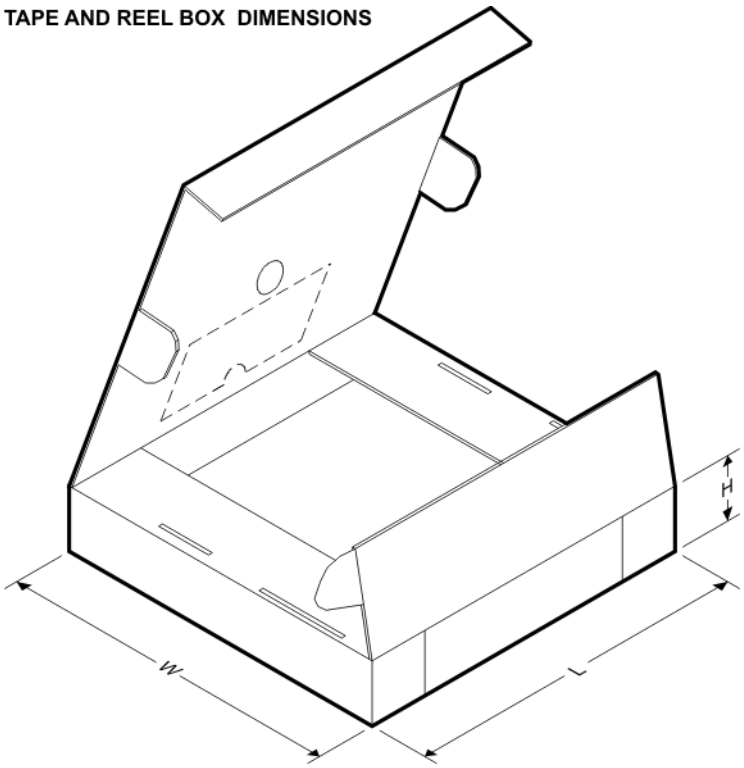
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8860APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8860PWPR | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8860PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

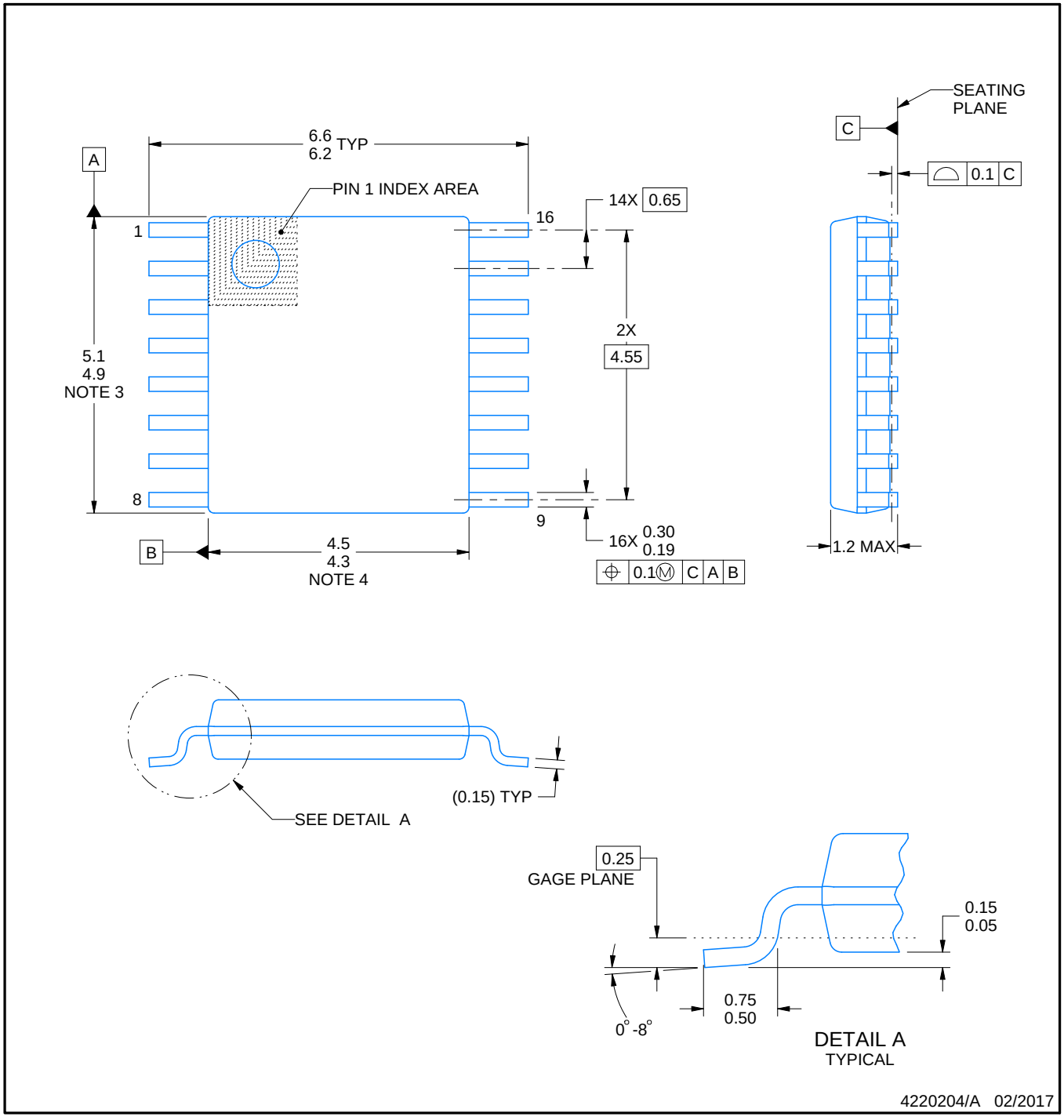
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8860APWR | TSSOP | PW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| DRV8860PWPR | HTSSOP | PWP | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| DRV8860PWR | TSSOP | PW | 16 | 2000 | 350.0 | 350.0 | 43.0 |

# PACKAGE OUTLINE

## PW0016A

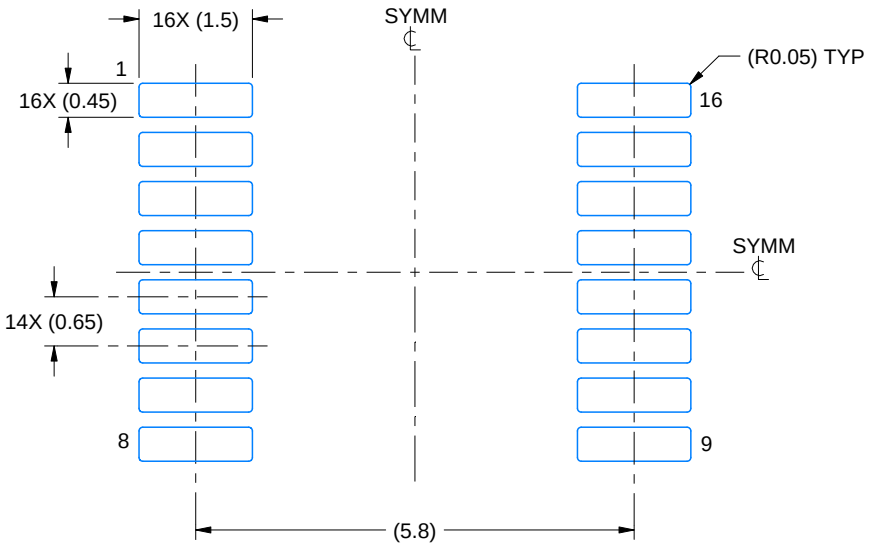
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

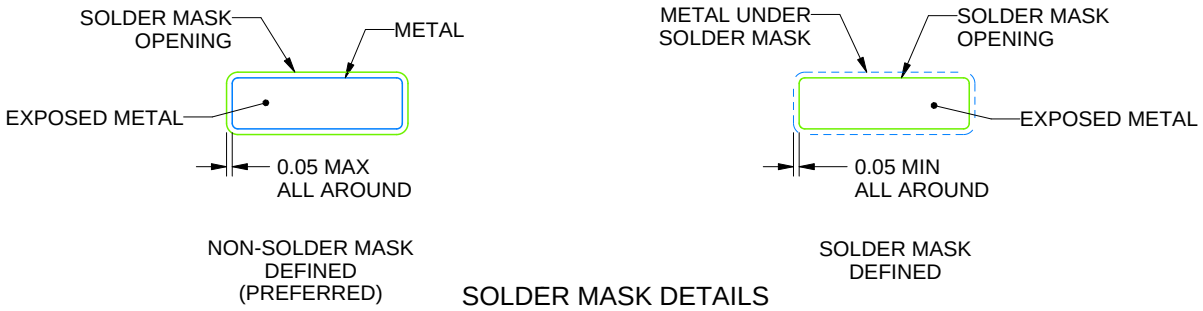



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

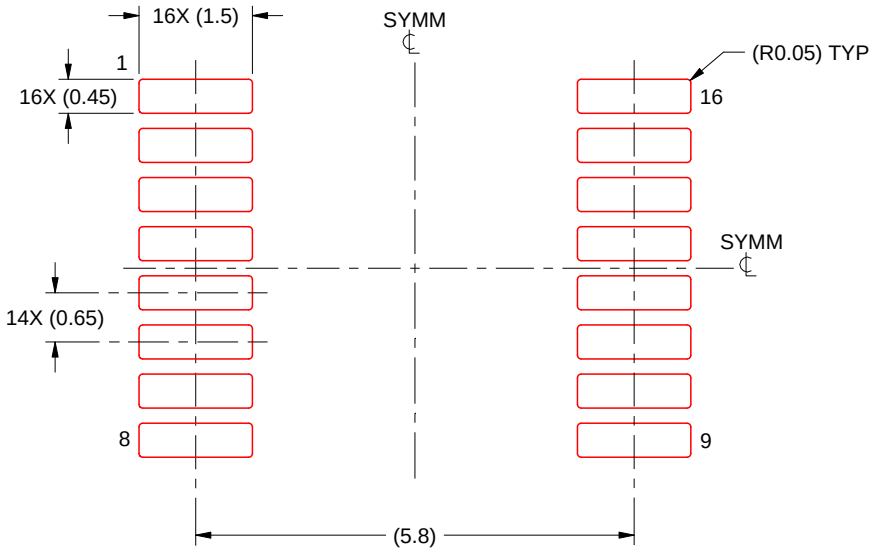



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

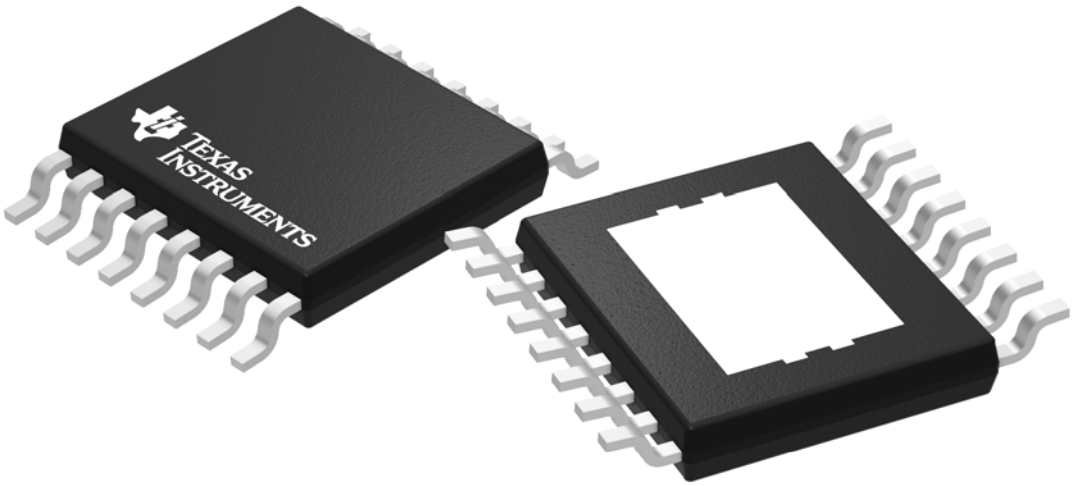
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

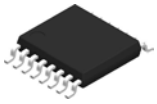
PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

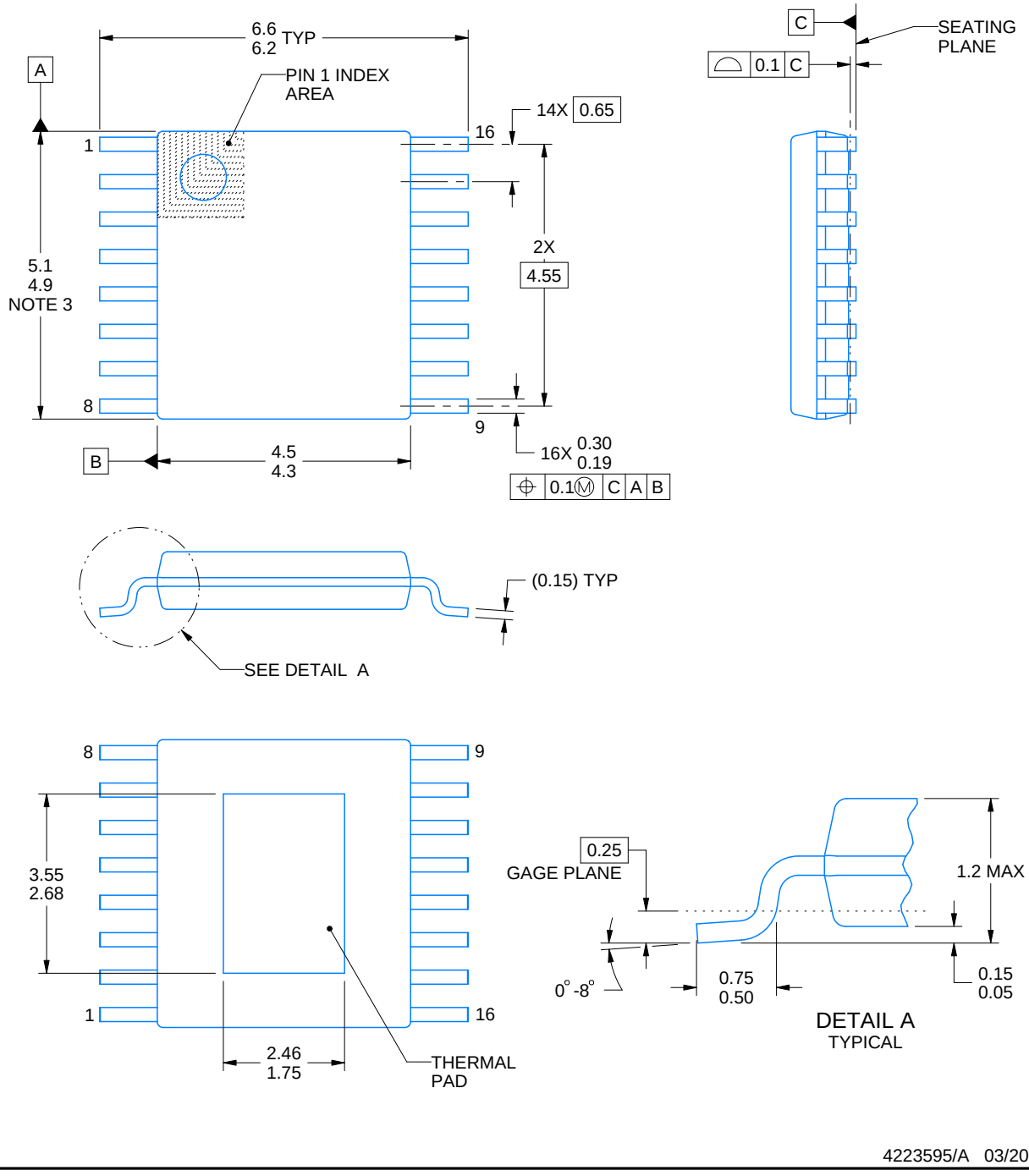
# PACKAGE OUTLINE

## PWP0016J



## PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

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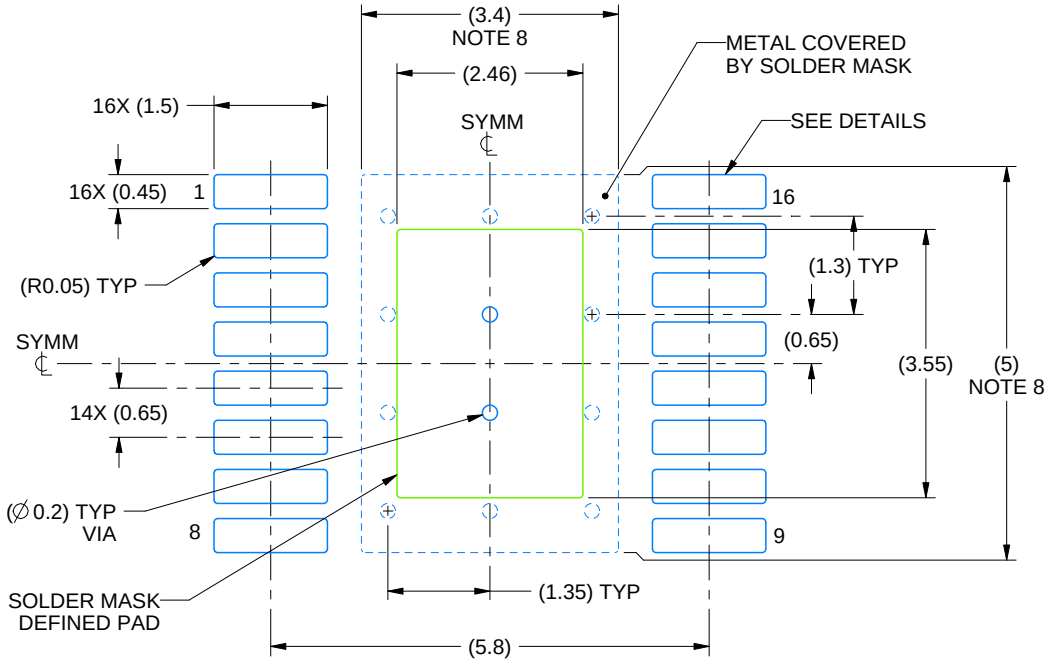
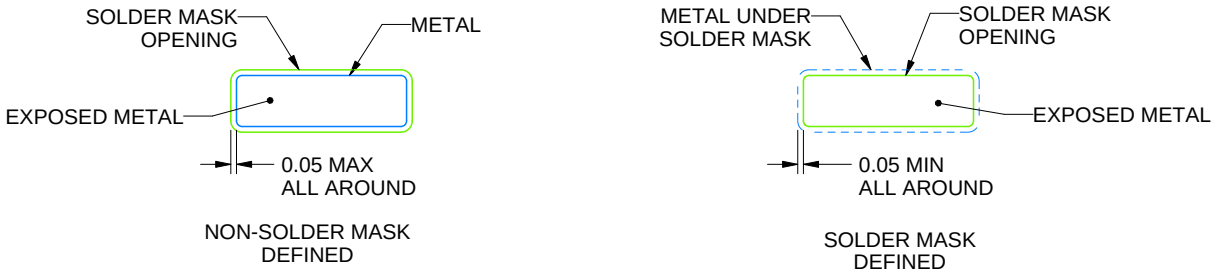
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

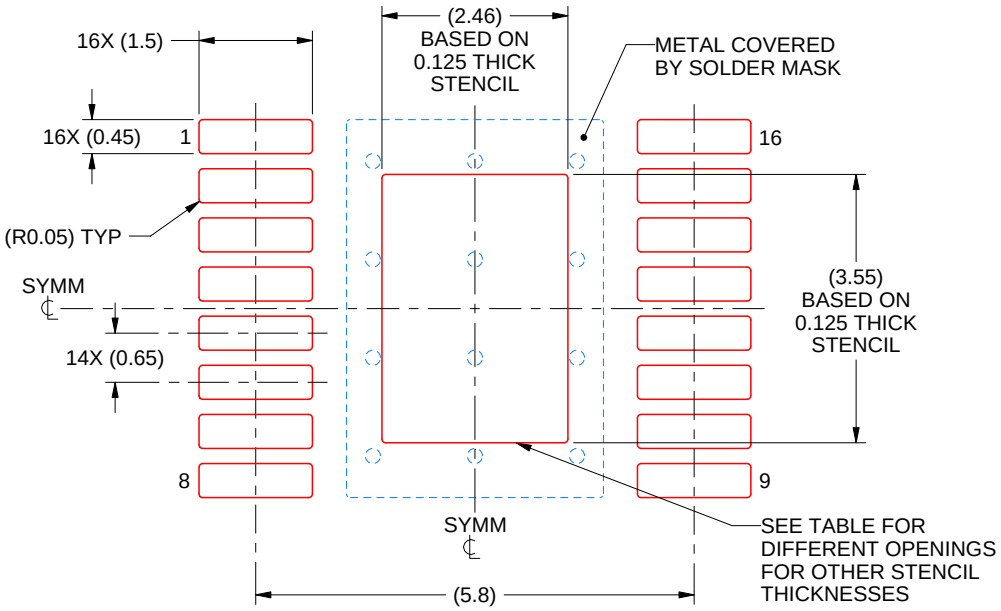



SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 2.75 X 3.97 |
| 0.125 | 2.46 X 3.55 (SHOWN) |
| 0.15 | 2.25 X 3.24 |
| 0.175 | 2.08 X 3.00 |

4223595/A 03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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