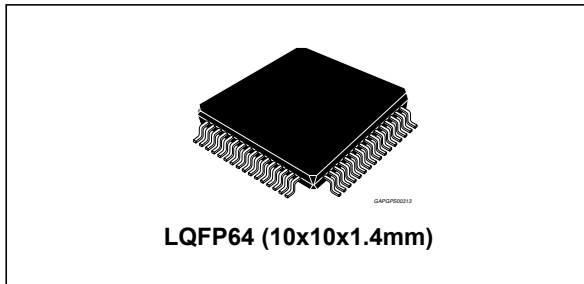


Automotive IC for a specific application of electric parking braking

Data brief



Features

- AEC-Q100 qualified
- Functional safety concept for ISO26262 compliance
- 4 High-side and Low-side gate pre-drivers for 8 external power NFETs
- Overcurrent protection with programmable thresholds
- Programmable and NFET independent thresholds for VDS monitoring
- 10 integrated Fully differential amplifiers with low offset, very precise gain, and self-test
- 10 separate ADC channels for digital processing of motor current and voltage measurement
- 32-bits - 10 MHz SPI with CRC for internal setting, self-test and diagnostics
- Full drive of external power NFETs down to 5.5 V battery input voltage
- Monitoring on Main power supply and continuous BIST for internal regulators
- Double Bandgap reference
- 4 General Purpose I/O stages (GPIO)
- Button Interface (9 configurable I/O pins) for monitoring and diagnostics in Normal and Sleep Mode.



- 2 Motor Speed Sensors (MSS) interfaces to acquire speed information feedbacks via external Hall sensors.
- System wake-up in Sleep Mode
- Watchdog (configurable via SPI)

Description

The L9370 targets the specific application of electric parking braking, suitable for system configuration in cable-puller or Motor Gear Unit (MGU).

The cores are two H-bridge driver stages to drive 8 external FETs for the rear wheels brakes actuators. The stages are fully driven and configurable via SPI, also in PWM control mode and protected against overcurrent, with drain-source and gate-source voltages monitoring.

A synchronized motor voltages and currents acquisition, is performed via full differential amplifiers with programmable and precise gain and low offset and 10 ADC sigma-delta modulators.

Two configurable HS/LS stages are present with programmable output voltage to drive LED arrays, with feedforward regulation.

2 Motor Speed Sensor interfaces (MSS) are available to acquire position feedback from brake actuators (shared with Lamp driver stage and GPIO).

The set of the interfaces is completed by 4 GPIO (General Purpose I/O) pins and a button interface allows to manage specific customer requirements from Electronic parking braking (EPB) button console both in Normal and Sleep Mode.

Table 1. Device summary

Order code	Package	Packing
L9370-TR	LQFP64	Tape & Reel

Contents

1	Block diagram and pin description	3
2	Package information	9
2.1	LQFP64 (10x10x1.4 mm) package information	9
2.2	LQFP64 (10x10x1.4 mm) marking information	11
3	Revision history	12

1 Block diagram and pin description

Figure 1. Simplified block diagram

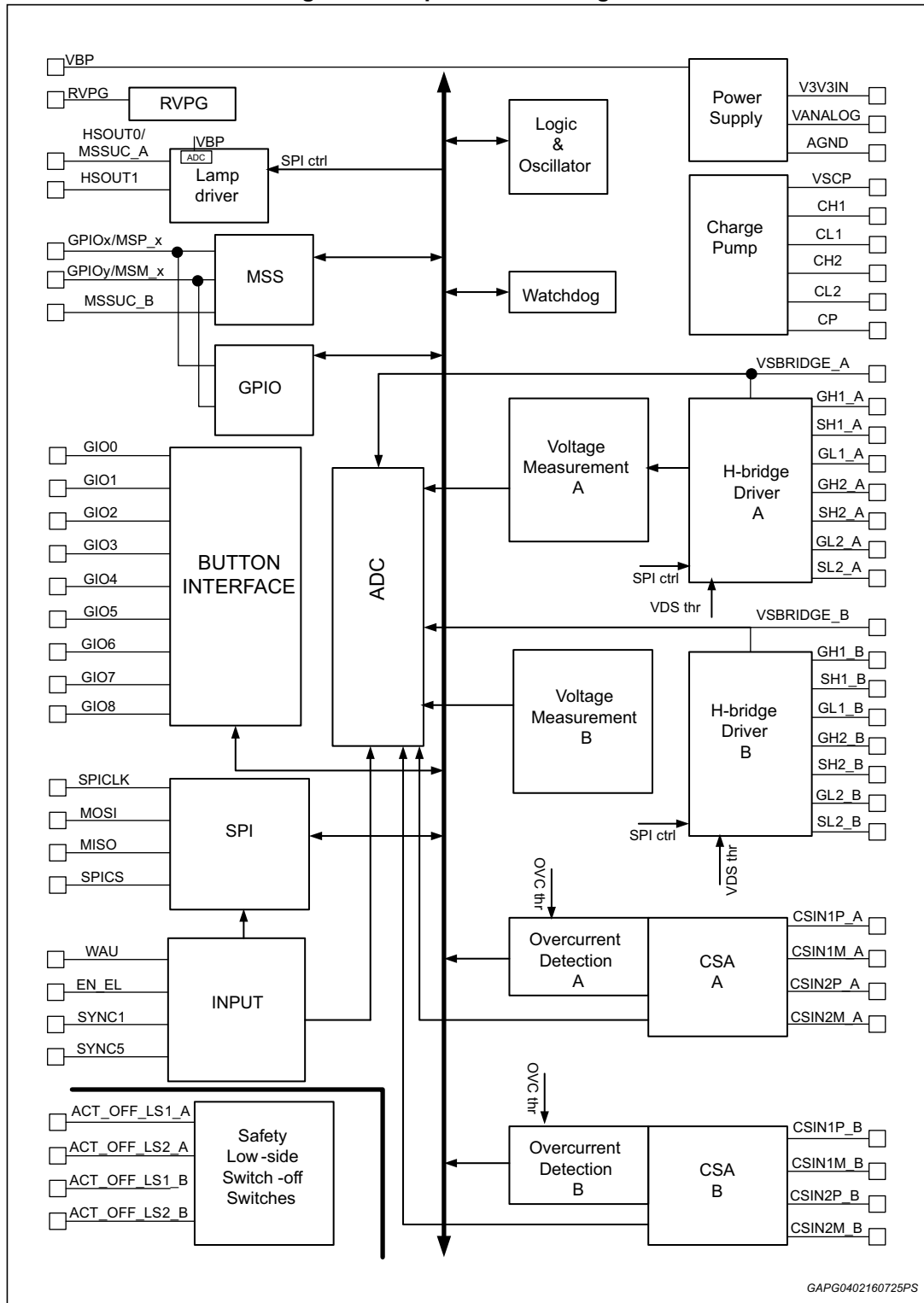
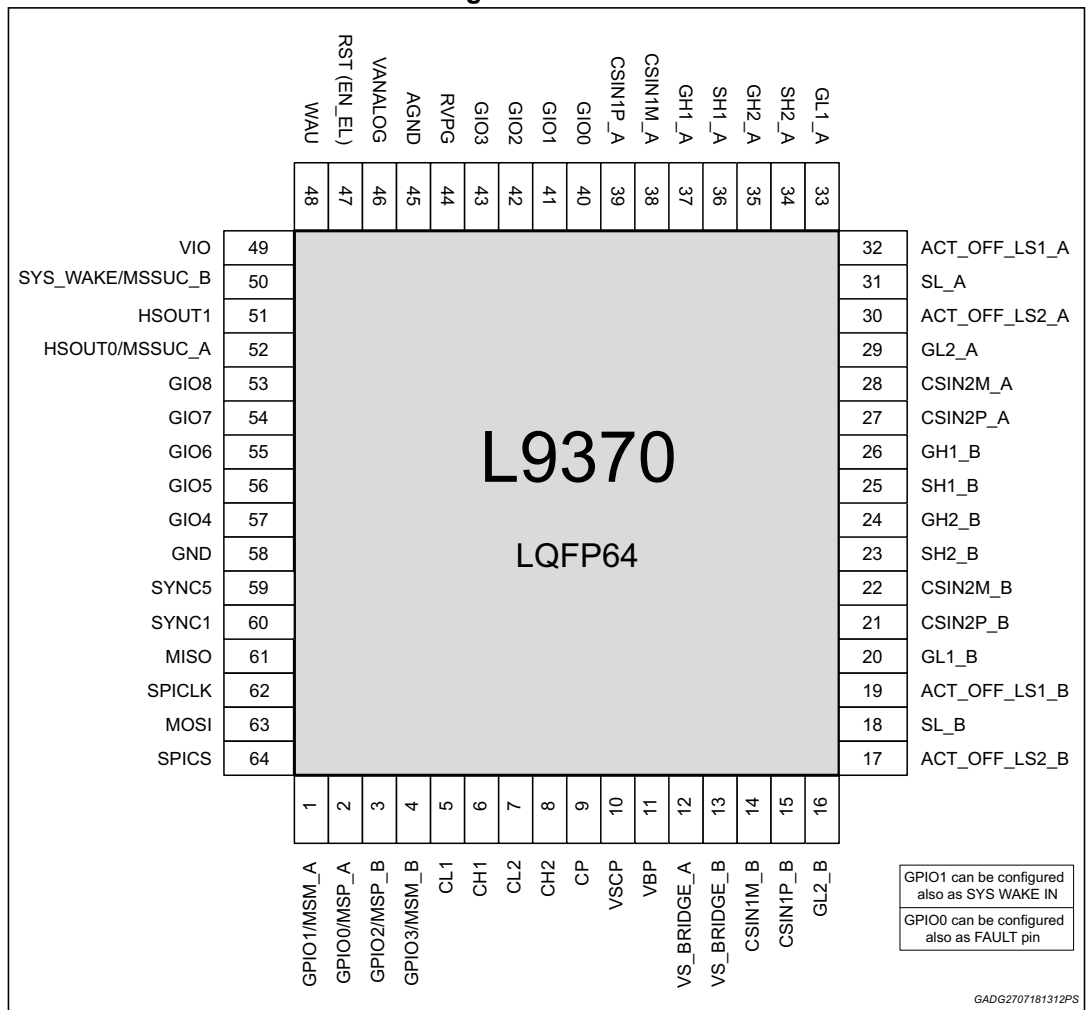


Figure 2. Pin out



PIN-out definition and related functions are described in the following [Table 2](#).

Table 2. Pin definition and brief function description

Pin #	Symbol	Function	I/O type
1	SYS_WAKE_IN / (GPIO1) / (MSM_A)	<p>SYS_WAKE_IN is a GPIO (General Purpose Programmable input/output) configured by default as digital input for system wake-up trigger in Sleep mode only. Configuration is stored in PROM. <i>(This function needs the SYS_WAKE as companion function to work properly, as SYS_WAKE_IN (feedback from ext network) is managed by logic to provide wake-up output pulse to System basis chip (SBC) during sleep mode (WAU=low). MSM_A is disabled due to pin sharing with GPIO block).</i></p> <p>GPIO1 = General Purpose Programmable input/output pin. After the 1st start-up SYS_WAKE_IN can be disabled via SPI in case not requested by application.</p> <p>MSM_A = Return pin for the motor speed sensor of stage A with monitoring and short-circuit protection. (SYS_WAKE_IN and GPIO1 functionalities are disabled)</p>	I/O
2	GPIO0 / MSP_A (FAULT PIN)	<p>GPIO0 = General Purpose Programmable input/output pin</p> <p>MSP_A = Supply pin for the motor speed sensor of stage A with monitoring short to GND protection and reverse supply protection</p> <p><i>(GPIO0 can be configured as Fault pin with programmable fault set via SPI and storage in PROM).</i></p>	I/O
3	GPIO2/MSP_B	<p>GPIO2 = General Purpose Programmable input/output pin</p> <p>MSP_B = Supply pin for the motor speed sensor of stage B with monitoring short to GND protection and reverse supply protection</p>	I/O
4	GPIO3/MSM_B	<p>GPIO3 = General Purpose Programmable input/output pin</p> <p>MSM_B = Return pin for the motor speed sensor of stage B with monitoring and short-circuit protection</p>	I/O
5	CL1	Low connection of the stage 1 external pump capacitor	I
6	CH1	High connection of the stage 1 external pump capacitor	I
7	CL2	Low connection of the stage 2 external pump capacitor	I
8	CH2	High connection of the stage 2 external pump capacitor	I
9	CP	Charge pump output voltage	O
10	VSCP	Charge pump supply voltage with monitoring	I
11	VBP	Battery supply and redundant supply for charge pump stage. <i>(Due to PROM data loss, configuration is lost if VBP < VBPpermanent)</i>	I
12	VSBRIDGE_A	Drain connection of the external H-Bridge High-side NFET and measurement input for H-bridge supply voltage (stage A)	I
13	VSBRIDGE_B	Drain connection of the external H-Bridge High-side NFET and measurement input for H-bridge supply voltage (stage B)	I
14	CSIN1M_B	Negative input pin of the external shunt #1 connected to CSA stage B	I

Table 2. Pin definition and brief function description (continued)

Pin #	Symbol	Function	I/O type
15	CSIN1P_B	Positive input pin of the external shunt #1 connected to CSA stage B	I
16	GL2_B	Gate connection of the H-Bridge Low-side NFET for wheel brake actuator B	O
17	ACT_OFF_LS2_B	Safety LS switch-off switches for H-bridge stage B	I
18	SL_B	Source connection of the H-Bridge Low-side switches for wheel brake actuator B	I
19	ACT_OFF_LS1_B	Safety LS switch-off switches for stage H-bridge B	I
20	GL1_B	Gate connection of the H-Bridge Low-side NFET for right wheel brake actuator B	I
21	CSIN2P_B	Positive input signal of the external shunt #2 connected to redundant CSA for stage B	I
22	CSIN2M_B	Negative input signal of the external shunt #2 connected to redundant CSA for stage B	I
23	SH2_B	Source connection of the H-Bridge High-side NFET for wheel brake actuator B	I
24	GH2_B	Gate connection of the H-Bridge High-side NFET for wheel brake actuator B	O
25	SH1_B	Source connection of the H-Bridge High-side NFET for wheel brake actuator B	I
26	GH1_B	Gate connection of the H-Bridge High-side NFET for wheel brake actuator B	O
27	CSIN2P_A	Positive input signal of the external shunt #2 connected to redundant CSA stage for A	I
28	CSIN2M_A	Negative input signal of the external shunt #2 connected to redundant CSA for stage A	I
29	GL2_A	Gate connection of the H-Bridge Low-side NFET for wheel brake actuator A	O
30	ACT_OFF_LS2_A	Safety LS switch-off switch for stage H-bridge A	I
31	SL_A	Source connection of the H-Bridge Low-side switches for wheel brake actuator A	I
32	ACT_OFF_LS1_A	Safety LS switch-off switch for stage H-bridge A	I
33	GL1_A	Gate connection of the H-Bridge Low-side NFET for wheel brake actuator A	O
34	SH2_A	Source connection of the H-Bridge High-side NFET for wheel brake actuator A	I
35	GH2_A	Gate connection of the H-Bridge High-side NFET for wheel brake actuator A	O
36	SH1_A	Source connection of the H-Bridge High-side NFET for wheel brake actuator A	I

Table 2. Pin definition and brief function description (continued)

Pin #	Symbol	Function	I/O type
37	GH1_A	Gate connection of the H-Bridge High-side NFET for wheel brake actuator A	O
38	CSIN1M_A	Negative input signal of the external shunt #1 connected to CSA for stage A	I
39	CSIN1P_A	Positive input signal of the external shunt #1 connected to CSA for stage A	I
40	GIO0	Programmable Input / Output for Button Interface control	I/O
41	GIO1	Programmable Input / Output for Button Interface control	I/O
42	GIO2	Programmable Input / Output for Button Interface control	I/O
43	GIO3	Programmable Input / Output for Button Interface control	I/O
44	RVPG	Gate driver output for reverse voltage switch control	O
45	AGND	Analog reference ground connection	GND
46	VANALOG	L9370 generated Low noise analog voltage, supplies the internal current measurement path. <i>(It can be used to supply external circuits with low current consumption. External capacitor required for stabilization.)</i>	O
47	RST (EN_EL)	EN_EL : digital enable input for GPIO (default pin function). RST : High active Input Reset pin. <i>(Enabled via dedicated SPI bit. GPIO block can be enabled and configured independently)</i>	I
48	WAU	Wake-up input. <i>(digital input, low level active to enter Sleep Mode)</i>	I
49	VIO	3.3 V / 5 V compatible supply voltage for L9370 output buffers	I
50	SYS_WAKE/MSSUC_B	SYS_WAKE (default configuration at start-up) is a digital output pin to wake System basis chip (SBC) up as support for general diagnostics on the external button during Sleep Mode only. This function/pin needs the SYS_WAKE_IN as companion function to work properly. MSSUC_B is disabled due to pin sharing with GPIO block. In case the SYS_WAKE function is not requested by application, It can be disabled via SPI at 1 st start-up and the pin can be configured as: MSSUC_B = Motor speed sensor signal output to the μ C. <i>(MSS interface is disabled by default and its functionality is shared with Lamp driver HSOUT).</i>	O
51	HSOUT1	HSOUT1 = SPI programmable HS/LS current source for external bulb lamp or LED array with monitoring	O
52	HSOUT0/MSSUC_A	HSOUT0 = SPI programmable HS/LS current source for external bulb lamp or LED array with monitoring MSSUC_A = Motor speed sensor signal output to the μ C. <i>MSS interface is disabled by default.</i>	O
53	GIO8	Programmable Input / Output for Button Interface control	I/O

Table 2. Pin definition and brief function description (continued)

Pin #	Symbol	Function	I/O type
54	GIO7	Programmable Input / Output for Button Interface control	I/O
55	GIO6	Programmable Input / Output for Button Interface control	I/O
56	GIO5	Programmable Input / Output for Button Interface control	I/O
57	GIO4	Programmable Input / Output for Button Interface control	I/O
58	GND	Digital and power ground connection	GND
59	SYNC5	Synchronization signal from μC for ADC voltage/current measurement path	I
60	SYNC1	Synchronization signal from μC for ADC voltage/current measurement path	I
61	MISO	Serial data out for SPI communication to μC	O
62	SPICLK	Clock signal for SPI	I
63	MOSI	Serial data input for SPI communication from μC	I
64	SPICS	Chip select for SPI	I

Table 3. General conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Parameter ID
T_{junction}	Function temperature	(parameters guaranteed)	-40	-	175	$^{\circ}\text{C}$	L9370_194
R_{th}	Application specific R_{th}	(Housing mounted on 6-Layer PCB)	-	-	40	$^{\circ}\text{C}/\text{W}$	L9370_3052

2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 LQFP64 (10x10x1.4 mm) package information

Figure 3. LQFP64 (10x10x1.4 mm) package outline

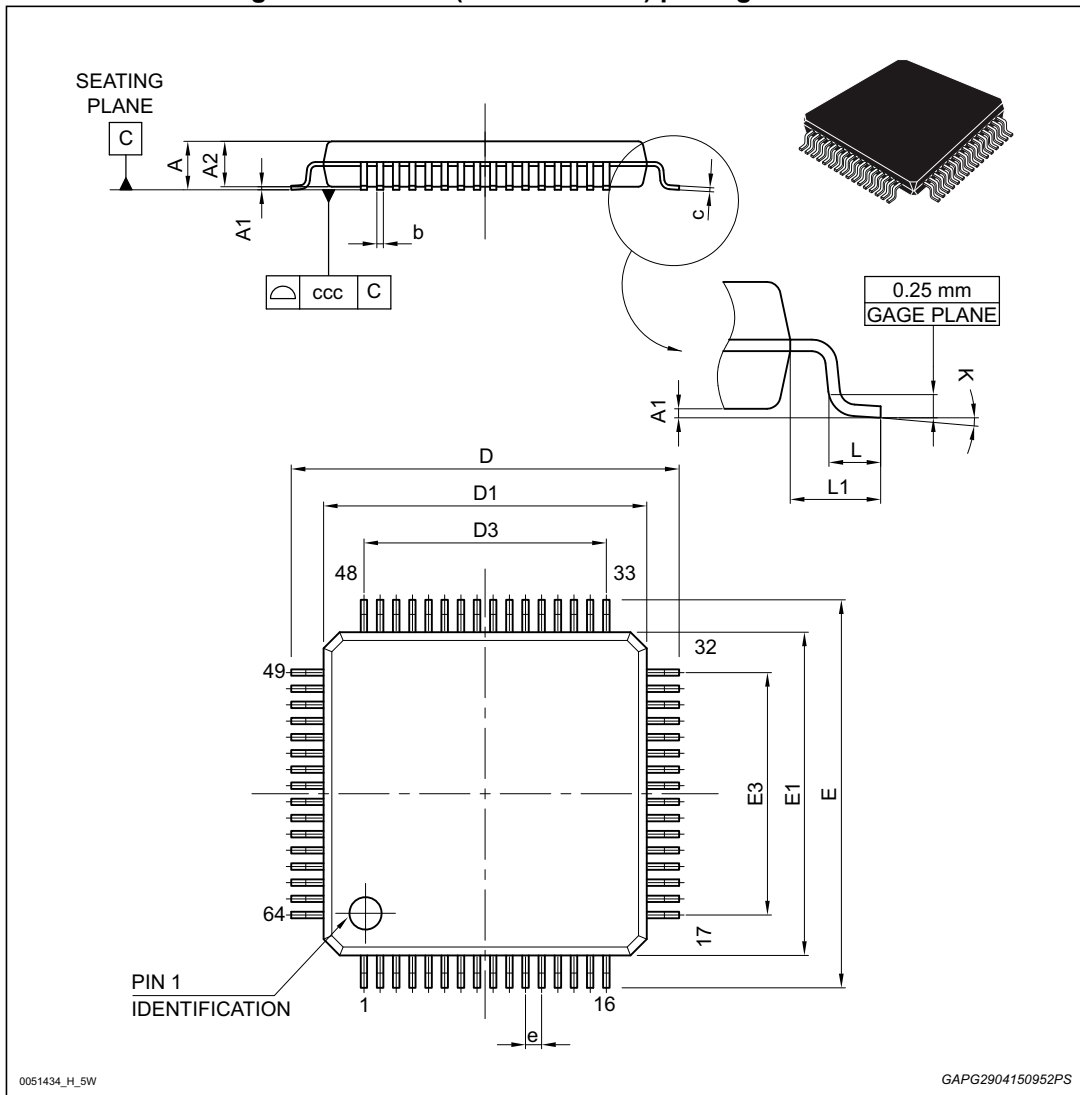


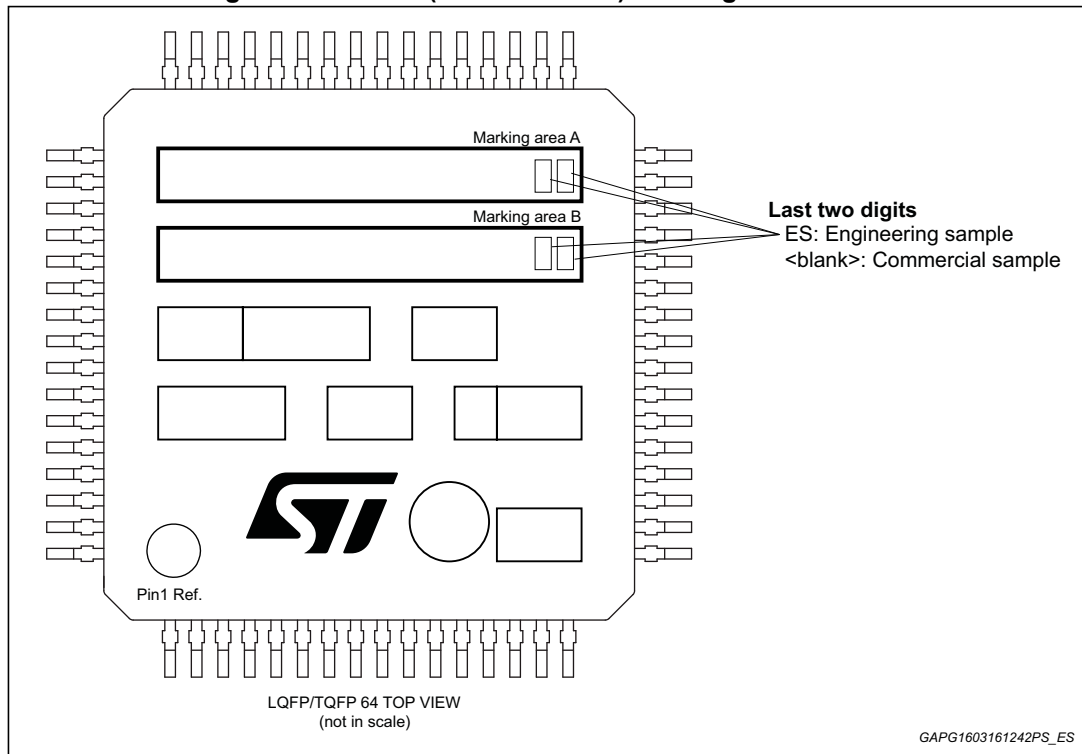
Table 4. LQFP64 (10x10x1.4 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.350	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.20	0.0035	-	0.0079
D	11.80	12.00	12.20	0.4646	0.4724	0.4803
D1	9.80	10.00	10.20	0.3858	0.3937	0.4016
D3	-	7.50	-	-	0.2953	-
E	11.80	12.00	12.20	0.4646	0.4724	0.4803
E1	9.80	10.00	10.20	0.3858	0.3937	0.4016
E3	-	7.50	-	-	0.2953	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0° (min.), 3.5° (typ.) 7° (max.)					
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2.2 LQFP64 (10x10x1.4 mm) marking information

Figure 4. LQFP64 (10x10x1.4 mm) marking information



Parts marked as 'ES' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event ST is liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

3 Revision history

Table 5. Document revision history

Date	Revision	Changes
11-Jan-2019	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved