AMC1411 High-Impedance, 2-V Input, Reinforced Isolated Amplifier in a 15-mm Stretched SOIC Package

1 Features

- 2-V, high-impedance input voltage range optimized for isolated voltage measurements
- Fixed gain: 1.0 V/V
- Low DC errors:
  - Offset error ±1.5 mV (max)
  - Offset drift: ±10 µV/°C (max)
  - Gain error: ±0.2% (max)
  - Gain drift: ±40 ppm/°C (max)
  - Nonlinearity 0.04% (max)
- 3.3-V or 5-V operation on high-side and low-side
- High CMTI: 100 kV/µs (min)
- 15-mm creepage, stretched SOIC package
- Reinforced isolation:
  - 10600-V_{PK} reinforced isolation per DIN VDE V 0884-11: 2017-01
  - 7500-V_{RMS} isolation for 1 minute per UL1577
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Isolated voltage sensing in:
  - Motor drives
  - Frequency inverters
  - Solar inverters
  - Wind turbine inverters

3 Description

The AMC1411 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier meets the industry standard for reinforced galvanic isolation of up to 7.5 kV_{RMS} and supports a working voltage of up to 1.6 kV_{RMS}.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage.

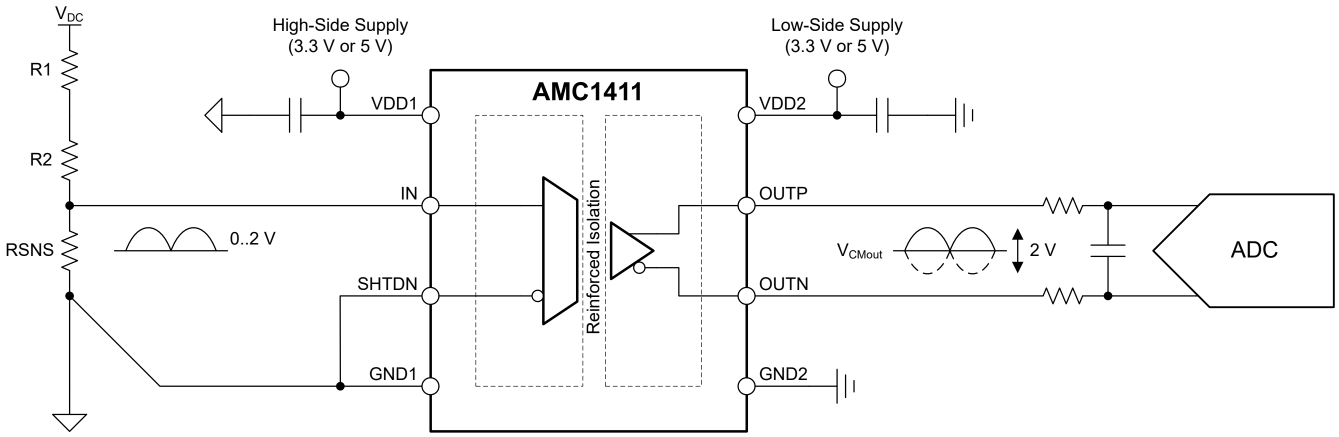
The high-impedance input of the AMC1411 is optimized for connection to high-impedance resistive dividers or other voltage signal sources with high output resistance. The excellent DC accuracy and low temperature drift supports accurate voltage sensing in DC/DC converters, solar or wind turbine inverters, and motor-drive applications over the extended industrial temperature range from –40°C to +125°C.

The integrated missing high-side supply detection feature simplifies system-level design and diagnostics.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1411	SOIC (8)	6.4 mm × 14.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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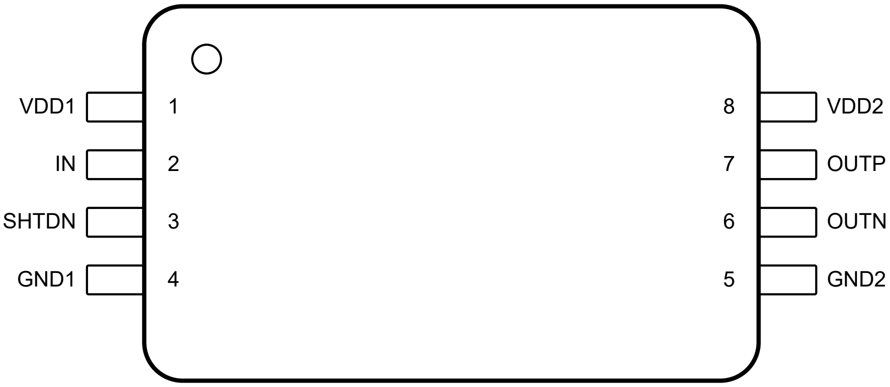
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2021	*	Initial Release

5 Pin Configuration and Functions



Not to scale

Figure 5-1. DWV Package, 8-Pin SOIC, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	**NAME**		
1	VDD1	High-side power	High-side power supply(1)
2	INP	Analog input	Analog input
3	SHTDN	Digital input	Shutdown input, active high, with internal pullup resistor (typical value: 100 kΩ)
4	GND1	High-side ground	High-side analog ground
5	GND2	Low-side ground	Low-side analog ground
6	OUTN	Analog output	Inverting analog output
7	OUTP	Analog output	Noninverting analog output
8	VDD2	Low-side power	Low-side power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Input voltage	IN	GND1 – 6	VDD1 + 0.5	V
	SHTDN	GND1 – 0.5	VDD1 + 0.5	
Output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* table. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1	3	5	5.5	V
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Input voltage before clipping output	IN to GND1		2.516		V
V_{FSR}	Specified linear full-scale voltage	IN to GND1	–0.1		2	V
DIGITAL INPUT						
	Input voltage	SHTDN to GND1	0		VDD1	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–55		125	°C
	Specified ambient temperature		–40		125	

6.4 Thermal Information

THERMAL METRIC[1]		AMC1411 DWL (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	26.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	98	mW
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 3.6 V	30	mW
		VDD1 = 5.5 V	53	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
		VDD2 = 5.5 V	45	

ADVANCE INFORMATION

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 14.7	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 15.7	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2256	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1600	V_{RMS}
		At DC voltage	2256	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	10600	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	12730	
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(3)	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 7500\ V_{RMS}$ or 10600 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 9000\ V_{RMS}$, t = 1 s (100% production test)	7500	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: pending	Certificate number: pending

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = TBD°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C			360	mA
		$R_{\theta JA}$ = TBD°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C			550	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = TBD°C/W, T_J = 150°C, T_A = 25°C			1980	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

ADVANCE INFORMATION

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, IN = –0.1 V to +2 V, and SHTDN = GND1 = 0 V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{OS}	Input offset voltage	T_A = 25°C, 4.5V ≤ VDD1 ≤ 5.5V(1) (2)	–1.5	±0.4	+1.5	mV
		T_A = 25°C, 3.0V ≤ VDD1 ≤ 5.5V(1) (2) (3)	–2.5	–1.1	+2.5	
TCV_{OS}	Input offset thermal drift(1) (2) (4)		–10	±3	+10	μV/°C
R_{IN}	Input resistance			1		GΩ
I_{IB}	Input bias current	IN = GND1	–15	3.5	15	nA
TCI_{IB}	Input bias current drift			±10		pA/°C
C_{IN}	Input capacitance	f_{IN} = 275 kHz		7		pF
ANALOG OUTPUT						
	Nominal gain			1		
E_G	Gain error(1)	at T_A = 25°C	–0.2%	±0.05%	0.2%	
TCE_G	Gain error drift(1) (5)		–40	±5	40	ppm/°C
	Nonlineartity(1)		–0.04%	±0.01%	+0.04%	
	Nonlinearity thermal drift			1		ppm/°C
THD	Total harmonic distortion	IN = 2 V, f_{IN} = 10 kHz, BW = 10 kHz		–87		dB
SNR	Signal-to-noise ratio	V_{IN} = 2 V, f_{IN} = 1 kHz, BW = 10 kHz	79	82.6		dB
		IN = 2 V, f_{IN} = 10 kHz, BW = 100 kHz		70.9		
	Output noise	IN = GND1, BW = 100 kHz		220		μVrms
PSRR	Power-supply rejection ratio(2)	vs VDD1, at DC		–65		dB
		vs VDD2, at DC		–85		
		vs VDD1, 10 kHz / 100 mV ripple		–65		
		vs VDD2, 10 kHz / 100 mV ripple		–70		
V_{CMout}	Output common-mode voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	$V_{OUT} = (V_{OUTP} – V_{OUTN})$; $V_{IN} > V_{Clipping}$		2.49		V
$V_{Failsafe}$	Failsafe differential output voltage	SHTDN = high, or VDD1 undervoltage, or VDD1 missing		–2.6	–2.5	V
BW	Output bandwidth		220	275		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		<0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, IN = GND1, outputs shorted to either GND or VDD2		14		mA
CMTI	Common-mode transient immunity		100	150		kV/μs
DIGITAL INPUT						
I_{IN}	Input current	SHTDN pin, GND1 ≤ SHTDN ≤ VDD1	–70		1	μA
C_{IN}	Input capacitance	SHTDN pin		5		pF
V_{IH}	High-level input voltage		0.7 × VDD1		VDD1 + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × VDD1	V

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, IN = –0.1 V to +2 V, and SHTDN = GND1 = 0 V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold	VDD1 falling	1.75	2.53	2.7	V
I_{DD1}	High-side supply current	3.0 V < VDD1 < 3.6 V		6.0	8.4	mA
		4.5 V < VDD1 < 5.5 V, SHTDN = low		7.1	9.7	mA
		SHTDN = high		1.3		µA
I_{DD2}	Low-side supply current	3.0 V < VDD2 < 3.6 V		5.3	7.2	mA
		4.5 V < VDD2 < 5.5 V		5.9	8.1	mA

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) The typical value is at VDD1 = 3.3 V.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G\ (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25°C)} \times TempRange) \times 10^6$

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	IN to OUTx signal delay (50% - 10%)	Unfiltered output		1	1.5	µs
	IN to OUTx signal delay (50% - 50%)	Unfiltered output		1.6	2.1	µs
	IN to OUTx signal delay (50% - 90%)	Unfiltered output		2.5	3	µs
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to V_{OUTP}, V_{OUTN} valid, 0.1% settling		50	100	µs
t_{EN}	Device enable time	SHTDN high to low		50	100	µs
t_{SHTDN}	Device shutdown time	SHTDN low to high		3	10	µs

6.11 Timing Diagram

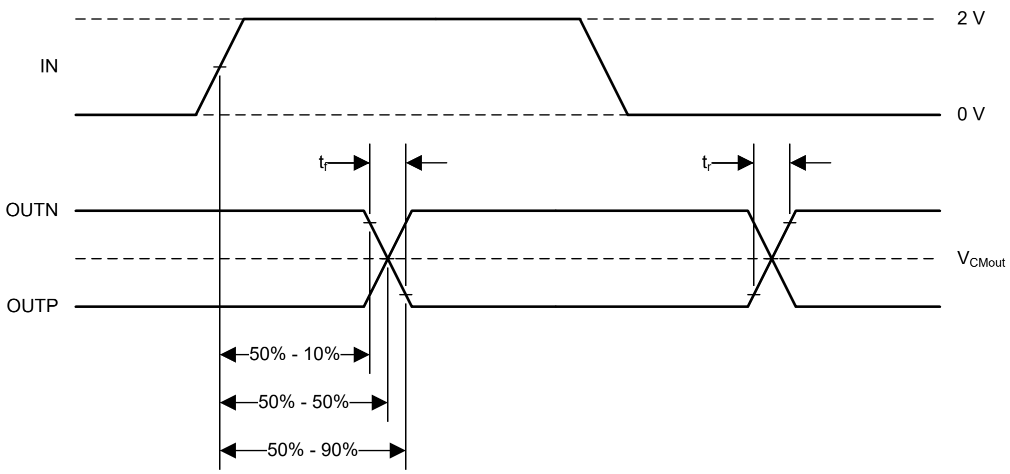


Figure 6-1. Rise, Fall, and Delay Time Definition

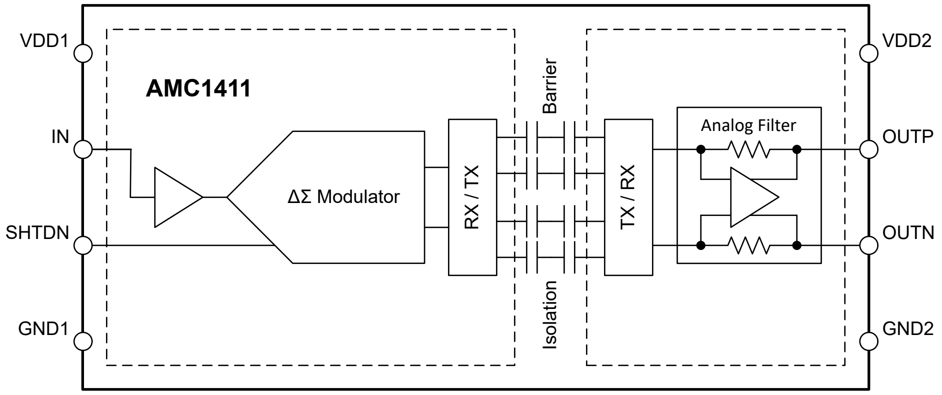
7 Detailed Description

7.1 Overview

The AMC1411 is a single-ended input, precision, isolated amplifier with a high input-impedance and wide input voltage range. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier and separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1411 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The single-ended, high-impedance input stage of the AMC1411 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal IN. First, if the input voltage V_{IN} exceeds the range specified in the *Absolute Maximum Ratings* table, the input current must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device is ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) as specified in the *Recommended Operating Conditions* table.

7.3.2 Isolation Channel Signal Transmission

The AMC1411 uses an on-off keying (OOK) modulation scheme, as shown in Figure 7-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1411 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1411 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

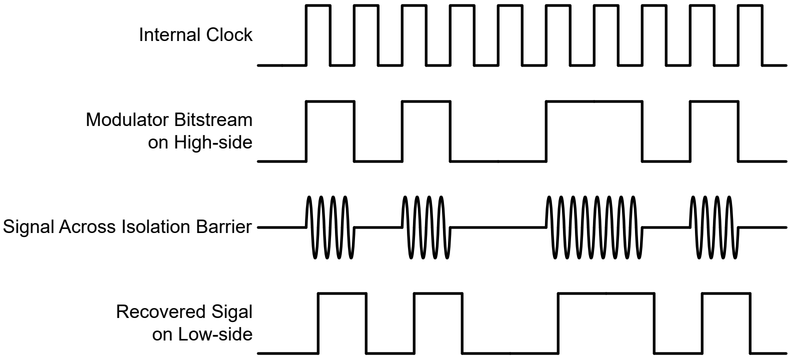


Figure 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC1411 provides a differential analog output on the OUTP and OUTN pins. For input voltages V_{IN} in the range from –0.1 V to +2 V, the device provides a linear response with a nominal gain of 1. For example, for an input voltage of 2 V, the differential output voltage (V_{OUTP} – V_{OUTN}) is 2 V. At zero input (IN shorted to GND1), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For input voltages greater than 2 V but less than approximately 2.5 V, the differential output voltage continues to increase but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in Figure 7-2, if the input voltage exceeds the $V_{Clipping}$ value.

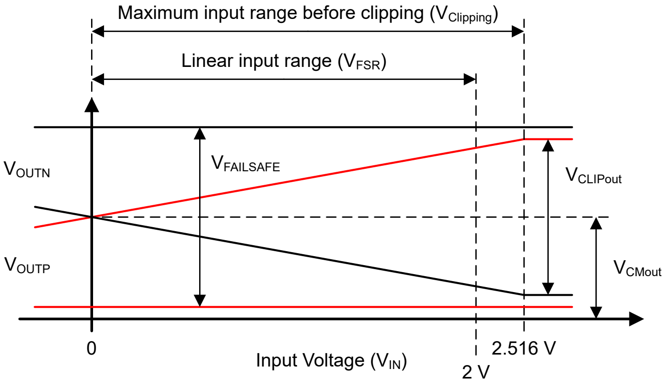


Figure 7-2. Output Behavior of the AMC1411

The AMC1411 output offers a fail-safe feature that simplifies diagnostics on system level. Figure 7-2 shows the fail-safe mode, in which the AMC1411 outputs a negative differential output voltage that does not occur under normal operating conditions. The failsafe output is active in three cases:

- When the high-side supply VDD1 of the AMC1411 device is missing
- When the high-side supply VDD1 falls below the undervoltage threshold $VDD1_{UV}$
- When the SHTDN pin is pulled high

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for failsafe detection on a system level.

7.4 Device Functional Modes

The AMC1411 is operational when the power supplies VDD1 and VDD2 are applied as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The high input impedance, low input bias current, excellent accuracy, and low temperature drift make the AMC1411 a high-performance solution for industrial applications where voltage sensing in the presence of high common-mode voltage levels is required.

8.2 Typical Application

Most reinforced isolated amplifiers come in a SOIC package with less than 9 mm of clearance and creepage specification. Equipment with working voltages greater than 1000 V_{RMS}, impulse voltage requirements greater than 8000 V, or systems designed for altitudes greater than 2000 m or for a pollution degree 2 or higher, may require clearance and creepage distances greater than 9 mm depending on the overvoltage category the system is designed for. Such an example is a 690-V unearthed (IT) 3-phase power network for high-reliability industrial applications.

The AMC1411 comes in a SOIC package with greater than 15 mm of creepage distance and is specifically designed for use in high-voltage systems that require accurate voltage monitoring and reinforced isolation between high-voltage and low-voltage parts of the system.

Figure 8-1 shows a 3-phase motor-drive application that uses the AMC1411 to monitor the 1200-V DC-link voltage. The DC-link voltage is divided down to an approximate 2-V level across the bottom resistor (RSNS) of a high-impedance resistive divider that is sensed by the AMC1411. The output of the AMC1411 is a differential analog output voltage of the same value as the input voltage but is galvanically isolated from the high-side by a reinforced isolation barrier.

The high isolation voltage rating and high common-mode transient immunity (CMTI) of the AMC1411 ensure reliable and accurate operation even in high-noise environments.

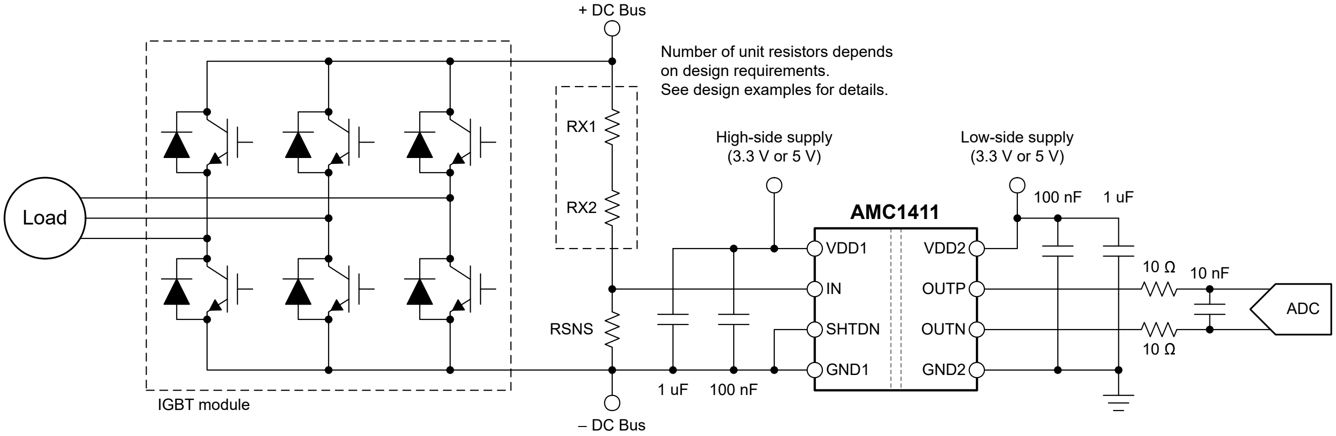


Figure 8-1. Using the AMC1411 for DC Link Voltage Sensing in Frequency Inverters

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
System input voltage	3-phase, 690 V, 50 Hz, IT system
Overvoltage category	II
Altitude	≤4000 m
DC-link voltage	1200 V (maximum)
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Maximum resistor operating voltage	75 V
Voltage drop across the sense resistor (RSNS) for a linear response	2 V (maximum)
Current through the resistive divider, I_{CROSS}	300 µA

8.2.2 Detailed Design Procedure

The 300-µA cross-current requirement at the maximum DC-link voltage (1200 V) determines that the total impedance of the resistive divider is 4 MΩ. The impedance of the resistive divider is dominated by the top portion (shown exemplary as RX1 and RX2 in Figure 8-1) and the voltage drop across RSNS can be neglected for a moment. The maximum allowed voltage drop per unit resistor is specified as 75 V; therefore, the minimum number of unit resistors in the top portion of the resistive divider is 1200 V / 75 V = 16. The calculated unit value is 4 MΩ / 16 = 250 kΩ and the next closest value from the E96 series is 249 kΩ.

RSNS is sized such that the voltage drop across the resistor at the maximum DC-link voltage (1200 V) equals the linear full-scale range input voltage (V_{FSR}) of the AMC1411 that is 2 V. This voltage is calculated as RSNS = V_{FSR} / ($V_{DC\text{-link, max}}$ – V_{FSR}) x R_{TOP}, where R_{TOP} is the total value of the top resistor string (16 x 249 kΩ = 3984 kΩ). RSNS is calculated as 6.65 kΩ and matches a value from the E96 series.

Table 8-2 summarizes the design of the resistive divider.

Table 8-2. Resistor Value Example

PARAMETER	VALUE
Unit resistor value, RX	249 kΩ
Number of unit resistors	16
Sense resistor value, RSNS	6.65 kΩ
Total resistance value	3990.65 kΩ
Resulting current through resistive divider, I_{CROSS}	300.7 µA
Resulting full-scale voltage drop across sense resistor RSNS	2.000 V
Power dissipated in unit resistor RX	22.5 mW
Total power dissipated in resistive divider	361 mW

8.2.2.1 Insulation Coordination

In this example of a motor drive application, isolation between the high-voltage and low-voltage parts of the system must be checked against the requirements of the IEC61800-5-1 standard for electrical power drive systems. Isolation must be designed to withstand the rated impulse voltage, temporary overvoltage, and the working voltage. In addition, the physical distance between exposed metal parts on the high- and low-voltage side must meet the minimum creepage and clearance requirements.

Table B.1 of the IEC60664-1 standard defines the impulse voltage for a 690-V, 3-phase, unearthed system (such as an IT system, OVC II) as 6000 V, which is less than the V_{IOSM} (8000 V_{PK}) of the AMC1411.

Table B.1 of the IEC60664-1 standard also defines the system voltage of a 690-V, 3-phase IT system as 600 V. According to table 7 of the IEC61800-5-1 standard, the temporary overvoltage for a system voltage of 600 V is 3110 V_{PK}, which is lower than the V_{IOSM} (10500 V) of the AMC1411.

The working voltage in this example is 1200 V_{DC} or 850 V_{RMS} and is also lower than V_{IOWM} (2256 V_{DC}) of the AMC1411.

The minimum clearance for a 6000-V impulse voltage according the IEC61800-5-1, table 9, is 8 mm for reinforced isolation. The equipment is designed to operate up to 4000 m of altitude and, therefore, the minimum clearance must be multiplied by a factor of 1.29 according to IEC60664-1 table A.2, resulting in a minimum clearance of 10.4 mm.

Finally, the minimum creepage distance for a working voltage of 850 V_{RMS}, insulating material group I, pollution degree 2, reinforced isolation is 2 x 4.25 mm = 8.5 mm according to IEC61800-5-1 table 10. 4.25 mm is the interpolated value between the 800 V_{RMS} and 1000 V_{RMS} and is doubled for reinforced isolation. The 15-mm package of the AMC1411 exceeds the minimum requirements, both for clearance and creepage.

8.2.2.2 Input Filter Design

Placing an RC filter in front of the isolated amplifier improves signal-to-noise performance of the signal path. In practice, however, the impedance of the resistor divider is so high that adding a filter capacitor on the IN pin limits the signal bandwidth to an unacceptable low limit, such that the filter capacitor is omitted. When used, design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter

Most voltage-sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor (as shown in Figure 8-2) is sufficient to filter the input signal.

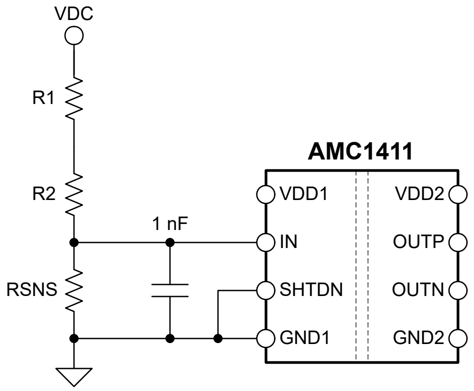


Figure 8-2. Input Filter

8.2.2.3 Differential-to-Single-Ended Output Conversion

Figure 8-3 shows an example of a TLV6001-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

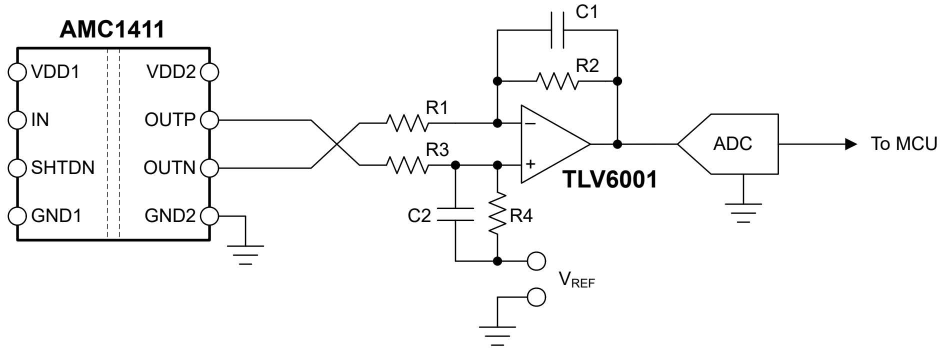


Figure 8-3. Connecting the AMC1411 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

8.2.3 Application Curve

One important aspect of system design is the effective detection of an overvoltage condition to protect switching devices and passive components from damage. To power off the system quickly in the event of an overvoltage condition, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC1411.

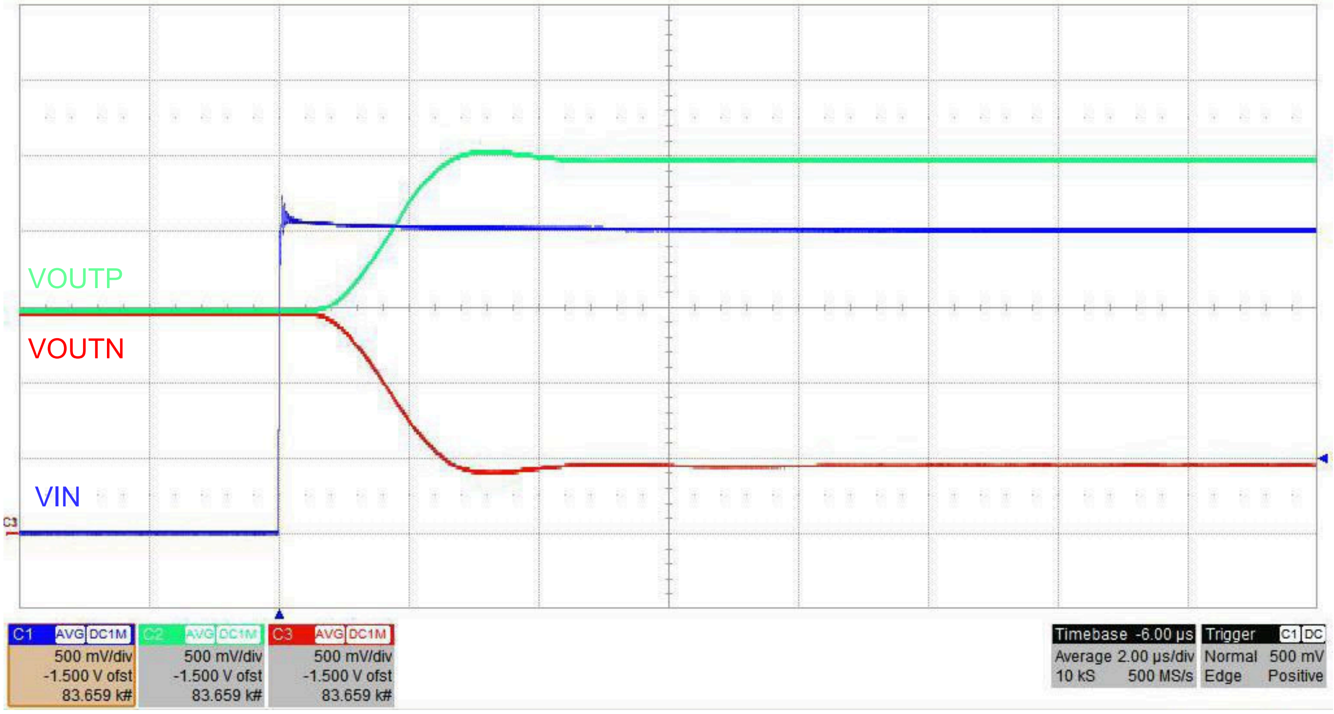


Figure 8-4. Step Response of the AMC1411

8.2.4 What To Do and What Not To Do

Do not leave the analog input (IN) of the AMC1411 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a negative input voltage that exceeds the specified input voltage range and the output of the device is invalid.

9 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC1411 is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC1411 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 9-1 shows the proper decoupling layout for the AMC1411.

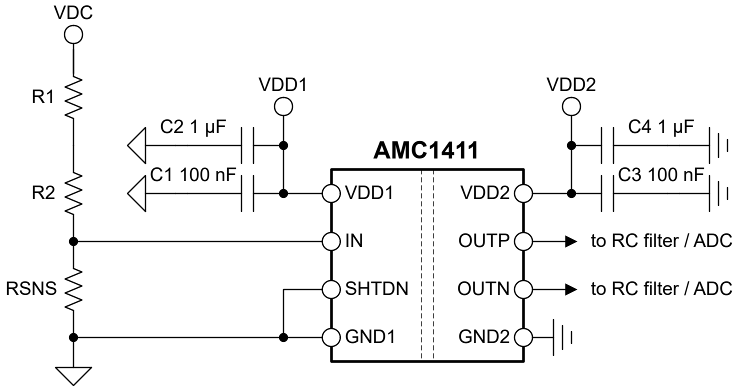


Figure 9-1. Decoupling of the AMC1411

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

10 Layout

10.1 Layout Guidelines

Figure 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1411 supply pins) and placement of the other components required by the device. For best performance, place the sense resistor close to the device input pin (IN).

10.2 Layout Example

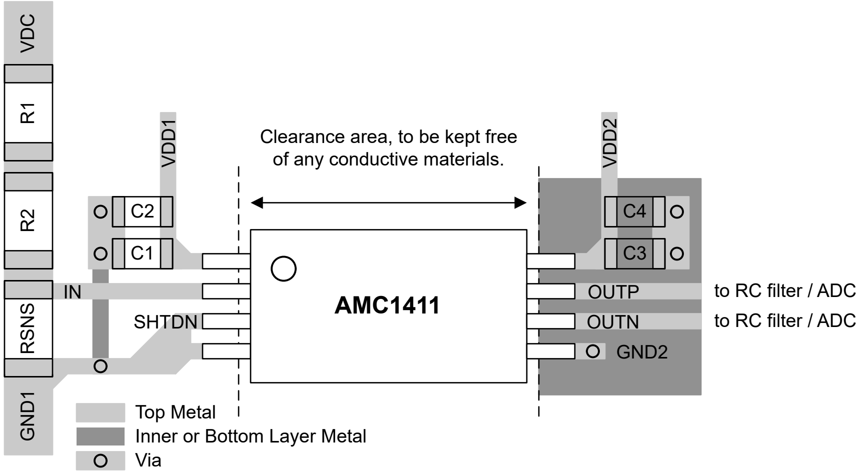


Figure 10-1. Recommended Layout of the AMC1411

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instrument, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* design guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

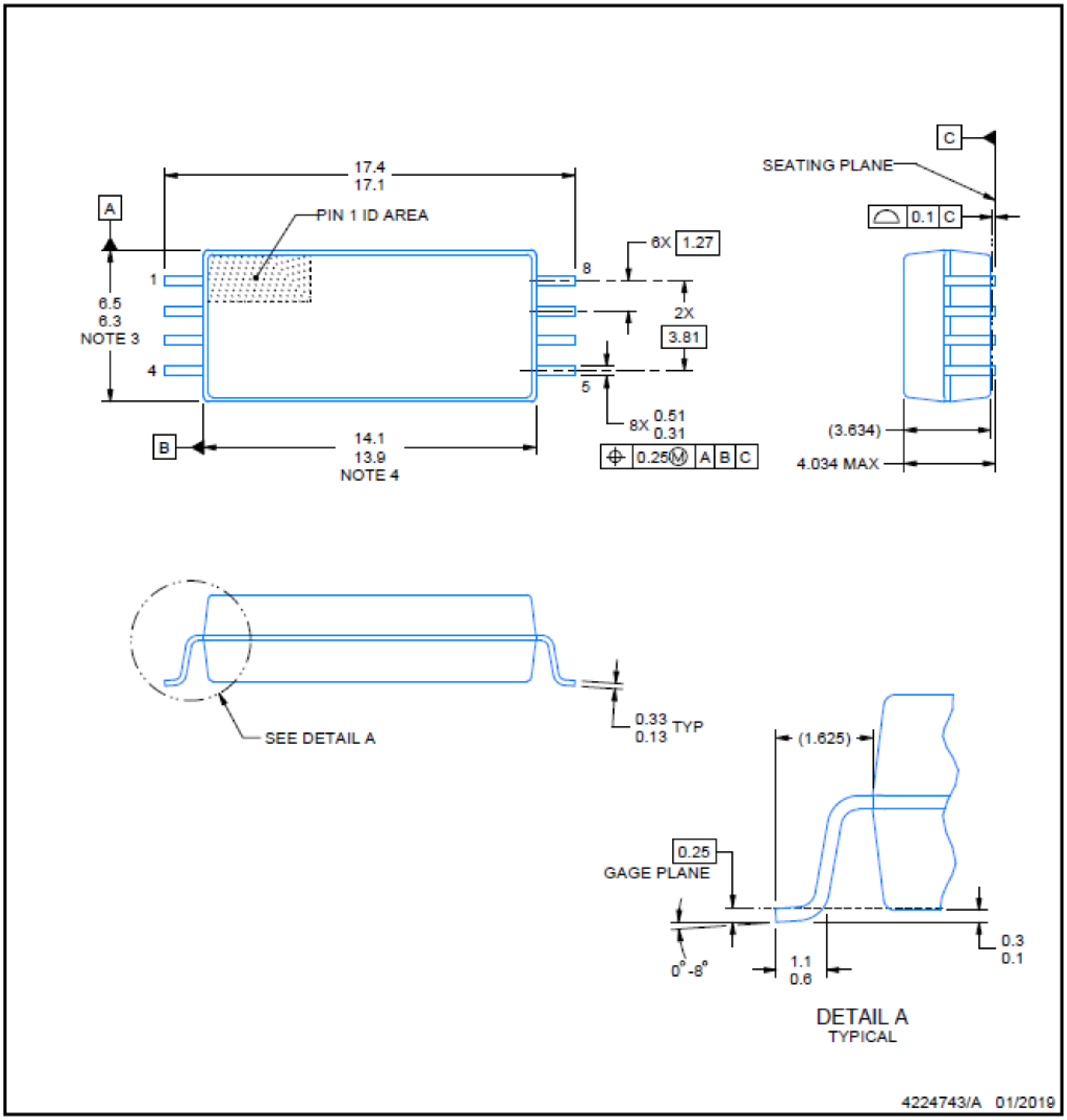
12.1 Mechanical Data

PACKAGE OUTLINE

DWL0008A

SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE



NOTES:

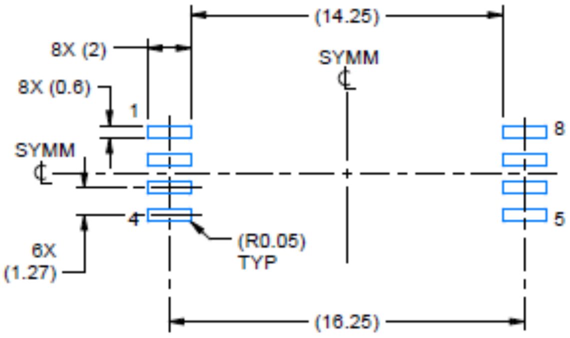
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

EXAMPLE BOARD LAYOUT

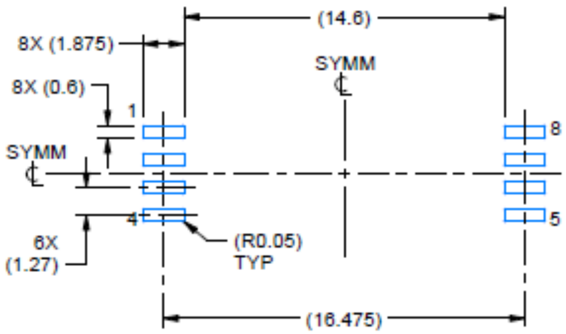
DWL0008A

SOIC - 4.034 mm max height

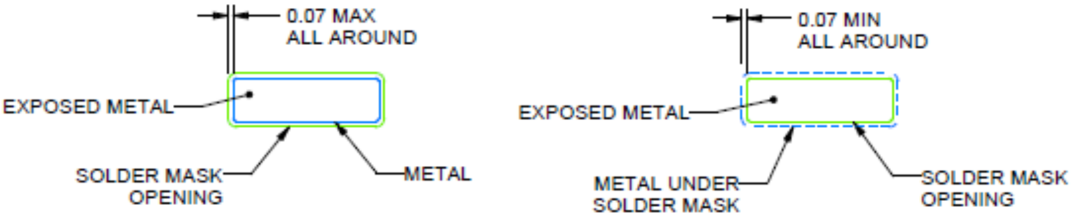
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
STANDARD
EXPOSED METAL SHOWN
SCALE:3X



LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
EXPOSED METAL SHOWN
SCALE:3X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224743/A 01/2019

ADVANCE INFORMATION

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

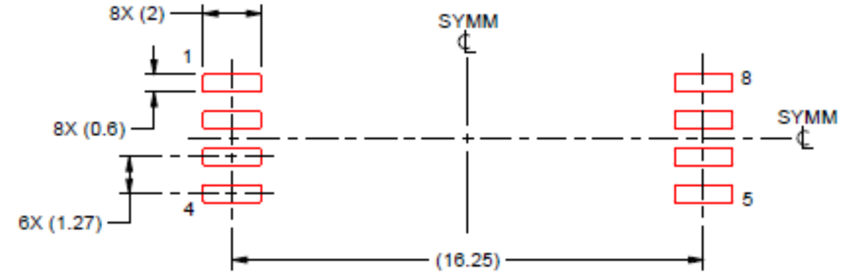
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

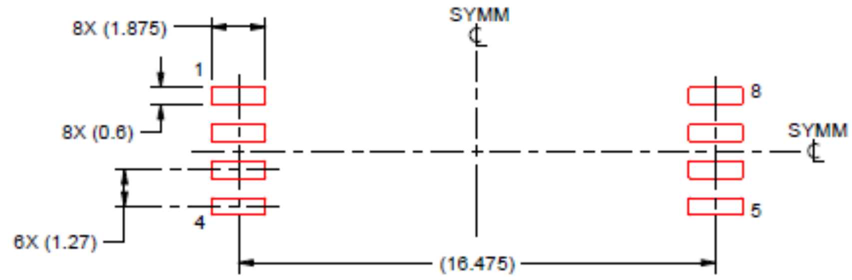
DWL0008A

SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4224743/A 01/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PAMC1411DWLR	ACTIVE	SOIC	DWL	8	500	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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