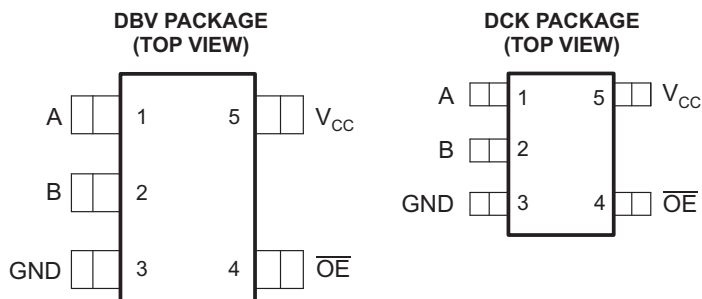


FEATURES

- 5- Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74CBTD1G384 features a single high-speed line switch. The switch is disabled when the output-enable (\overline{OE}) input is high. A diode to V_{CC} is integrated on the chip to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
-40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74CBTD1G384DBVR	P8D_
		Reel of 250	SN74CBTD1G384DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74CBTD1G384DCKR	P8_
		Reel of 250	SN74CBTD1G384DCKT	

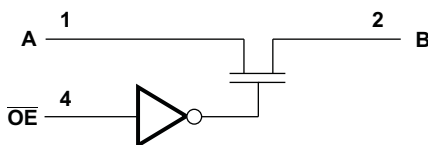
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



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SN74CBTD1G384

SINGLE FET BUS SWITCH

WITH LEVEL SHIFTING

SCDS066K–JULY 1998–REVISED JUNE 2006

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I	Input voltage range ⁽²⁾	–0.5	7	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current	$V_{IO} < 0$	–50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package	206	°C/W
		DCK package	252	
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA					−1.2	V	
V _{OH}		See Figure 2							
I _I		V _{CC} = 5.5 V, V _I = 5.5 V or GND					±1	μA	
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND					1.5	mA	
ΔI _{CC} ⁽²⁾	Control input	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND					2.5	mA	
C _i	Control input	V _I = 3 V or 0					2	pF	
C _{iO(OFF)}		V _O = 3 V or 0, \overline{OE} = V _{CC}					3.5	pF	
r _{on} ⁽³⁾		V _{CC} = 4.5 V	V _I = 0	I _I = 64 mA			5	7	Ω
				I _I = 30 mA			5	7	
			V _I = 2.4 V, I _I = 15 mA				35	50	

- (1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$
- (2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
- (3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

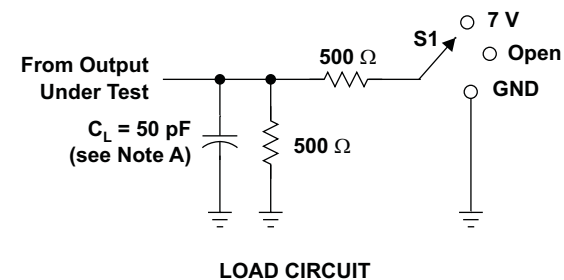
Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Figure 1](#))

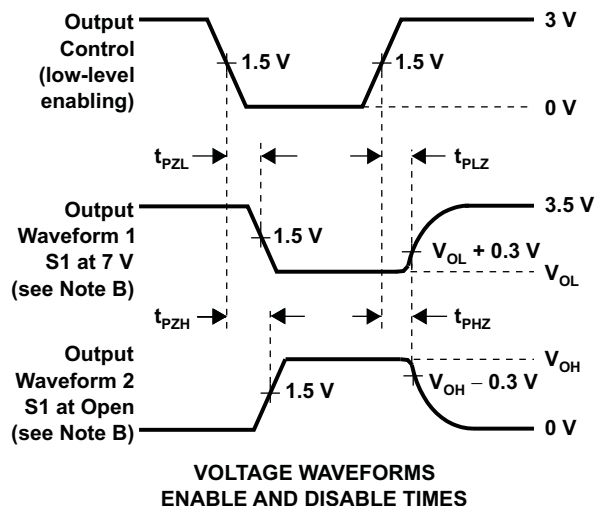
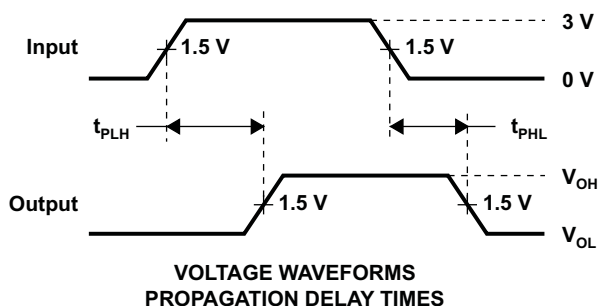
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^{(1)}$	A or B	B or A		0.25	ns
t_{en}	\overline{OE}	A or B	2	5.9	ns
t_{dis}	\overline{OE}	A or B	1	4.7	ns

- (1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

D. The output is measured with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

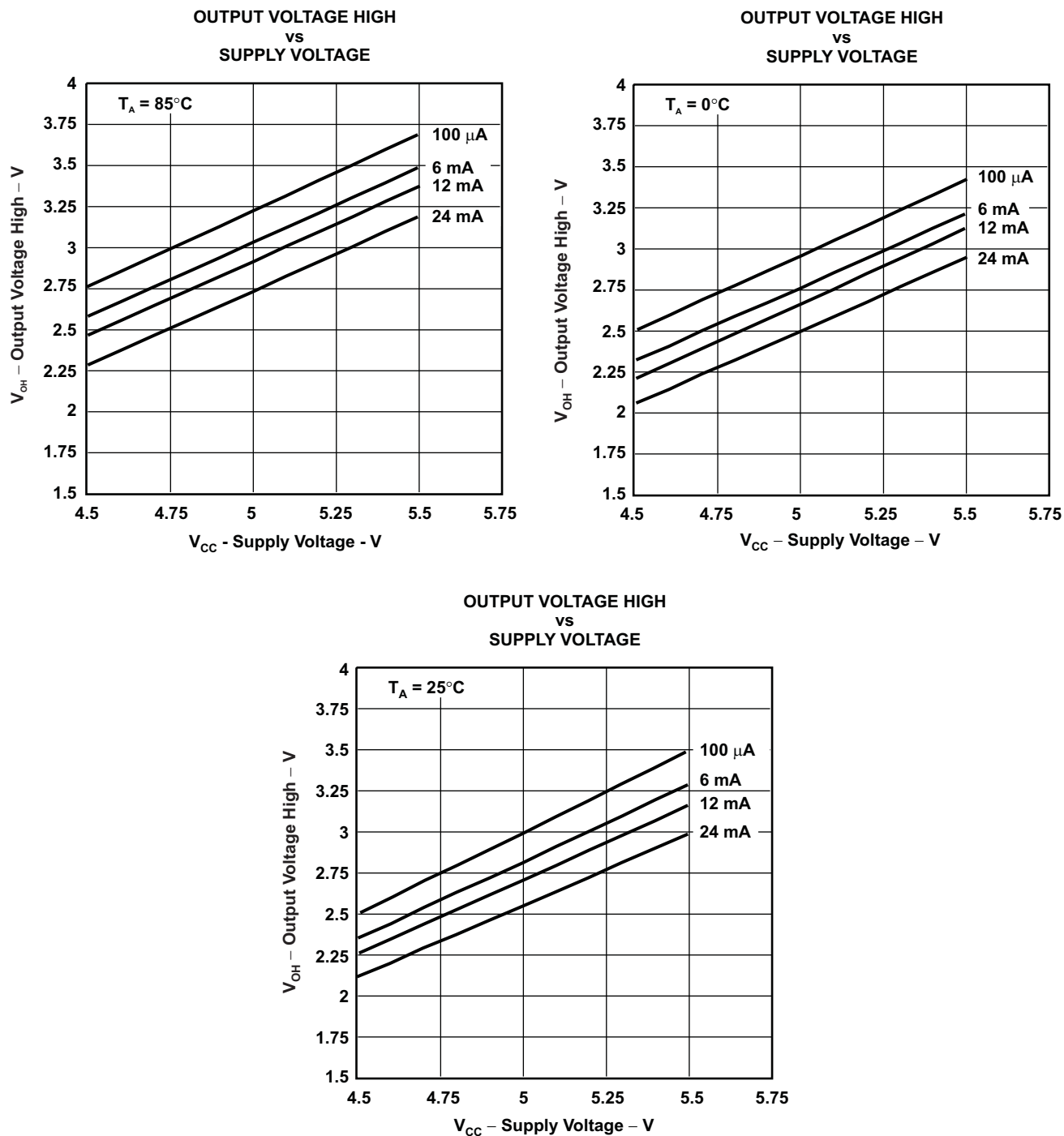


Figure 2. V_{OH} Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTD1G384DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(P8DG, P8DJ, P8DS)	Samples
SN74CBTD1G384DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(P8DJ, P8DS)	Samples
SN74CBTD1G384DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(P8J, P8S)	Samples
SN74CBTD1G384DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(P8J, P8S)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTD1G384DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74CBTD1G384DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74CBTD1G384DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74CBTD1G384DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74CBTD1G384DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74CBTD1G384DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74CBTD1G384DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74CBTD1G384DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74CBTD1G384DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTD1G384DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74CBTD1G384DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74CBTD1G384DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74CBTD1G384DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74CBTD1G384DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74CBTD1G384DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74CBTD1G384DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74CBTD1G384DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74CBTD1G384DCKT	SC70	DCK	5	250	202.0	201.0	28.0

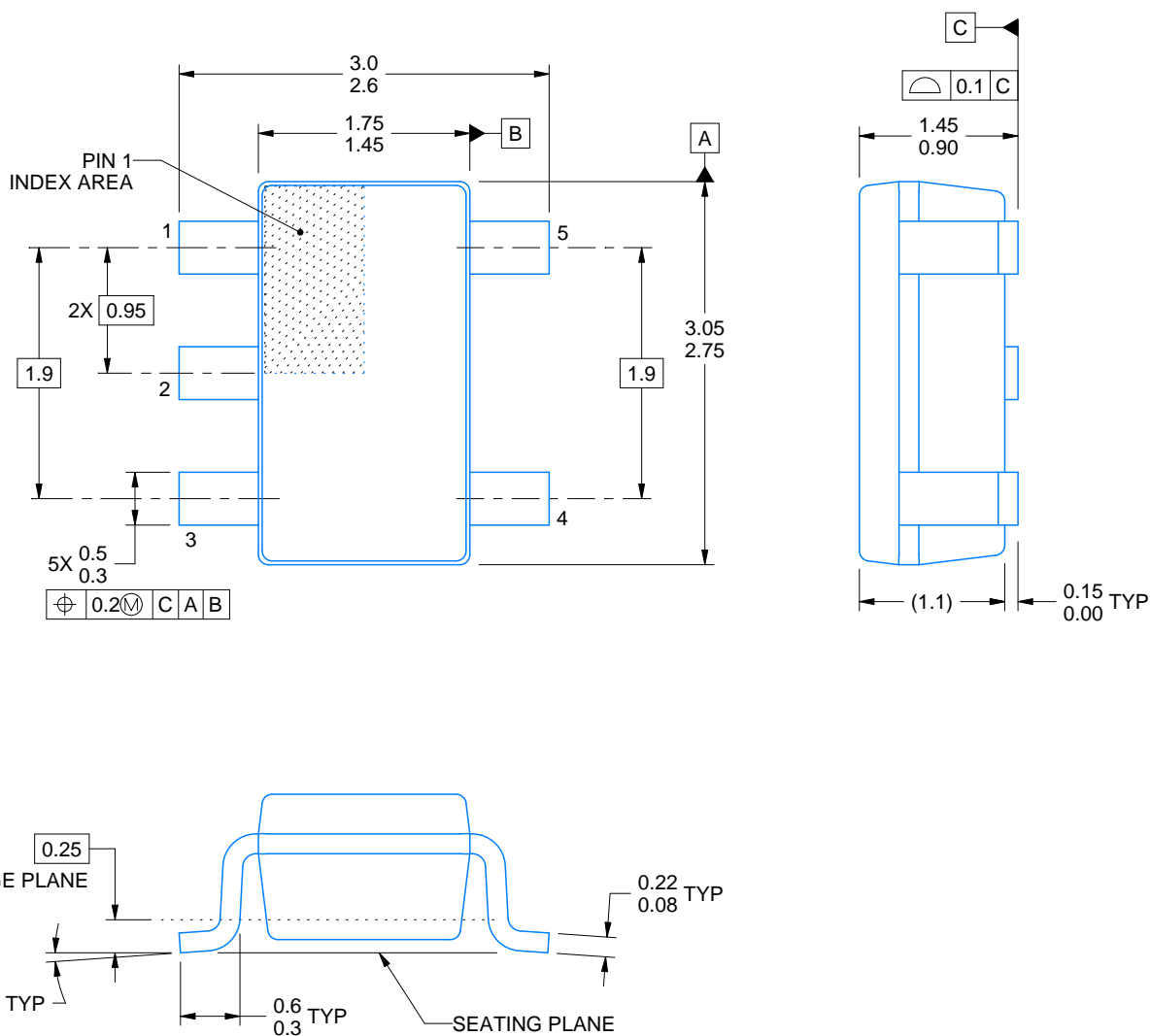


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

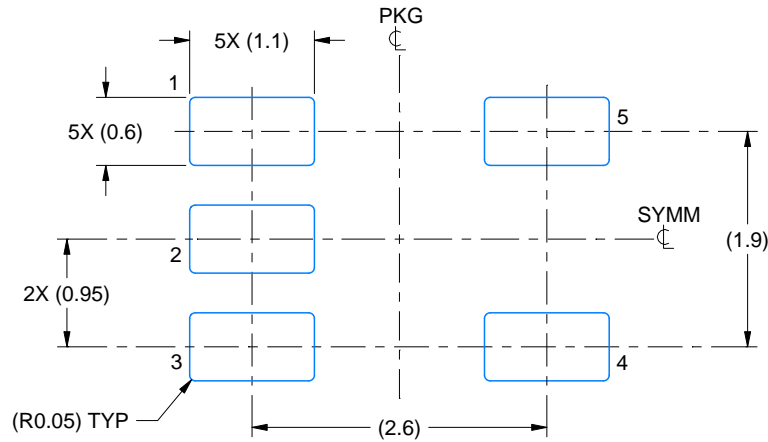
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

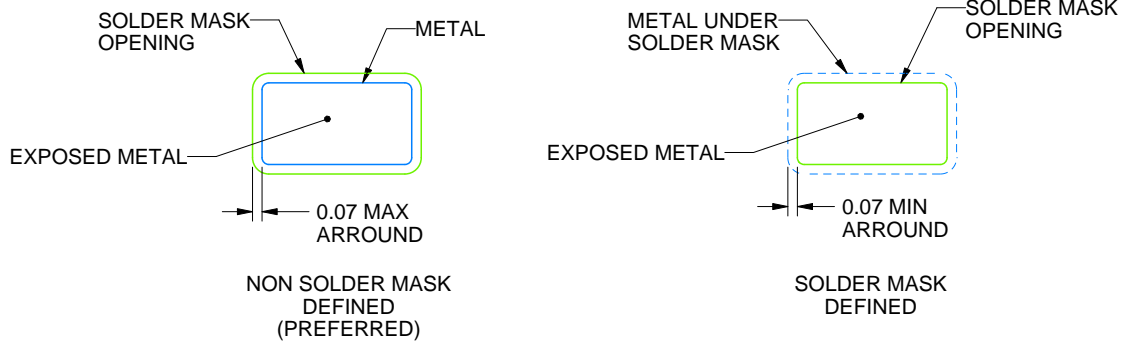
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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