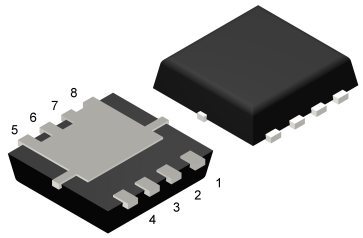
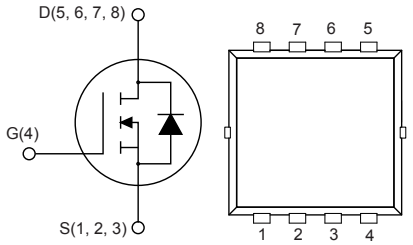
N-channel 100 V, 11.3 mΩ typ., 12 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 3.3x3.3 package



PowerFLAT™ 3.3x3.3



AM15810v1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL12N10F7	100 V	13.3 mΩ	12 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status link
STL12N10F7

Product summary	
Order code	STL12N10F7
Marking	12N10
Package	PowerFLAT™ 3.3x3.3
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
I_D[(1)]	Drain current (continuous) at T_C = 25 °C	44	A
I_D[(1)]	Drain current (continuous) at T_C = 100 °C	28	A
I_{DM}[(1)(2)]	Drain current (pulsed)	176	A
I_D[(3)]	Drain current (continuous) at T_{pcb} = 25 °C	12	A
I_D[(3)]	Drain current (continuous) at T_{pcb} = 100 °C	7	A
I_{DM}[(2)(3)]	Drain current (pulsed)	48	A
P_{TOT}[(1)]	Total dissipation at T_C = 25 °C	52	W
P_{TOT}[(3)]	Total dissipation at T_{pcb} = 25 °C	3	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *This value is rated according to $R_{thj\text{-}c}$.*
2. *Pulse width is limited by safe operating area.*
3. *This value is rated according to $R_{thj\text{-}pcb}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$[(1)]	Thermal resistance junction-pcb max.	42.8	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	2.4	°C/W

1. *When mounted on an FR-4 board of 1 inch², 2oz Cu, t < 10 s.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 100 V			1	µA
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		11.3	13.3	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	1820	-	pF
C_{oss}	Output capacitance		-	400	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 12 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	30	-	nC
Q_{gs}	Gate-source charge		-	11.3	-	nC
Q_{gd}	Gate-drain charge		-	6.4	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	22.4	-	ns
t_r	Rise time		-	8.7	-	ns
$t_{d(off)}$	Turn-off delay time		-	28.6	-	ns
t_f	Fall time		-	8.9	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0 V	-		1.2	V
t_{rr}	Reverse recovery time	I_D = 12 A, di/dt = 100 A/µs, V_{DD} = 80 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	47.5		ns
Q_{rr}	Reverse recovery charge		-	59.4		nC
I_{RRM}	Reverse recovery current		-	2.5		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

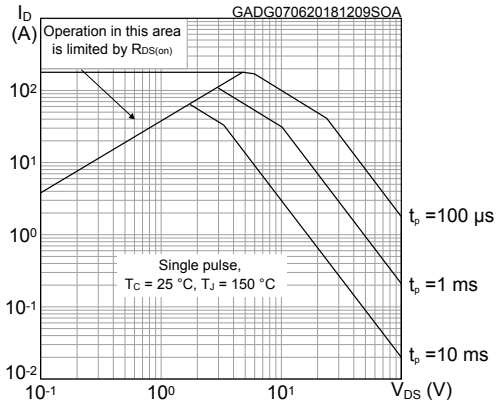


Figure 2. Thermal impedance

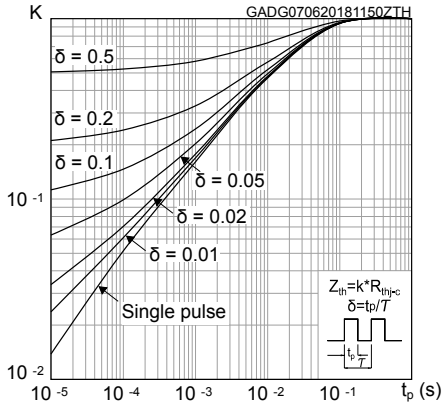


Figure 3. Output characteristics

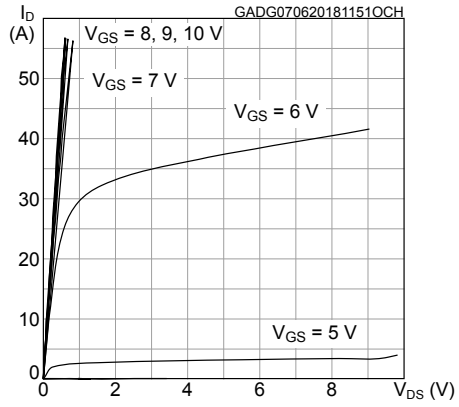


Figure 4. Transfer characteristics

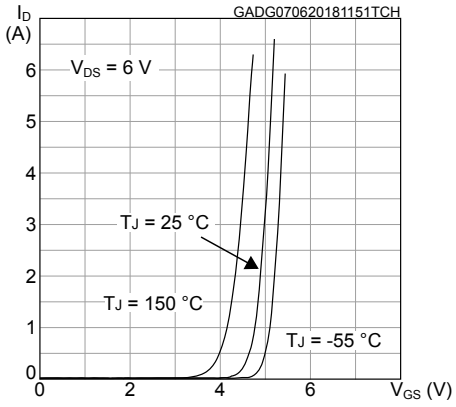


Figure 5. Gate charge vs gate-source voltage

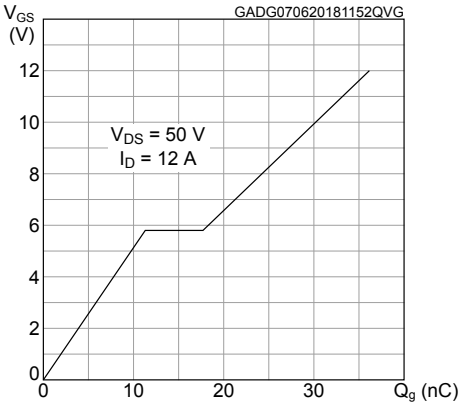


Figure 6. Static drain-source on-resistance

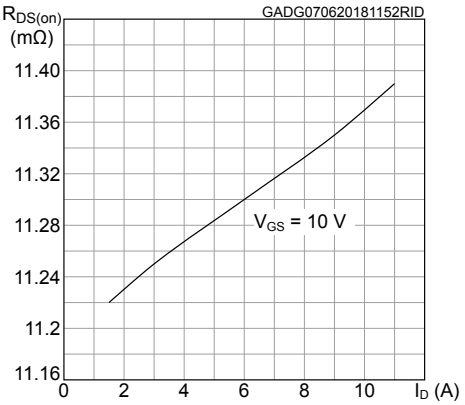


Figure 7. Capacitance variations

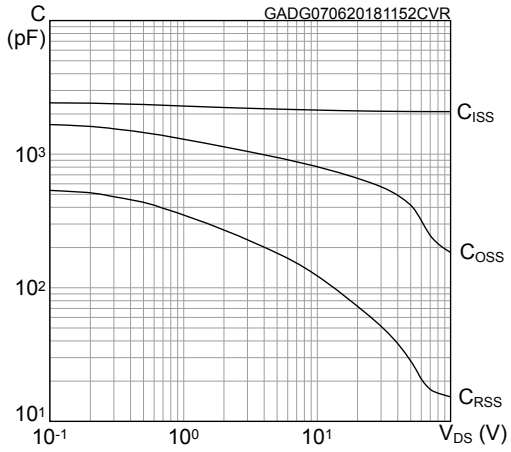


Figure 8. Normalized gate threshold voltage vs temperature

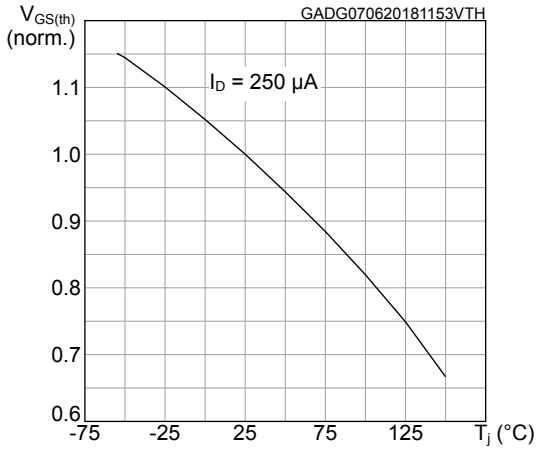


Figure 9. Normalized on-resistance vs temperature

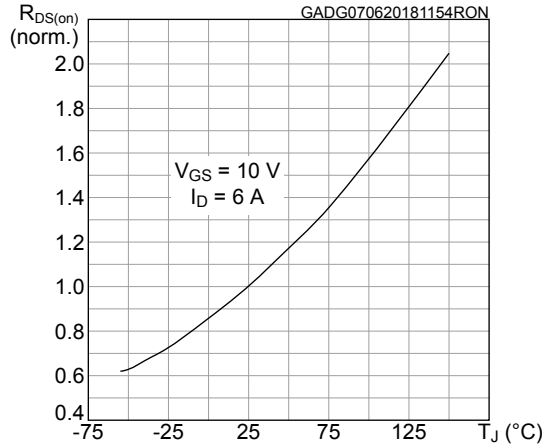


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

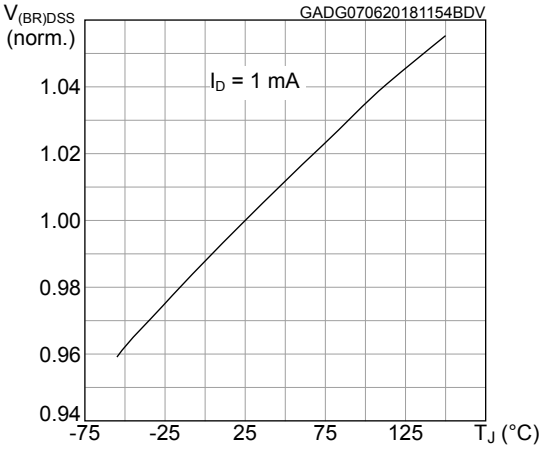
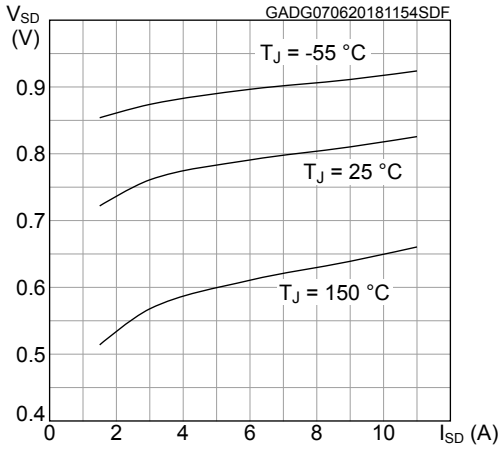


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

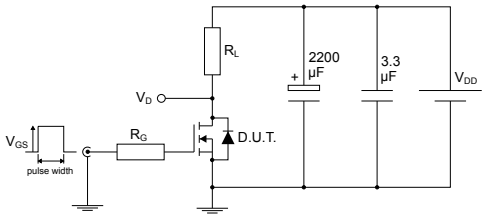


Figure 13. Test circuit for gate charge behavior

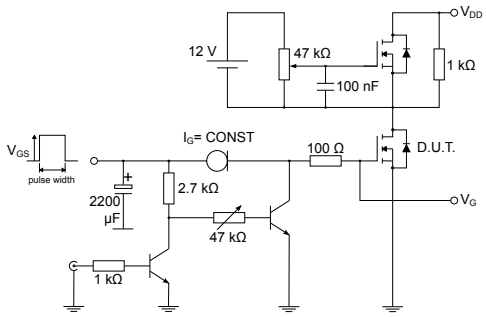


Figure 14. Test circuit for inductive load switching and diode recovery times

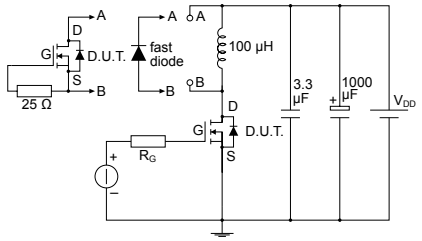


Figure 15. Unclamped inductive load test circuit

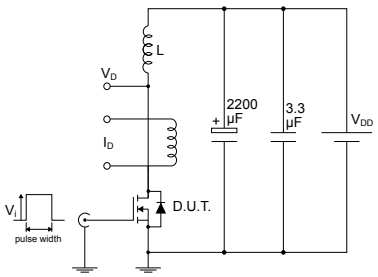


Figure 16. Unclamped inductive waveform

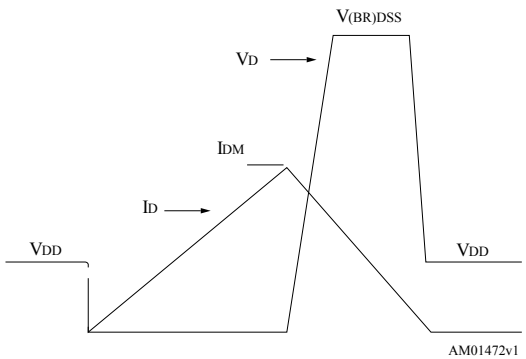
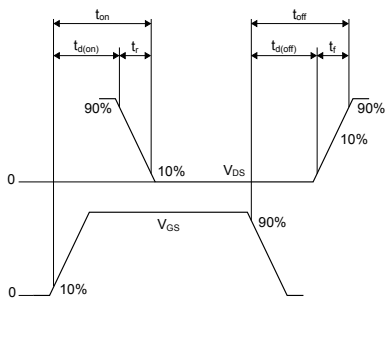


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 3.3x3.3 package information

Figure 18. **PowerFLAT™ 3.3x3.3 package outline**

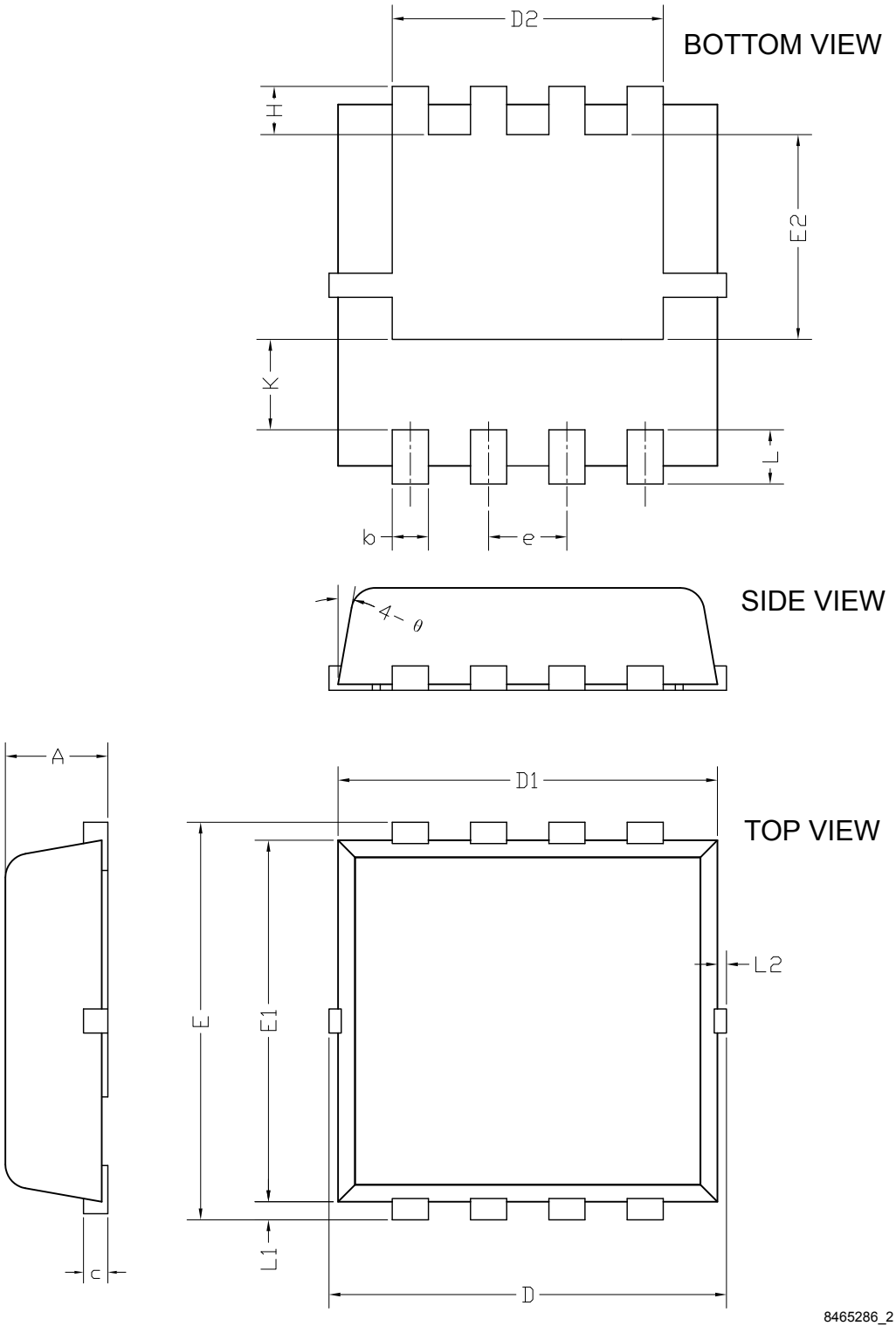
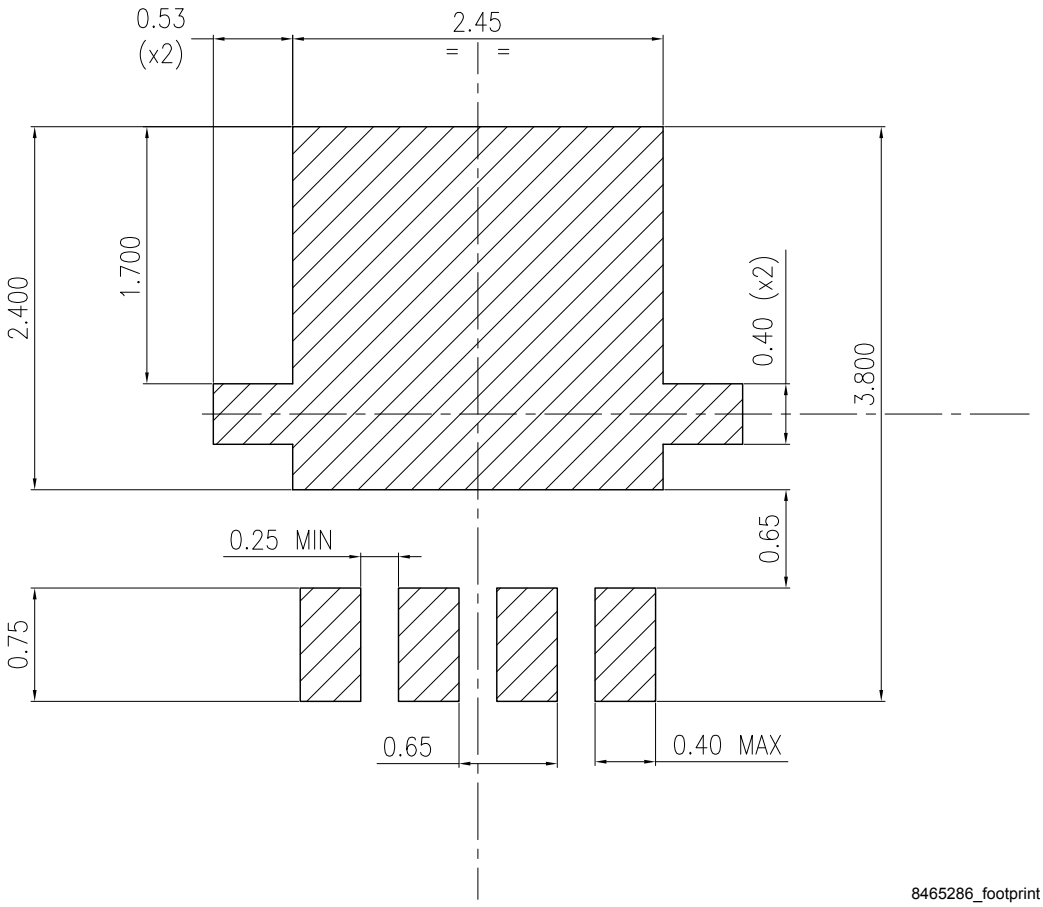


Table 7. **PowerFLAT™ 3.3x3.3 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 19. **PowerFLAT™ 3.3x3.3 recommended footprint (dimensions are in mm)**



Revision history

Table 8. **Document revision history**

Date	Revision	Changes
22-Feb-2017	1	First release
14-Jun-2018	2	Removed maturity status indication from cover page. Updated features on cover page. Updated Section 1 Electrical ratings and Section 2 Electrical characteristics. Added Section 2.1 Electrical characteristics (curves). Minor text changes

Contents