智能电池系统 (SBS) 兼容电量计和保护 已启用具有可选 DQ 接口的 IMPEDANCE TRACK™

查询样品: bq34z950

特性

- 已为下一代产品申请专利 **Impedance Track™** 技术可准确测量锂离子和锂聚合物电池中的可用电量
  - 在电池使用寿命范围内小于 **1%** 的误差
- 支持智能电池技术规范 **SBS V1.1**
- 可选 **DQ** 通信接口
- 针对 **2** 节串联至 **4** 节串联锂离子与锂聚合物电池的灵活配置
- 支持超低功耗模式的强大 **8** 位精简指令集 **(RISC) CPU**
- 可编程保护特性的完全阵列
  - 电压
  - 电流
  - 温度
- 符合 **JEITA** 标准
- 可处理更复杂充电模式的附加灵活性
- 针对电池组情况，驱动 **3**，**4** 和 **5** 段 **LED** 或者 **LCD**
- 支持 **SHA-1** 认证
- 同一封装中的完整电池保护与电量计解决方案
- 采用 **44** 引脚薄型小外形尺寸 **(TSSOP) (DBT)** 封装

应用范围

- 笔记本电脑
- 医疗与测试设备
- 便携式仪表

说明

采用获专利的 Impedance Track™ 技术的 bq34z950 SBS 兼容电量计与保护集成电路 (IC) 是面向电池组或系统内安装的单一 IC 解决方案。 bq34z950 使用其集成型高性能模拟外设，可测量锂离子或锂聚合物电池内的可用电量并保存可用电量的准确记录。 bq34z950 可监控容量变化、电池阻抗、开路电压以及其它电池组关键参数，并通过串行通信总线将信息报告给系统主机控制器。 同时提供系统管理总线 (SMBus) 和单线制 DQ 通信接口。 通过与集成型模拟前端 (AFE) 短路与过负载保护功能结合在一起，bq34z950 在大大降低智能电池电路的外部组件数量、成本、和尺寸的同时，大大提高功能性和安全性。

所执行的 Impedance Track™ 电量计量技术可持续地分析电池阻抗，从而可实现出色的电量计量精度。 这样，通过使用每个周期的每个阶段内精确的放电速率、温度以及电池老化情况，可计算出剩余容量。

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. AVAILABLE OPTIONS

T_A	PACKAGE(1)	
	44-PIN TSSOP (DBT) Tube	44-PIN TSSOP (DBT) Tape and Reel
–40°C to 85°C	bq34z950DBT(2)	bq34z950DBTR(3)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) A single tube quantity is 40 units.
(3) A single reel quantity is 2000 units.

THERMAL INFORMATION

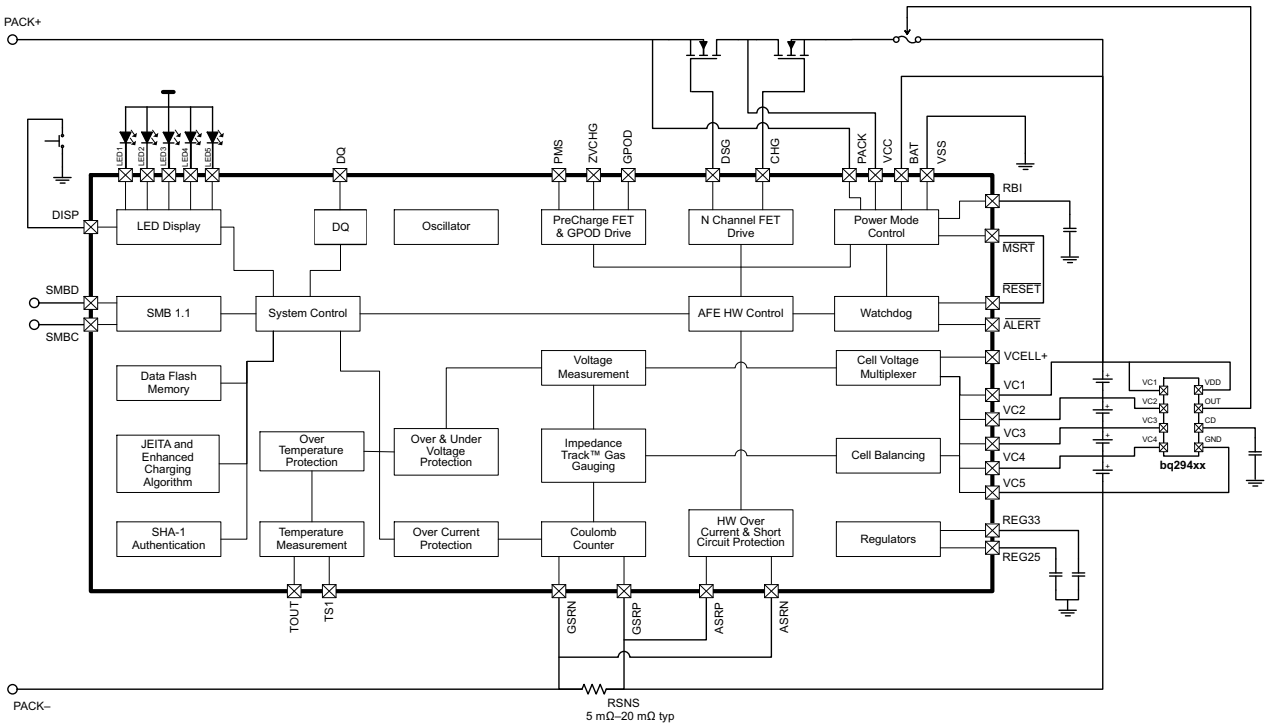
THERMAL METRIC(1)	bq34z950	UNITS
	44-PIN TSSOP (DBT)	
θ_{JA} Junction-to-ambient thermal resistance	47.6	°C/W
$T_A \leq$ 25°C Power Rating	2101	mW
Derating Factor $T_A >$ 25°C	21.01	mW/°C
$T_A \leq$ 70°C Power Rating	1155	mW
$T_A \leq$ 85°C Power Rating	840	mW

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

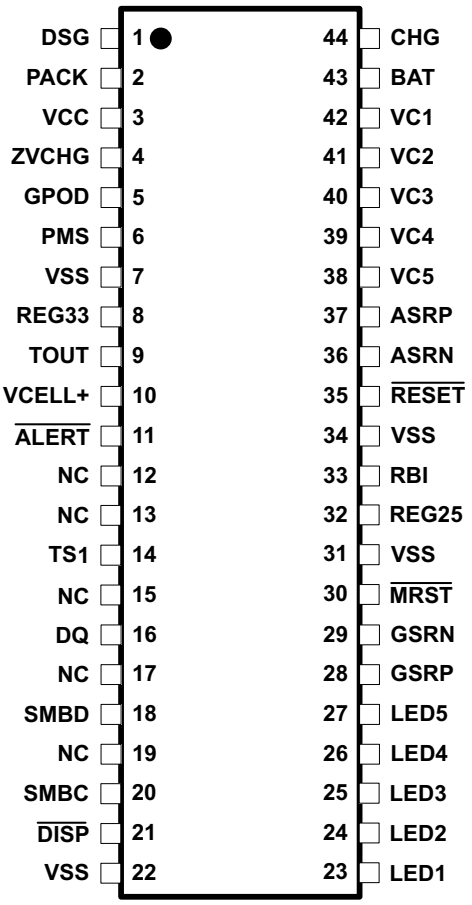
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SYSTEM PARTITIONING DIAGRAM



PACKAGE PINOUT DIAGRAM

bq34z950
DBT PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O(1)	DESCRIPTION
NO.	NAME		
1	DSG	O	High side N-CH discharge FET gate drive
2	PACK	IA, P	Battery pack input voltage sense input. It also serves as device wake up when device is in SHUTDOWN mode.
3	VCC	P	Positive device supply input. Connect to the center connection of the CHG FET and DSG FET to ensure device supply either from battery stack or battery pack input.
4	ZVCHG	O	P-CH pre-charge FET gate drive
5	GPOD	OD	High voltage general purpose open drain output. Can be configured to be used in pre-charge condition.
6	PMS	I	PRE-CHARGE mode setting input. Connect to PACK to enable 0-V precharge using charge FET connected at CHG pin. Connect to VSS to disable 0 V pre-charge using charge FET connected at CHG pin.
7	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
8	REG33	P	3.3-V regulator output. Connect at least a 2.2-µF capacitor to REG33 and VSS.
9	TOUT	P	Thermistor bias supply output
10	VCELL+	—	Internal cell voltage multiplexer and amplifier output. Connect a 0.1-µF capacitor to VCELL+ and VSS.
11	$\overline{\text{ALERT}}$	OD	Alert output. In case of short circuit condition, overload condition and watchdog time out this pin will be triggered.
12	NC	—	Not used—leave floating
13	NC	—	Not used—leave floating
14	TS1	IA	1st Thermistor voltage input connection to monitor temperature
15	NC	—	Not used—leave floating
16	DQ	I/OD	Single-wire bidirectional DQ interface
17	NC	—	Not used—leave floating
18	SMBD	I/OD	SMBus data open-drain bidirectional pin used to transfer address and data to and from the bq34z950
19	NC	—	Not used—leave floating
20	SMBC	I/OD	SMBus clock open-drain bidirectional pin used to clock the data transfer to and from the bq34z950
21	$\overline{\text{DISP}}$	I	Display control for the LEDs. This pin is typically connected to VCC via a 100-kΩ resistor and a push button switch connected to VSS.
22	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
23	LED1	I	LED1 display segment that drives an external LED depending on the firmware configuration
24	LED2	I	LED2 display segment that drives an external LED depending on the firmware configuration
25	LED3	I	LED3 display segment that drives an external LED depending on the firmware configuration
26	LED4	I	LED4 display segment that drives an external LED depending on the firmware configuration
27	LED5	I	LED5 display segment that drives an external LED depending on the firmware configuration
28	GSRP	IA	Coulomb counter differential input. Connect to one side of the sense resistor.
29	GSRN	IA	Coulomb counter differential input. Connect to one side of the sense resistor.
30	$\overline{\text{MRST}}$	I	Master reset input that forces the device into reset when held low. Must be held high for normal operation. Connect to $\overline{\text{RESET}}$ for correct operation of device.
31	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
32	REG25	P	2.5-V regulator output. Connect at least a 1-mF capacitor to REG25 and VSS.
33	RBI	P	RAM/Register backup input. Connect a capacitor to this pin and VSS to protect loss of RAM/Register data in case of short circuit condition.
34	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
35	$\overline{\text{RESET}}$	O	Reset output. Connect to $\overline{\text{MSRT}}$.
36	ASRN	IA	Short circuit and overload detection differential input. Connect to the sense resistor.
37	ASRP	IA	Short circuit and overload detection differential input. Connect to the sense resistor.

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O(1)	DESCRIPTION
NO.	NAME		
38	VC5	IA, P	Cell voltage sense input and cell balancing input for the negative voltage of the bottom cell in the cell stack.
39	VC4	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the bottom cell and the negative voltage of the second lowest cell in the cell stack.
40	VC3	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second lowest cell in the cell stack and the negative voltage of the second highest cell in 4-series cell applications.
41	VC2	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second highest cell and the negative voltage of the highest cell in 4-series cell applications. Connect to VC3 in the 2-series cell stack applications.
42	VC1	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the highest cell in cell stack in 4-series cell applications. Connect to VC2 in 3- or 2-series cell stack applications.
43	BAT	I, P	Battery stack voltage sense input
44	CHG	O	High side N-CH charge FET gate drive

ABSOLUTE MAXIMUM RATINGS

Over-operating free-air temperature (unless otherwise noted) (1)

		PIN	UNIT
V_{SS}	Supply voltage range	BAT, VCC	–0.3 V to 34 V
		PACK, PMS	–0.3 V to 34 V
		VC(n)–VC(n+1); n = 1, 2, 3, 4	–0.3 V to 8.5 V
		VC1, VC2, VC3, VC4	–0.3 V to 34 V
		VC5	–0.3 V to 1 V
V_{IN}	Input voltage range	DQ, SMBD, SMBC. LED1, LED2, LED3, LED4, LED5, $\overline{DISP}$	–0.3 V to 6 V
		TS1, VCELL+, $\overline{ALERT}$	–0.3 V to $V_{(REG25)}$ + 0.3 V
		$\overline{MRST}$, GSRN, GSRP, RBI	–0.3 V to $V_{(REG25)}$ + 0.3 V
		ASRN, ASRP	–1 V to 1 V
V_{OUT}	Output voltage range	DSG, CHG, GPOD	–0.3 V to 34 V
		ZVCHG	–0.3 V to $V_{(BAT)}$
		TOUT, $\overline{ALERT}$, REG33	–0.3 V to 6 V
		$\overline{RESET}$	–0.3 V to 7 V
		REG25	–0.3 V to 2.75 V
I_{SS}	Maximum combined sink current for input pins	DQ, SMBD, SMBC, LED1, LED2, LED3, LED4, LED5	50 mA
T_A	Operating free-air temperature range		–40°C to 85°C
T_F	Functional temperature		–40°C to 100°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over-operating free-air temperature range (unless otherwise noted)

		PIN	MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage	VCC, BAT	4.5		25	V
$V_{(STARTUP)}$	Minimum startup voltage	VCC, BAT, PACK	5.5			V

RECOMMENDED OPERATING CONDITIONS (continued)

Over-operating free-air temperature range (unless otherwise noted)

		PIN	MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	VC(n)–VC(n+1); n = 1,2,3,4	0		5	V
		VC1, VC2, VC3, VC4	0		V_{SS}	V
		VC5	0		0.5	V
		ASRN, ASRP	–0.5		0.5	V
		PACK, PMS	0		25	V
$V_{(GPOD)}$	Output voltage range	GPOD	0		25	V
$I_{(GPOD)}$	Drain current(1)	GPOD			1	mA
$C_{(REG25)}$	2.5-V LDO capacitor	REG25	1			µF
$C_{(REG33)}$	3.3-V LDO capacitor	REG33	2.2			µF
$C_{(VCELL+)}$	Cell voltage output capacitor	VCELL+	0.1			µF
$R_{(PACK)}$	PACK input block resistor(2)	PACK	1			kΩ

(1) Use an external resistor to limit the current to GPOD to 1 mA in high voltage application.
(2) Use an external resistor to limit the in-rush current PACK pin required.

ELECTRICAL CHARACTERISTICS

Over-operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{(NORMAL)}$	Firmware running			550		µA
$I_{(SLEEP)}$	SLEEP mode	CHG FET on; DSG FET on		124		µA
		CHG FET off; DSG FET on		90		µA
		CHG FET off; DSG FET off		52		µA
$I_{(SHUTDOWN)}$	SHUTDOWN mode			0.1	1	µA
SHUTDOWN WAKE; T_A = 25°C (unless otherwise noted)						
$I_{(PACK)}$	Shutdown exit at $V_{STARTUP}$ threshold				1	µA
SRx WAKE FROM SLEEP; T_A = 25°C (unless otherwise noted)						
$V_{(WAKE)}$	Positive or negative wake threshold with 1.00 mV, 2.25 mV, 4.5-mV and 9-mV programmable options		1.25		10	mV
$V_{(WAKE\_ACR)}$	Accuracy of $V_{(WAKE)}$	$V_{(WAKE)}$ = 1 mV; $I_{(WAKE)}$= 0, RSNS1 = 0, RSNS0 = 1	–0.7		0.7	mV
		$V_{(WAKE)}$ = 2.25 mV; $I_{(WAKE)}$) = 1, RSNS1 = 0, RSNS0 = 1; $I_{(WAKE)}$ = 0, RSNS1 = 1, RSNS0 = 0	–0.8		0.8	
		$V_{(WAKE)}$ = 4.5 mV; $I_{(WAKE)}$ = 1, RSNS1 = 1, RSNS0 = 1; $I_{(WAKE)}$ = 0, RSNS1 = 1, RSNS0 = 0	–1.0		1.0	
		$V_{(WAKE)}$ = 9 mV; $I_{(WAKE)}$ = 1, RSNS1 = 1, RSNS0 = 1	–1.4		1.4	
$V_{(WAKE\_TCO)}$	Temperature drift of $V_{(WAKE)}$ accuracy			0.5		%/°C
$t_{(WAKE)}$	Time from application of current and wake of bq34z950			1	10	ms
WATCHDOG TIMER						
t_{WDTINT}	Watchdog start up detect time		250	500	1000	ms
t_{WDWT}	Watchdog detect time		50	100	150	µs
2.5-V LDO; $I_{(REG33OUT)}$ = 0 mA; T_A = 25°C (unless otherwise noted)						
$V_{(REG25)}$	Regulator output voltage	4.5 < VCC or BAT < 25 V; $I_{(REG25OUT)}$) ≤ 16 mA; T_A = –40°C to 100°C	2.41	2.5	2.59	V

ELECTRICAL CHARACTERISTICS (continued)

Over-operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{(REG25TEMP)}$	Regulator output change with temperature	$I_{(REG25OUT)}$ = 2 mA; T_A = –40°C to 100°C		±0.2		%
$\Delta V_{(REG25LINE)}$	Line regulation	5.4 < VCC or BAT < 25 V; $I_{(REG25OUT)}$ = 2 mA		3	10	mV
$\Delta V_{(REG25LOAD)}$	Load regulation	0.2 mA ≤ $I_{(REG25OUT)}$ ≤ 2 mA		7	25	mV
		0.2 mA ≤ $I_{(REG25OUT)}$ ≤ 16 mA		25	50	
$I_{(REG25MAX)}$	Current limit	Drawing current until REG25 = 2 V to 0 V	5	40	75	mA
3.3-V LDO; $I_{(REG25OUT)}$ = 0 mA; T_A = 25°C (unless otherwise noted)						
$V_{(REG33)}$	Regulator output voltage	4.5 < VCC or BAT < 25 V; $I_{(REG33OUT)}$ ≤ 25 mA; T_A = –40°C to 100°C	3	3.3	3.6	V
$\Delta V_{(REG33TEMP)}$	Regulator output change with temperature	$I_{(REG33OUT)}$ = 2 mA; T_A = –40°C to 100°C		±0.2		%
$\Delta V_{(REG33LINE)}$	Line regulation	5.4 < VCC or BAT < 25 V; $I_{(REG33OUT)}$ = 2 mA		3	10	mV
$\Delta V_{(REG33LOAD)}$	Load regulation	0.2 mA ≤ $I_{(REG33OUT)}$ ≤ 2 mA		7	17	mV
		0.2 mA ≤ $I_{(REG33OUT)}$ ≤ 25 mA		40	100	
$I_{(REG33MAX)}$	Current limit	drawing current until REG33 = 3 V	25	100	145	mA
		short REG33 to VSS, REG33 = 0 V	12		65	
THERMISTOR DRIVE						
$V_{(TOUT)}$	Output voltage	$I_{(TOUT)}$ = 0 mA; T_A = 25°C		$V_{(REG25)}$		V
$R_{DS(on)}$	TOUT pass element resistance	$I_{(TOUT)}$ = 1 mA; $R_{DS(on)}$ = ($V_{(REG25)}$ – $V_{(TOUT)}$)/ 1 mA; T_A = –40°C to 100°C		50	100	Ω
LED OUTPUTS						
V_{OL}	Output low voltage	LED1, LED2, LED3, LED4, LED5			0.4	V
VCELL+ HIGH VOLTAGE TRANSLATION						
$V_{(VCELL+OUT)}$	Translation output	VC(n) – VC(n+1) = 0 V; T_A = –40°C to 100°C	0.950	0.975	1	V
		VC(n) – VC(n+1) = 4.5 V; T_A = –40°C to 100°C	0.275	0.3	0.375	
$V_{(VCELL+REF)}$		Internal AFE reference voltage; T_A = –40°C to 100°C	0.965	0.975	0.985	
$V_{(VCELL+PACK)}$		Voltage at PACK pin; T_A = –40°C to 100°C	0.98 × $V_{(PACK)}$/18	$V_{(PACK)}$/18	1.02 × $V_{(PACK)}$/18	
$V_{(VCELL+BAT)}$		Voltage at BAT pin; T_A = –40°C to 100°C	0.98 × $V_{(BAT)}$/18	$V_{(BAT)}$/18	1.02 × $V_{(BAT)}$/18	
CMMR	COMMON mode rejection ratio	VCELL+	40			dB
K	Cell scale factor	K= {VCELL+ output (VC5=0 V; VC4=4.5 V) – VCELL+ output (VC5=0 V; VC4=0 V)}/4.5	0.147	0.150	0.153	
		K= {VCELL+ output (VC2=13.5 V; VC1=18 V) – VCELL+ output (VC5=13.5 V; VC1=13.5 V)}/4.5	0.147	0.150	0.153	
$I_{(VCELL+OUT)}$	Drive Current to VCELL+ capacitor	VC(n) – VC(n+1) = 0 V; VCELL+ = 0 V; T_A = –40°C to 100°C	12	18		µA
$V_{(VCELL+O)}$	CELL offset error	CELL output (VC2 = VC1 = 18 V) – CELL output (VC2 = VC1 = 0 V)	–18	–1	18	mV
I_{VCnL}	VC(n) pin leakage current	VC1, VC2, VC3, VC4, VC5 = 3 V	–1	0.01	1	µA
CELL BALANCING						
R_{BAL}	internal cell balancing FET resistance	$R_{DS(on)}$ for internal FET switch at V_{DS} = 2 V; T_A = 25°C	200	400	600	Ω
HARDWARE SHORT CIRCUIT AND OVERLOAD PROTECTION; T_A = 25°C (unless otherwise noted)						
$V_{(OL)}$	OL detection threshold voltage accuracy	V_{OL} = 25 mV (min)	15	25	35	mV
		V_{OL} = 100 mV; RSNS = 0, 1	90	100	110	
		V_{OL} = 205 mV (max)	185	205	225	

ELECTRICAL CHARACTERISTICS (continued)

Over-operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(SCC)}$	SCC detection threshold voltage accuracy	$V_{(SCC)}$ = 50 mV (min)		30	50	70	mV
		$V_{(SCC)}$ = 200 mV; RSNS = 0, 1		180	200	220	
		$V_{(SCC)}$ = 475 mV (max)		428	475	523	
$V_{(SCD)}$	SCD detection threshold voltage accuracy	$V_{(SCD)}$ = –50 mV (min)		–30	–50	–70	mV
		$V_{(SCD)}$ = –200 mV; RSNS = 0, 1		–180	–200	–220	
		$V_{(SCD)}$ = –475 mV (max)		–428	–475	–523	
t_{da}	Delay time accuracy				±15.25		µs
t_{pd}	Protection circuit propagation delay				50		µs
FET DRIVE CIRCUIT; T_A = 25°C (unless otherwise noted)							
$V_{(DSGON)}$	DSG pin output on voltage	$V_{(DSGON)} = V_{(DSG)} – V_{(PACK)}$; $V_{(GS)}$ connected to 10 MΩ; DSG and CHG on; T_A = –40°C to 100°C		8	12	16	V
$V_{(CHGON)}$	CHG pin output on voltage	$V_{(CHGON)} = V_{(CHG)} – V_{(BAT)}$; $V_{(GS)}$ = 10 MΩ; DSG and CHG on; T_A = –40°C to 100°C		8	12	16	V
$V_{(DSGOFF)}$	DSG pin output off voltage	$V_{(DSGOFF)} = V_{(DSG)} – V_{(PACK)}$				0.2	V
$V_{(CHGOFF)}$	CHG pin output off voltage	$V_{(CHGOFF)} = V_{(CHG)} – V_{(BAT)}$				0.2	V
t_r	Rise time	C_L= 4700 pF	$V_{(CHG)}$: $V_{(PACK)} \geq V_{(PACK)}$ + 4 V		400	1000	µs
			$V_{(DSG)}$: $V_{(BAT)} \geq V_{(BAT)}$ + 4V		400	1000	
t_f	Fall time	C_L= 4700pF	$V_{(CHG)}$: $V_{(PACK)} + V_{(CHGON)} \geq V_{(PACK)}$+ 1 V		40	200	µs
			$V_{(DSG)}$: VC1 + $V_{(DSGON)} \geq$ VC1 + 1 V		40	200	
$V_{(ZVCHG)}$	ZVCHG clamp voltage	BAT = 4.5 V		3.3	3.5	3.7	V
LOGIC; T_A = –40°C to 100°C (unless otherwise noted)							
$R_{(PULLUP)}$	Internal pullup resistance	$\overline{ALERT}$		60	100	200	kΩ
		$\overline{RESET}$		1	3	6	
V_{OL}	Logic low output voltage level	$\overline{ALERT}$				0.2	V
		$\overline{RESET}$; $V_{(BAT)}$ = 7 V; $V_{(REG25)}$ = 1.5 V; $I_{(\overline{RESET})}$ = 200 µA				0.4	
		GPOD; $I_{(GPOD)}$ = 50 µA				0.6	
LOGIC SMBC, SMBD, DQ, $\overline{ALERT}$, $\overline{DISP}$							
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	Output voltage high(1)	I_L = –0.5 mA		V_{REG25}–0.5			V
V_{OL}	Low-level output voltage	DQ, $\overline{ALERT}$, $\overline{DISP}$; I_L = 7 mA;				0.4	V
C_I	Input capacitance				5		pF
I_{lkg}	Input leakage current					1	µA
ADC(2)							
	Input voltage range	TS1, using Internal V_{ref}		–0.2		1	V
	Conversion time				31.5		ms
	Resolution (no missing codes)			16			bits
	Effective resolution			14	15		bits
	Integral nonlinearity					±0.03	%FSR(3)
	Offset error(4)				140	250	µV
	Offset error drift(4)	T_A = 25°C to 85°C			2.5	18	µV/°C
	Full-scale error(5)				±0.1%	±0.7%	
	Full-scale error drift				50		PPM/°C

(1) RC[0:7] bus
(2) Unless otherwise specified, the specification limits are valid at all measurement speed modes.
(3) Full-scale reference
(4) Post-calibration performance and no I/O changes during conversion with SRN as the ground reference.
(5) Uncalibrated performance. This gain error can be eliminated with external calibration.

ELECTRICAL CHARACTERISTICS (continued)

Over-operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

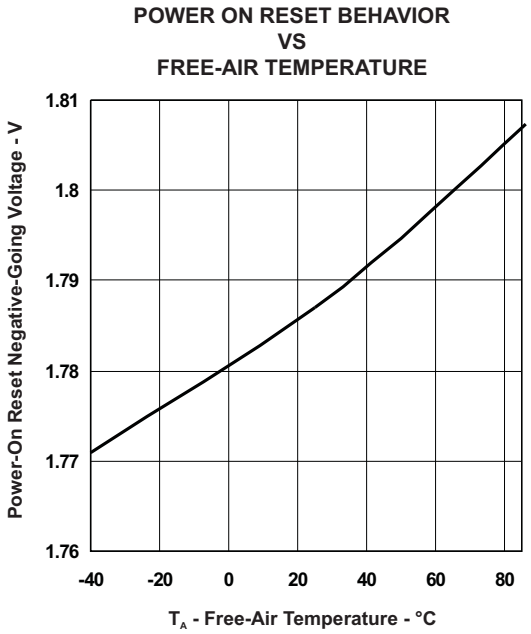
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Effective input resistance(6)		8			MΩ
COULOMB COUNTER						
	Input voltage range		–0.20		0.20	V
	Conversion time	Single conversion		250		ms
	Effective resolution	Single conversion	15			bits
	Integral nonlinearity	–0.1 V to 0.20 V		±0.007	±0.034	%FSR
		–0.20 V to –0.1 V		±0.007		
	Offset error (7)	T_A = 25°C to 85°C		10		µV
	Offset error drift			0.4	0.7	µV/°C
	Full-scale error(8) (9)			±0.35%		
	Full-scale error drift			150		PPM/°C
	Effective input resistance(10)	T_A = 25°C to 85°C	2.5			MΩ
INTERNAL TEMPERATURE SENSOR						
$V_{(TEMP)}$	Temperature sensor voltage(11)			–2.0		mV/°C
VOLTAGE REFERENCE						
	Output voltage		1.215	1.225	1.230	V
	Output voltage drift			65		PPM/°C
HIGH FREQUENCY OSCILLATOR						
$f_{(OSC)}$	Operating frequency			4.194		MHz
$f_{(EIO)}$	Frequency error (12) (13)		–3%	0.25%	3%	
		T_A = 20°C to 70°C	–2%	0.25%	2%	
$t_{(SXO)}$	Start-up time(14)			2.5	5	ms
LOW FREQUENCY OSCILLATOR						
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(13) (15)		–2.5%	0.25%	2.5%	
		T_A = 20°C to 70°C	–1.5%	0.25%	1.5%	
$t_{(LSXO)}$	Start-up time(14)				500	µs

(6) The A/D input is a switched-capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.
(7) Post-calibration performance
(8) Reference voltage for the coulomb counter is typically V_{ref}/3.969 at $V_{(REG25)}$ = 2.5 V, T_A = 25°C.
(9) Uncalibrated performance. This gain error can be eliminated with external calibration.
(10) The CC input is a switched capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.
(11) –53.7 LSB/°C
(12) The frequency error is measured from 4.194 MHz.
(13) The frequency drift is included and measured from the trimmed frequency at $V_{(REG25)}$ = 2.5 V, T_A = 25°C.
(14) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.
(15) The frequency error is measured from 32.768 kHz.

POWER-ON RESET

Over-operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIT–	Negative-going voltage input		1.7	1.8	1.9	V
VHYS	Power-on reset hysteresis		5	125	200	mV
t_{RST}	$\overline{RESET}$ active low time	Active low time after power up or watchdog reset	100	250	560	µs



DATA FLASH CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Typical values at T_A = 25°C and $V_{(REG25)}$ = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention	See (1)	10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				200	ms
$t_{(PAGEERASE)}$	Page-erase time				20	ms
$I_{(DDPROG)}$	Flash-write supply current			5	10	mA
$I_{(DDERASE)}$	Flash-erase supply current			5	10	mA
RAM/REGISTER BACKUP						
$I_{(RB)}$	RB data-retention input current	$V_{(RBI)} > V_{(RBI)MIN}$, $V_{REG25} < V_{IT-}$, T_A = 85°C		1000	2500	nA
		$V_{(RBI)} > V_{(RBI)MIN}$, $V_{REG25} < V_{IT-}$, T_A = 25°C		90	220	
$V_{(RB)}$	RB data-retention input voltage (1)		1.7			V

(1) Specified by design. Not production tested.

SMBus TIMING CHARACTERISTICS

T_A = –40°C to 85°C Typical Values at T_A = 25°C and V_{REG25} = 2.5 V (Unless Otherwise Noted)

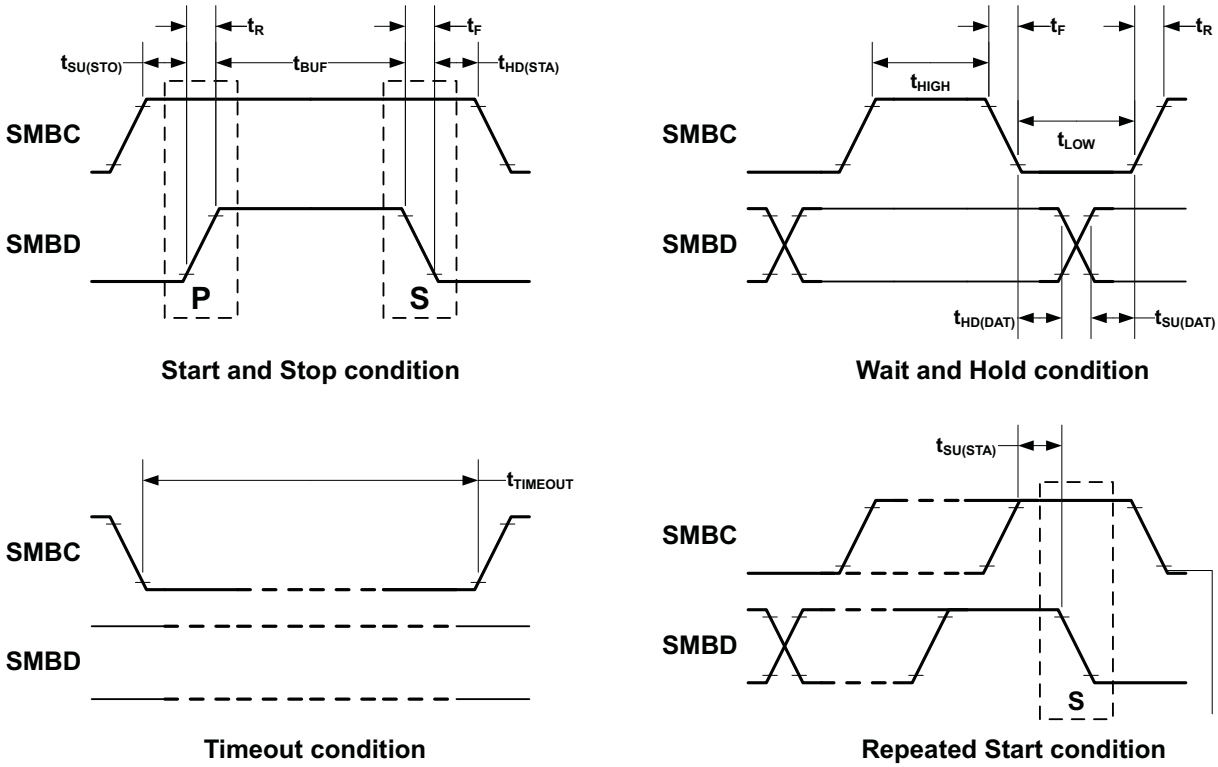
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SMB)}$	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
$f_{(MAS)}$	SMBus master clock frequency	MASTER mode, No clock low slave extend		51.2		kHz
$t_{(BUF)}$	Bus free time between start and stop (see Figure 1)		4.7			µs
$t_{(HD:STA)}$	Hold time after (repeated) start (see Figure 1)		4			µs
$t_{(SU:STA)}$	Repeated start setup time (see Figure 1)		4.7			µs
$t_{(SU:STO)}$	Stop setup time (see Figure 1)		4			µs
$t_{(HD:DAT)}$	Data hold time (see Figure 1)	RECEIVE mode	0			ns
		TRANSMIT mode	300			

SMBus TIMING CHARACTERISTICS (continued)

T_A = –40°C to 85°C Typical Values at T_A = 25°C and V_{REG25} = 2.5 V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(SU:DAT)}$	Data setup time (see Figure 1)		250			ns
$t_{(TIMEOUT)}$	Error signal/detect (see Figure 1)	See (1)	25		35	µs
$t_{(LOW)}$	Clock low period (see Figure 1)		4.7			µs
$t_{(HIGH)}$	Clock high period (see Figure 1)	See (2)	4		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{(LOW:MEXT)}$	Cumulative clock low master extend time (see Figure 1)	See (4)			10	ms
t_f	Clock/data fall time	See (5)			300	ns
t_r	Clock/data rise time	See (6)			1000	ns

(1) The bq34z950 times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction involving bq34z950 that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{(LOW:MEXT)}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time t_r = VILMAX – 0.15) to (VIHMIN + 0.15)
(6) Fall time t_f = 0.9V_{DD} to (VILMAX – 0.15)



A. SCLKACK is the acknowledge-related clock pulse generated by the master.

Figure 1. SMBus Timing Diagram

DQ 1-WIRE INTERFACE

DQ TIMING SPECIFICATIONS

V_{DD} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CYCH)}$	Cycle time, host to bq34z950	See (1)	3			ms
$t_{(CYCB)}$	Cycle time, bq34z950 to host		3		6	ms
$t_{(STRH)}$	Start hold, host to bq34z950		5			ns
$t_{(STRB)}$	Start hold, bq34z950 to host		500		750	µs
$t_{(DSU)}$	Data setup					µs
$t_{(DH)}$	Data hold		750			µs
$t_{(DV)}$	Data valid		1.5			ms
$t_{(SSU)}$	Stop setup				2.25	ms
$t_{(SH)}$	Stop hold		700			µs
$t_{(SV)}$	Stop valid		2.95			ms
$t_{(B)}$	Break		3			ms
$t_{(BR)}$	Break recovery		1			ms

(1) The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

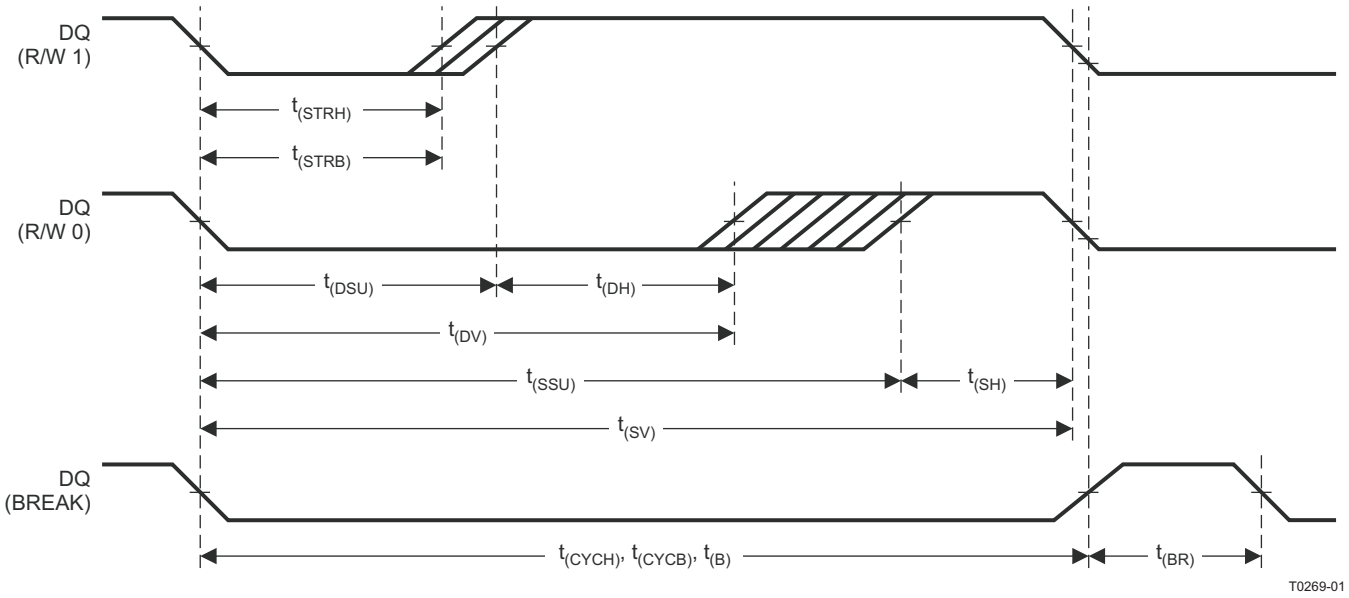
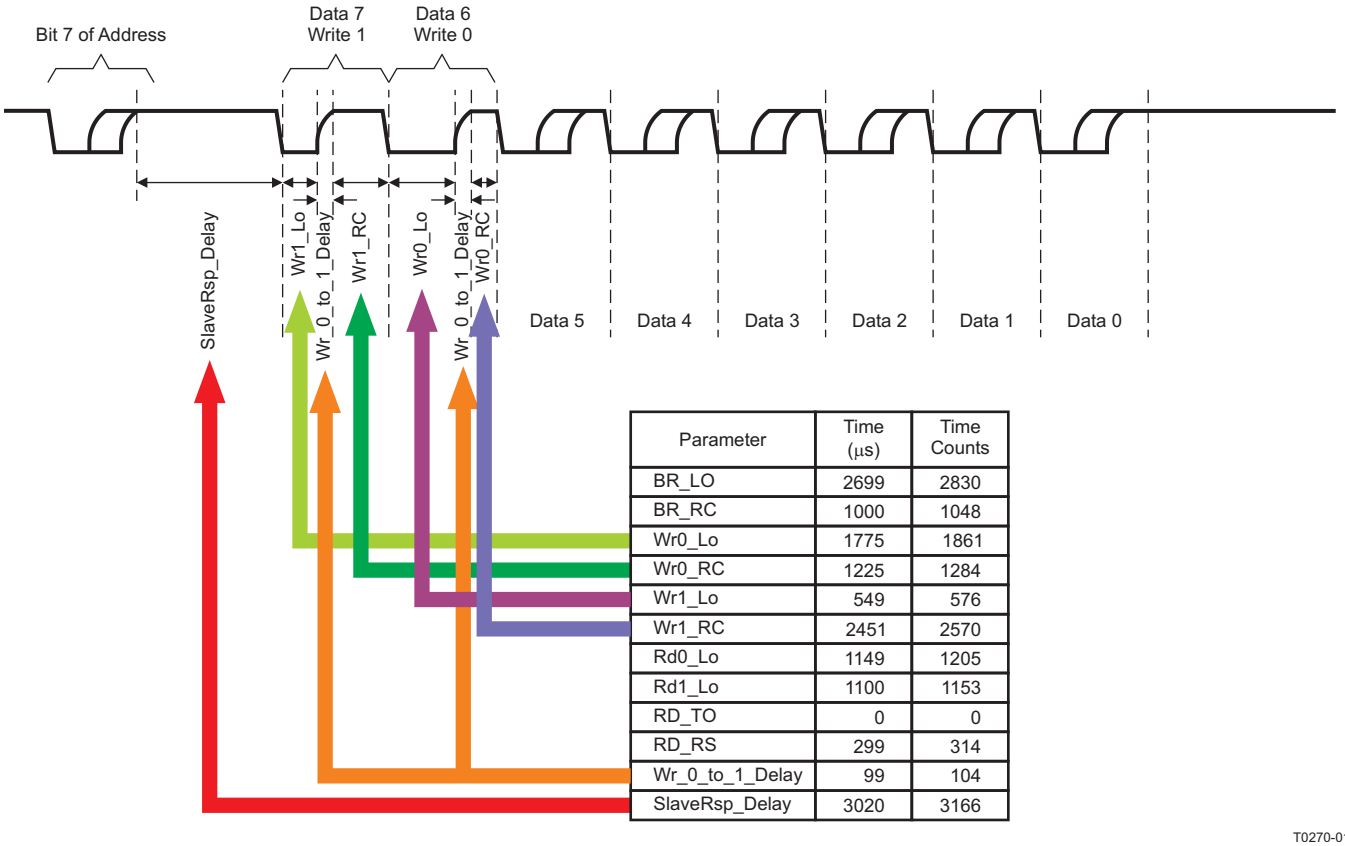


Figure 2. DQ Timing Diagram

DQ timing for this device is selectable by adjusting values in Data Flash Sub Class 0x113. See Figure 3 for an overview of the flash values.



Parameter	Time (µs)	Time Counts
BR_LO	2699	2830
BR_RC	1000	1048
Wr0_Lo	1775	1861
Wr0_RC	1225	1284
Wr1_Lo	549	576
Wr1_RC	2451	2570
Rd0_Lo	1149	1205
Rd1_Lo	1100	1153
RD_TO	0	0
RD_RS	299	314
Wr_0_to_1_Delay	99	104
SlaveRsp_Delay	3020	3166

T0270-01

Figure 3. DQ Timing Control

FEATURE SET

Primary (First-Level) Safety Features

The bq34z950 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short circuit
- Charge and discharge overtemperature
- AFE watchdog

Secondary (Second-Level) Safety Features

The secondary safety features of the bq34z950 can be used to indicate more serious faults. The secondary safety protection features include:

- Safety overvoltage
- Safety overcurrent in charge and discharge
- Safety overtemperature in Charge and Discharge
- Charge FET and 0-V charge FET fault
- Discharge FET fault
- AFE communication fault

Charge Control Features

The bq34z950 charge control features include:

- Reports the appropriate charging current needed for constant current charging, and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts.
- Determines the chemical state of charge of each battery cell using Impedance Track technology, and can reduce the charge difference of the battery cells in a fully charged state of the battery pack, gradually using the cell balancing algorithm during charging. This prevents fully charged cells from overcharging and causing excessive degradation, and also increases the usable pack energy by preventing premature charge termination.
- Supports precharging/zero-volt charging
- Supports fast charging
- Supports charge inhibit and charge suspend if the battery pack temperature is out of temperature range
- Reports charging fault and also indicates charge status via charge and discharge alarms

Gas Gauging

The bq34z950 uses Impedance Track technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than 1% error over the lifetime of the battery, and there is no full charge discharge learning cycle required.

See the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application note (SLUA364) for further details.

Authentication

The bq34z950 supports authentication by the host using SHA-1.

Power Modes

The bq34z950 supports three power modes to reduce power consumption:

- In NORMAL mode, the bq34z950 performs measurements, calculations, protection decisions, and data updates in 1-s intervals. Between these intervals, the bq34z950 is in a reduced power state.

- In SLEEP mode, the bq34z950 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq34z950 is in a reduced power state. The bq34z950 has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the bq34z950 is completely disabled.

CONFIGURATION

Oscillator Function

The bq34z950 fully integrates the system oscillators. Therefore, the bq34z950 requires no external components for this feature.

BATTERY PARAMETER MEASUREMENTS

The bq34z950 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN pins. The integrating ADC measures bipolar signals from –0.25 V to 0.25 V. The bq34z950 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The bq34z950 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nV/h.

Voltage

The bq34z950 updates the individual series cell voltages at 1-s intervals. The internal ADC of the bq34z950 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track gas gauging.

Current

The bq34z950 uses the GSRP and GSRN inputs to measure and calculate the battery charge and discharge current using a 5-mΩ to 20-mΩ typical sense resistor.

Auto Calibration

The bq34z950 provides an autocalibration feature to cancel the voltage offset error across SRP and SRN for maximum charge measurement accuracy. The bq34z950 performs autocalibration when the SMBus and DQ lines stay low for a minimum of 16 s, and the DF:AutoCal_PerSleep counter has counted up to its programmed value. The AutoCal_PerSleep counter provides a way for the user to specify the number of times the part can enter SLEEP mode before an offset calibration is performed. This is to prohibit unnecessary calibration cycles for battery packs that enter SLEEP mode frequently. The bq34z950 is capable of automatic offset calibration down to 1 µV.

Temperature

The bq34z950 has an internal temperature sensor and external temperature sensor input, TS1, which can be used to sense the environmental temperature of the batteries. The bq34z950 can be configured to use internal or external temperature sensors. The external sensor input is used in conjunction with an NTC thermistor (default is Semitec 103AT).

COMMUNICATIONS

The bq34z950 uses SMBus v1.1 with MASTER mode and package error checking (PEC) options per the SBS specification. Integrated error checking is not available on the DQ interface.

SMBus/DQ On and Off States

The bq34z950 detects an SMBus/DQ off state when SMBC, SMBD, and DQ are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD or DQ to transition high. Within 1 ms, the communication bus is available.

SHA-1 Over DQ

SHA-1 Overview

The host sends a randomly generated 20-byte challenge, and then reads the 20-byte response generated by the bq34z950. The response generated by the bq34z950 is calculated using the SHA-1 hash algorithm and a shared private key known by both parties to the transaction. The host compares the bq34z950 response to the expected response, and if they agree, then the host concludes that the bq34z950 knows the key, and is thus authenticated.

The 20-byte challenge/response is written/read using registers 0x1B–0x2E. The bq34z950 calculates the response when a write of any data value is issued to register 0x2F. DQ communication is ignored when the response is calculated, which takes approximately 22 ms.

SHA-1 Usage Procedure

Use the following two steps to implement the SHA-1 algorithm in the bq34z950:

1. Create a unique authentication key and write it to the part during assembly.

   The authentication key resides in the SMBus addresses 0x63–0x66 in 4-byte strings. The four strings are read/write accessible until the bq34z950 is sealed. When written using an SMBus string write command, they are retained permanently in flash memory and can only be changed when the bq34z950 is unsealed. They are stored in Little Endian format. The SHA-1 authentication key defaults to 0123456789abcdeffedcba9876543210 in the bq34z950. This is a default and is not intended for production. It should be changed to a unique key prior to production to ensure that security is not compromised.

   For more details, see *Using SHA-1 in bq20Zxx Family of Gas Gauges* (SLUA359).

   The host sends a 20-byte random challenge string. This string must be written to the bq34z950 DQ registers in Little Endian format.

   Little Endian representation is as follows:

   Byte00, Byte01, Byte02, Byte03, Byte04, Byte05, Byte06, Byte07, Byte08, Byte09,
   Byte0A, Byte0B, Byte0C, Byte0D, Byte0E, Byte0F, Byte10, Byte11, Byte12, Byte13

   Big Endian representation is as follows:

   Byte13, Byte12, Byte11, Byte10, Byte0F, Byte0E, Byte0D, Byte0C, Byte0B, Byte0A,
   Byte09, Byte08, Byte07, Byte06, Byte05, Byte04, Byte10, Byte03, Byte02, Byte01, Byte00

2. Implement SHA-1 in the OEM host system.
   (a) The host must know the SHA-1 key defined in Step 1. This key is used in the host system to determine what the response should be.
   (b) The host must issue a random challenge: The host sends a challenge using a 20-byte string write to the SMBus command 0x2F or to the DQ registers in Little Endian format. For SHA-1 over DQ bus, the write of 20 bytes must be followed by a write access to register 0x2F to start the authentication. Any value can be written. It is important that the challenge be random every time to ensure security.
   (c) The host computes the response: With the known SHA-1 authentication key and random challenge, the host computes the anticipated response from the bq34z950.
   (d) bq34z950 computes the response: The bq34z950 computes the response at the same time that the host is computing it. The bq34z950 should be given greater than 22 ms to compute the response and put it into memory or the DQ registers for retrieval.
   (e) The host must read the response: The host reads the response from the same DQ registers to which the challenge was written. The response is a 20-byte string read in Little Endian format.
   (f) The host must validate the response: The host must compare the response read from the bq34z950 to what was computed in Step 2.c above.
   (g) If the response is validated, then the battery is authenticated. Otherwise, the host can reject the pack.

Table 2. DQ COMMAND SET SUMMARY

Symbol	Register Name	Loc. (hex)	Access	Equivalent SMBus Command (see SMBus Command Details for further information)
VBATH	Battery Voltage – High byte	40	Read	*Voltage()* 0x09
VBATL	Battery Voltage – Low byte	41	Read	
CELL4H	Cell 4 Voltage – High byte	42	Read	*VCELL4()* 0x3C
CELL4L	Cell 4 Voltage – Low byte	43	Read	
CELL3H	Cell 3 Voltage – High byte	44	Read	*VCELL3()* 0x3D
CELL3L	Cell 3 Voltage – Low byte	45	Read	
CELL2H	Cell 2 Voltage – High byte	46	Read	*VCELL2()* 0x3E
CELL2L	Cell 2 Voltage – Low byte	47	Read	
CELL1H	Cell 1 Voltage – High byte	48	Read	*VCELL1()* 0x3F
CELL1L	Cell 1 Voltage – Low byte	49	Read	
CYCH	Cycle Count – High byte	4A	Read	*Cyclecount()* 0x17
CYCL	Cycle Count – Low byte	4B	Read	
MFDH	Manufacturers Date – High byte	4C	Read	*ManufactureDate()* 0x1B
MFDL	Manufacturers Date – Low byte	4D	Read	
IH	Current – High byte	4E	Read	*Current()* 0x0A
IL	Current – Low byte	4F	Read	
AVIH	Average Current – High byte	50	Read	*AverageCurrent()* 0x0B
AVIL	Average Current – Low byte	51	Read	
TMPH	Temperature – High byte	52	Read	*Temperature()* 0x08
TMPL	Temperature – Low byte	53	Read	
SNH	Serial Number – High byte	54	Read	*SerialNumber()* 0x1C
SNL	Serial Number – Low byte	55	Read	
CHGVH	Charging Voltage – High byte	56	Read	*ChargingVoltage()* 0x15
CHGVL	Charging Voltage – Low byte	57	Read	
CHGIH	Charging Current – High byte	58	Read	*ChargingCurrent()* 0x14
CHGIL	Charging Current – Low byte	59	Read	
RSOC	Relative State of Charge	5A	Read	*RelativeStateofCharge()* 0x0D
ASOC	Absolute State of Charge	5B	Read	*AbsoluteStateofCharge()* 0x0E
MERH	Max Error – High byte	5C	Read	*MaxError()* 0x0C
MERL	Max Error – Low byte	5D	Read	

bq34z950 DQ Command Set Summary, SHA-1

Table 3. bq34z950 DQ COMMAND SET SUMMARY, SHA-1

SYMBOL	REGISTER NAME	LOC. (hex)	ACCESS	NOTE
CB00	Challenge Byte00	1B	R/W	Least significant byte
CB01	Challenge Byte01	1C	R/W	
CB02	Challenge Byte02	1D	R/W	
CB03	Challenge Byte03	1E	R/W	
CB04	Challenge Byte04	1F	R/W	
CB05	Challenge Byte05	20	R/W	
CB06	Challenge Byte06	21	R/W	
CB07	Challenge Byte07	22	R/W	
CB08	Challenge Byte08	23	R/W	

Table 3. bq34z950 DQ COMMAND SET SUMMARY, SHA-1 (continued)

SYMBOL	REGISTER NAME	LOC. (hex)	ACCESS	NOTE
CB09	Challenge Byte09	24	R/W	
CB0A	Challenge Byte0A	25	R/W	
CB0B	Challenge Byte0B	26	R/W	
CB0C	Challenge Byte0C	27	R/W	
CB0D	Challenge Byte0D	28	R/W	
CB0E	Challenge Byte0E	29	R/W	
CB0F	Challenge Byte0F	2A	R/W	
CB10	Challenge Byte10	2B	R/W	
CB11	Challenge Byte11	2C	R/W	
CB12	Challenge Byte12	2D	R/W	
CB13	Challenge Byte13	2E	R/W	Most significant byte
AUTHST	Start Authentication	2F	Write	A write of any value starts the authentication algorithm

SBS Standard Commands

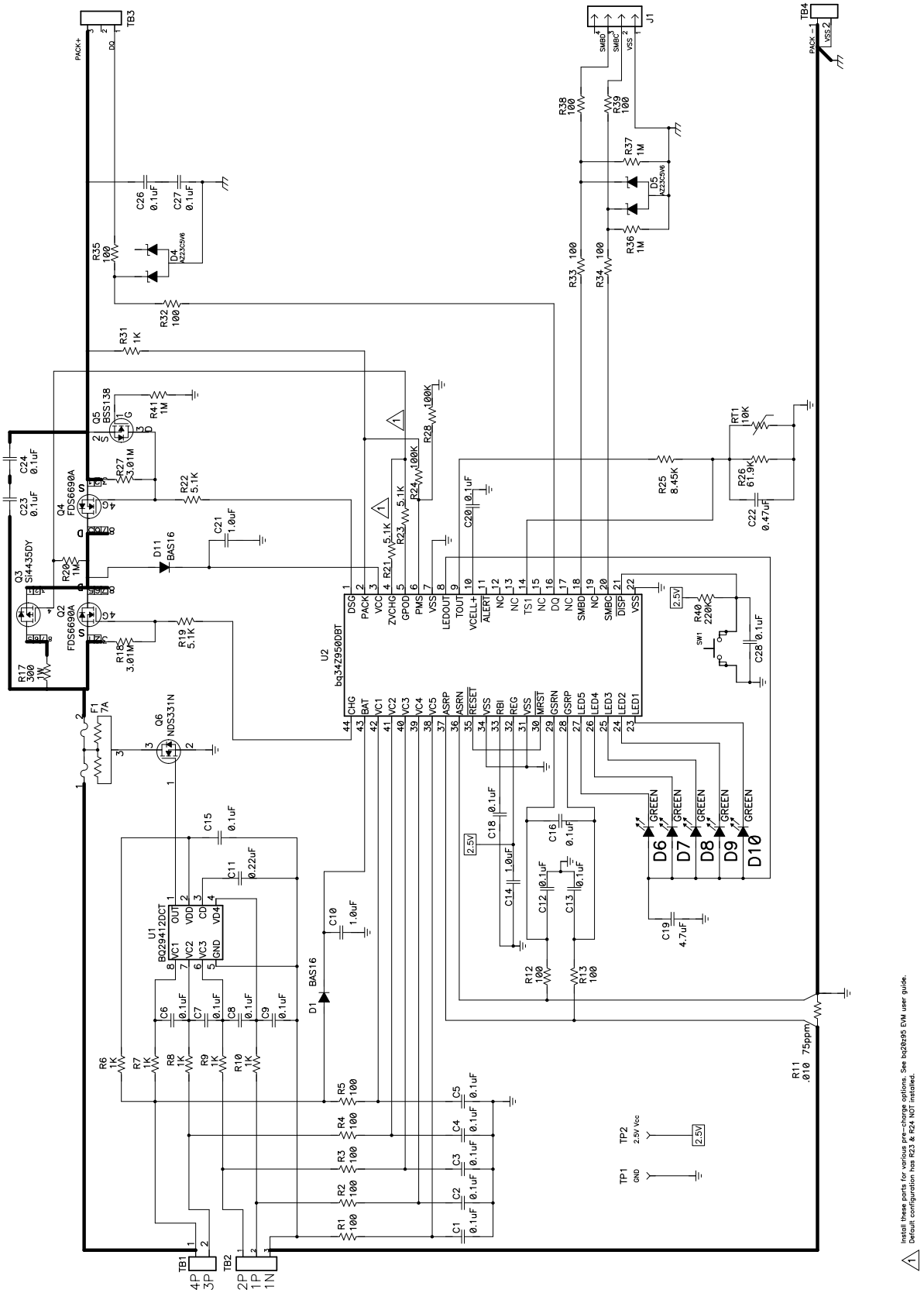
Table 4. SBS STANDARD COMMANDS

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x00	R/W	ManufacturerAccess	Hex	2	0x0000	0xffff	—	
0x01	R/W	RemainingCapacityAlarm	Unsigned int	2	0	65,535	—	mAh or 10 mWh
0x02	R/W	RemainingTimeAlarm	Unsigned int	2	0	65,535	—	min
0x03	R/W	BatteryMode	Hex	2	0x0000	0xffff	—	
0x04	R/W	AtRate	Signed int	2	–32,768	32,767	—	mA or 10 mW
0x05	R	AtRateTimeToFull	Unsigned int	2	0	65,535	—	min
0x06	R	AtRateTimeToEmpty	Unsigned int	2	0	65,535	—	min
0x07	R	AtRateOK	Unsigned int	2	0	65,535	—	
0x08	R	Temperature	Unsigned int	2	0	65,535	—	0.1°K
0x09	R	Voltage	Unsigned int	2	0	20,000	—	mV
0x0A	R	Current	Signed int	2	–32,768	32,767	—	mA
0x0B	R	AverageCurrent	Signed int	2	–32,768	32,767	—	mA
0x0C	R	MaxError	Unsigned int	1	0	100	—	%
0x0D	R	RelativeStateOfCharge	Unsigned int	1	0	100	—	%
0x0E	R	AbsoluteStateOfCharge	Unsigned int	1	0	100	—	%
0x0F	R/W	RemainingCapacity	Unsigned int	2	0	65,535	—	mAh or 10 mWh
0x10	R	FullChargeCapacity	Unsigned int	2	0	65,535	—	mAh or 10 mWh
0x11	R	RunTimeToEmpty	Unsigned int	2	0	65,535	—	min
0x12	R	AverageTimeToEmpty	Unsigned int	2	0	65,535	—	min
0x13	R	AverageTimeToFull	Unsigned int	2	0	65,535	—	min
0x14	R	ChargingCurrent	Unsigned int	2	0	65,535	—	mA
0x15	R	ChargingVoltage	Unsigned int	2	0	65,535	—	mV
0x16	R	BatteryStatus	Unsigned int	2	0x0000	0xffff	—	
0x17	R/W	CycleCount	Unsigned int	2	0	65,535	—	
0x18	R/W	DesignCapacity	Unsigned int	2	0	65,535	—	mAh or 10 mWh
0x19	R/W	DesignVoltage	Unsigned int	2	7,000	16,000	14,400	mV
0x1A	R/W	SpecificationInfo	Unsigned int	2	0x0000	0xffff	0x0031	
0x1B	R/W	ManufactureDate	Unsigned int	2	0	65,535	0	
0x1C	R/W	SerialNumber	Hex	2	0x0000	0xffff	—	
0x20	R/W	ManufacturerName	String	11 + 1	—	—	Texas Instruments	ASCII
0x21	R/W	DeviceName	String	7 + 1	—	—	bq34z950	ASCII
0x22	R/W	DeviceChemistry	String	4 + 1	—	—	LION	ASCII
0x23	R	ManufacturerData	String	14 + 1	—	—	—	ASCII
0x2F	R/W	Authenticate	String	20 + 1	—	—	—	ASCII
0x3C	R	CellVoltage4	Unsigned int	2	0	65,535	—	mV
0x3D	R	CellVoltage3	Unsigned int	2	0	65,535	—	mV
0x3E	R	CellVoltage2	Unsigned int	2	0	65,535	—	mV
0x3F	R	CellVoltage1	Unsigned int	2	0	65,535	—	mV

Table 5. EXTENDED SBS COMMANDS

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x45	R	AFEData	String	11 + 1	—	—	—	ASCII
0x46	R/W	FETControl	Hex	1	0x00	0xff	—	
0x4F	R	StateOfHealth	Unsigned int	1	0	100	—	%
0x51	R	SafetyStatus	Hex	2	0x0000	0xffff	—	
0x53	R	PFStatus	Hex	2	0x0000	0xffff	—	
0x54	R	OperationStatus	Hex	2	0x0000	0xffff	—	
0x55	R	ChargingStatus	Hex	2	0x0000	0xffff	—	
0x57	R	ResetData	Hex	2	0x0000	0xffff	—	
0x5A	R	PackVoltage	Unsigned int	2	0	65,535	—	mV
0x5D	R	AverageVoltage	Unsigned int	2	0	65,535	—	mV
0x60	R/W	UnSealKey	Hex	4	0x0000 0000	0xffff ffff	—	
0x61	R/W	FullAccessKey	Hex	4	0x0000 0000	0xffff ffff	—	
0x62	R/W	PFKey	Hex	4	0x0000 0000	0xffff ffff	—	
0x63	R/W	AuthenKey3	Hex	4	0x0000 0000	0xffff ffff	—	
0x64	R/W	AuthenKey2	Hex	4	0x0000 0000	0xffff ffff	—	
0x65	R/W	AuthenKey1	Hex	4	0x0000 0000	0xffff ffff	—	
0x66	R/W	AuthenKey0	Hex	4	0x0000 0000	0xffff ffff	—	
0x70	R/W	ManufacturerInfo	String	8 + 1	—	—	—	
0x71	R/W	SenseResistor	Unsigned int	2	0	65,535	—	µΩ
0x77	R/W	DataFlashSubClassID	Hex	2	0x0000	0xffff	—	
0x78	R/W	DataFlashSubClassPage1	Hex	32	—	—	—	
0x79	R/W	DataFlashSubClassPage2	Hex	32	—	—	—	
0x7A	R/W	DataFlashSubClassPage3	Hex	32	—	—	—	
0x7B	R/W	DataFlashSubClassPage4	Hex	32	—	—	—	
0x7C	R/W	DataFlashSubClassPage5	Hex	32	—	—	—	
0x7D	R/W	DataFlashSubClassPage6	Hex	32	—	—	—	
0x7E	R/W	DataFlashSubClassPage7	Hex	32	—	—	—	
0x7F	R/W	DataFlashSubClassPage8	Hex	32	—	—	—	

APPLICATION SCHEMATICS



REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Deleted 特性列表中的使用寿命数据资料记录	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ34Z950DBT	ACTIVE	TSSOP	DBT	44	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ34Z950	Samples
BQ34Z950DBTR	ACTIVE	TSSOP	DBT	44	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ34Z950	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

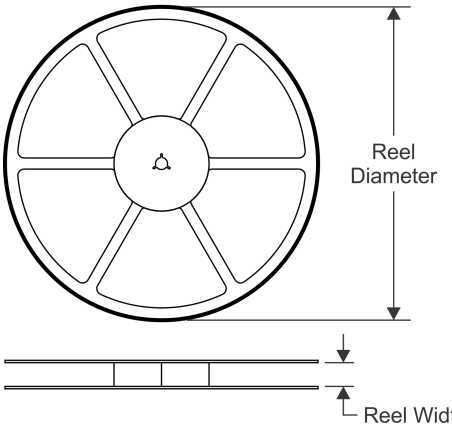
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

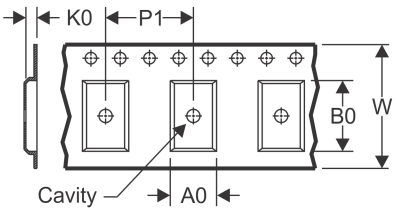
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

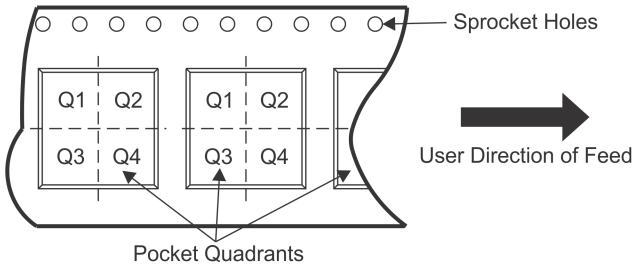


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

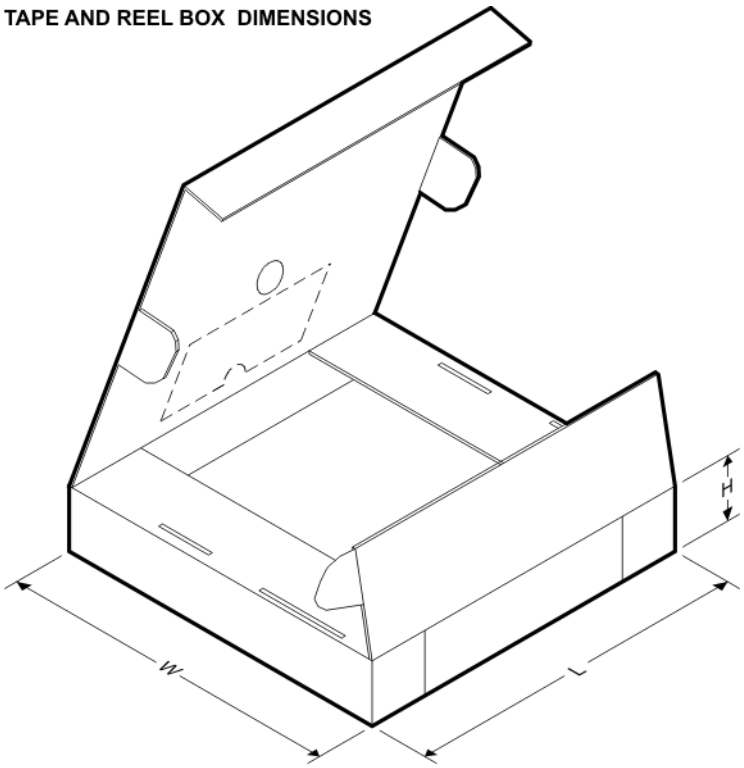
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ34Z950DBTR	TSSOP	DBT	44	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

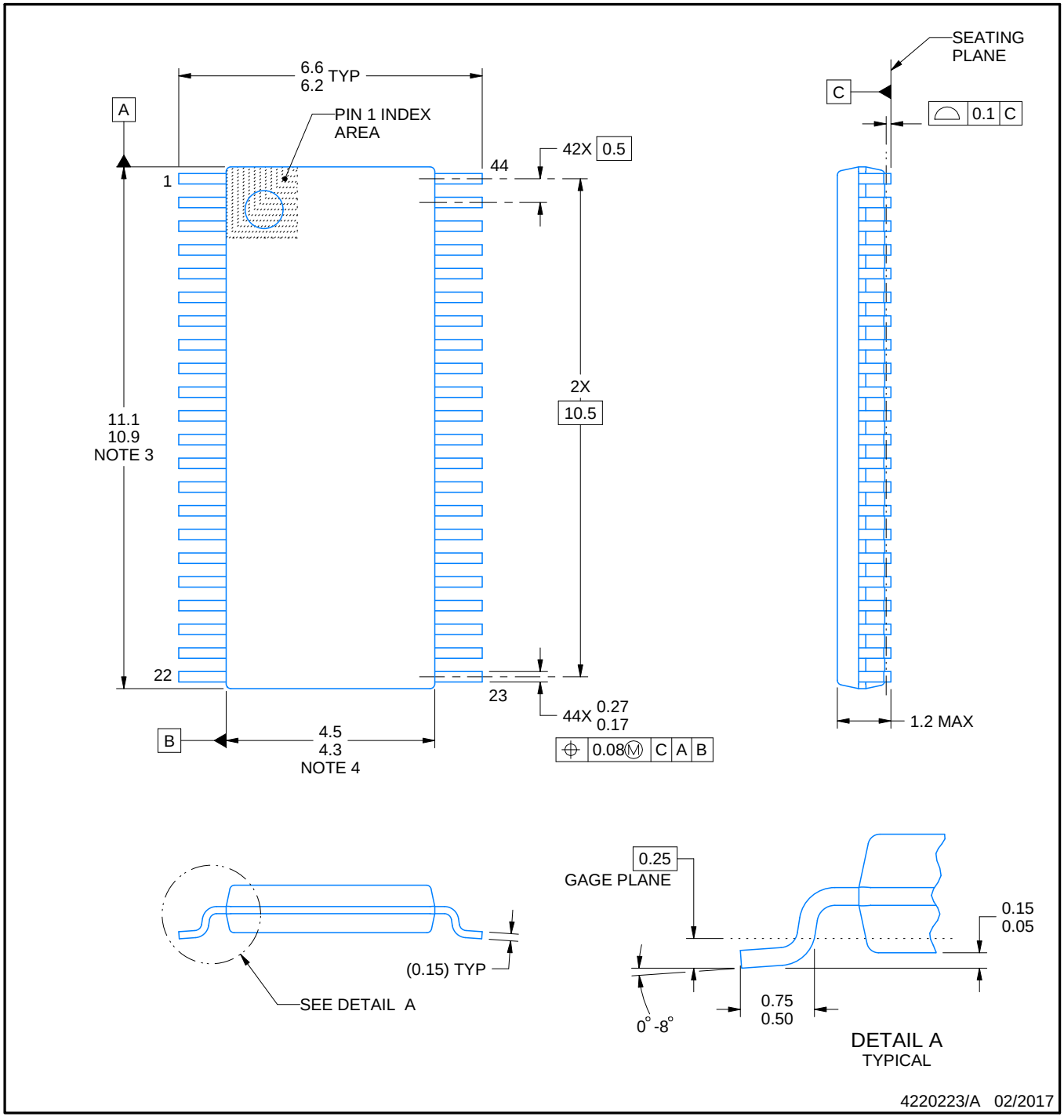
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ34Z950DBTR	TSSOP	DBT	44	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DBT0044A

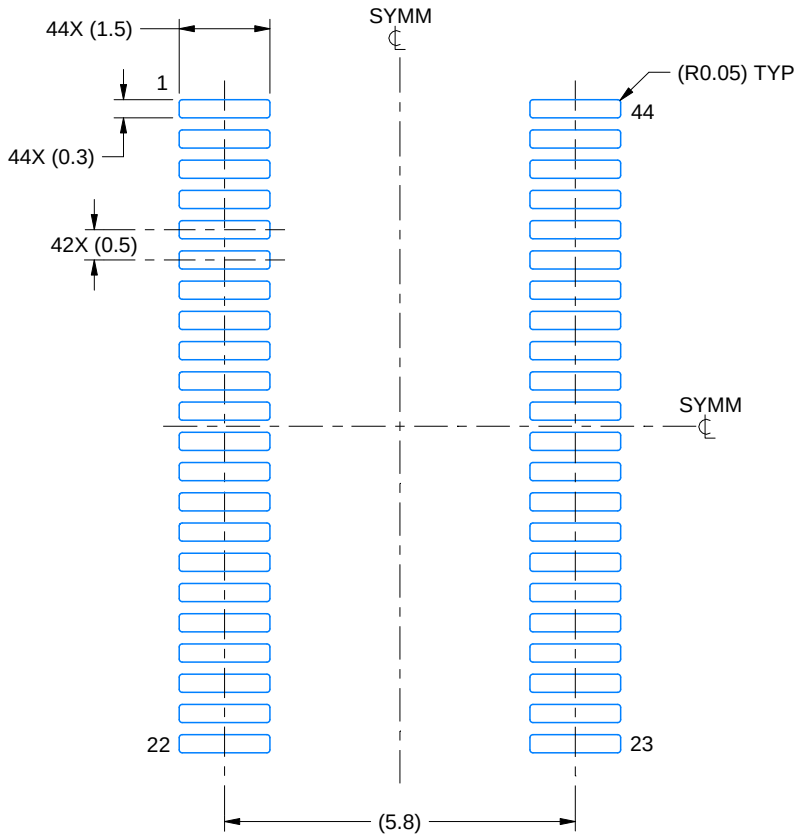
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

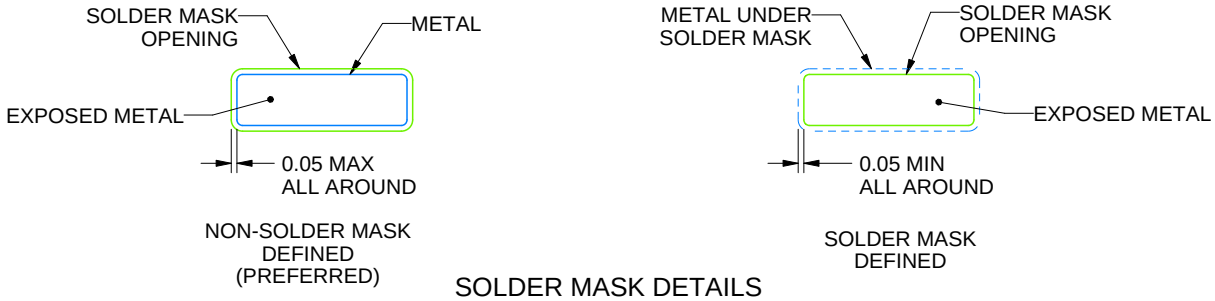


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

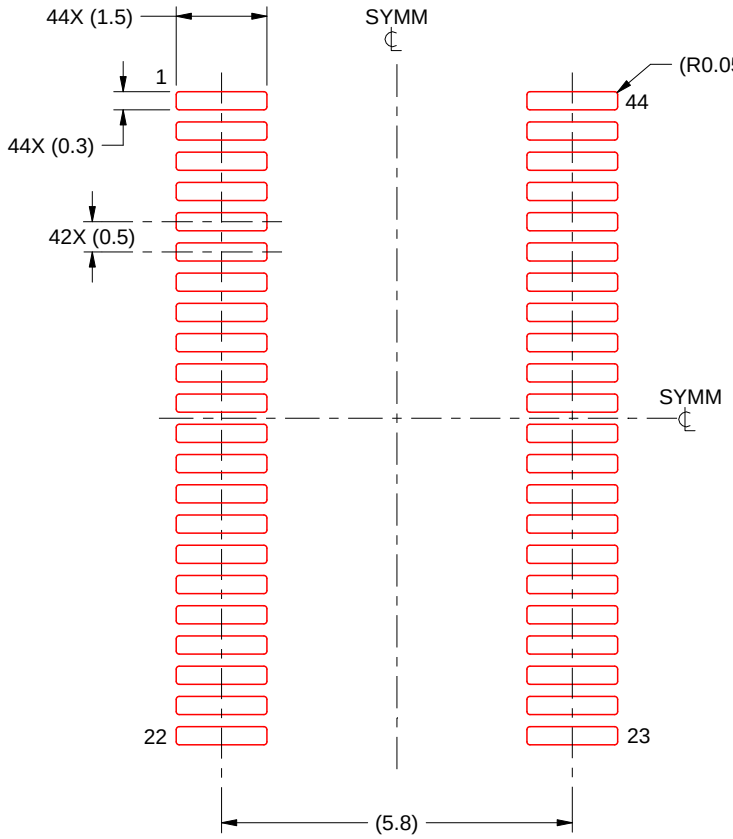


SOLDER MASK DETAILS

4220223/A 02/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4220223/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122