

RoHS

Built in VCXO, **Spread-Spectrum Clock Generator**

BU3087FV

Description

BU3087FV has built in VCXO that is necessary for the Digital-TV signal reception.

Connecting 27MHz crystal oscillator generates clock signals to 74.25MHz for Hi-Vision.

BU3087FV has built in Spread-Spectrum function too.

Features

- 3225 size crystal is usable
- ON / OFF of Spread-Spectrum is selectable
- Four kinds of Modulation-Rate is selectable $(\pm 0.25\% / \pm 0.50\% / \pm 0.75\% / \pm 1.00\%)$
- **Triangular Modulation**

Applications

Digital-TV, STB, TV-Tuner

Key Specifications

Package

- Crystal Pullability
- Modulation Frequency
- Cycle-to-Cycle Jitter
- 34.5kHz (Typ.) 180psec (Typ.)

±105ppm (Typ.)

- 45mA (Typ.) -10°C to +75°C
- **Operating Current Operating Temperature**

(Typ.) (Typ.) (Max.) 5.00mm x 6.40mm x 1.35mm



Typical Application Circuit 3.3V (Typ.) 27MHz Crystal CL CL Śrd XIN XOUT AVDD1 PDB 0.1 μ F CLKOUT AVSS1 VCTRL VDD 0.1 *µ* F VSS AVDD2 0.1 µ F AVSS2 SSON MODSEL1 TEST MODSEL2 CLK27M \cap Figure 1. Typical Application Circuit

(Caution) CL and RD in Typical Application Circuit should be optimized as to using crystal and board condition.

OProduct structure : Silicon monolithic integrated circuit OThis product is not designed protection against radioactive rays

BU3087FV

Block Diagram



Figure 2. Block Diagram

Pin Configuration



Figure 3.Pin Configuration (TOP VIEW)

Pin Function

PIN No.	PIN Name	Function
1	XIN	Crystal Input terminal
2	AVDD1	Power supply for VCXO
3	AVSS1	GND for VCXO
4	VCTRL	VCXO control input terminal
5	AVDD2	Power supply for PLL-Analog
6	AVSS2	GND for PLL-Analog
7	MODSEL1	Spread-Spectrum Modulation control terminal (Refer to Table of Spread-Spectrum Modulation) with pull-up
8	MODSEL2	Spread-Spectrum Modulation control terminal (Refer to Table of Spread-Spectrum Modulation) with pull-down
9	CLK27M	27.00000MHz Output
10	TEST	Test terminal, with pull-down
11	SSON	Spread-Spectrum ON \diagup OFF choice (H : ON, L : OFF) , with pull-up
12	VSS	GND for PLL-Digital
13	VDD	Power supply for PLL-Digital
14	CLKOUT	74.250000MHz Output
15	PDB	Power-down control terminal, with pull-up
16	XOUT	Crystal Output terminal

• Table of Spread-Spectrum Modulation (1Pin_XIN input frequency = 27.000000MHz)

In the case of 11Pin_SSON=H, outputs it according to the following table.

MODSEL2	MODSEL1	CLKOUT
L	L	74.250000MHz ±0.25% Modulation
L	Н	74.250000MHz ±0.50% Modulation
Н	L	74.250000MHz ±0.75% Modulation
н	Н	74.250000MHz ±1.00% Modulation

In the case of 11Pin • SSON=L, outputs unmodulated clock.

● Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.0	V
Input Voltage	VIN	-0.3 to VDD+0.3	V
Storage Temperature range	Tstg	-55 to 125	°C
Power dissipation	PD	690 ^{%1}	mW

A measure value at mounting on 70mm x 70mm x 1.6mm glass epoxy substrate. In the case of exceeding Ta=25°C, 6.9mW should be reduced per 1°C.

Recommended Operating Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	3.135 to 3.465	V
Input "H" Voltage	VIH	0.8VDD to VDD	V
Input "L" Voltage	VIL	0.0 to 0.2VDD	V
Operating Temperature	topr	-10 to 75	°C
Frequency Control Voltage	Vc	0.0 to VDD	V
Output load	CL	15 (MAX)	pF

*1 In case of Output load exceeds previous value , consideration should be adapted Rise Time and Fall Time for condition of use.

•Electrical Characteristics

DC Characteristics

(VDD=3.3V, Ta=25°C, Crystal Frequency=27.000000MHz, at No Load, unless otherwise specified)

Parameter	Symbol		Limit		Unit	Conditions	
Parameter	Symbol	Min.	Тур.	Max.	Unit		
Output H voltage	VOH	VDD-0.4	—	_	V	IOH=4.0mA	
Output L voltage	VOL	_	_	0.4	V	IOL=4.0mA	
Operating Circuit current	IDD	_	45.0	58.0	mA	Output no load, ±0.50% Modulation	
Input H current 1	lupH	-1.5	-	1.5	μA	PDB, SSON, MODSEL1 Terminal VIH=VDD	
Input H current 2	ldnH	35.0	70.0	105.5	μA	MODSEL2, TEST Terminal, VIH=VDD	
Input H current 3	IdirH	-1.5	-	1.5	μA	VCTRL Terminal, VIH=VDD	
Input L current 1	lupL	-105.5	-70.0	-35.0	μA	PDB, SSON, MODSEL1 Terminal VIL=0.0V	
Input L current 2	IdnL	-1.5	_	1.5	μA	MODSEL2, TEST Terminal,VIL=0.0V	
Input L current 3	IdirL	-1.5	-	1.5	μA	VCTRL Terminal,VIL=0.0V	
CLKOUT	CLKOUT	74.248144	74.250000	74.251856	MHz	VCTRL=1/2VDD	
Crystal Pullability	fp	±80	±105	±130	ppm	0≦VCTRL≦VDD ^{%1}	
Spread-Spectrum Modulation Frequency	Fmod	32.5	34.5	36.5	kHz	Triangular Modulation, Independently of Modulation Rate	

*1 This is a guarantee with only IC. It is finished with confirmation to operate with Crystal (DSX321G • 8pF load) made in DAISHINKU CORP.

AC Characteristics

(VDD=3.3V, Ta=25°C, Crystal Frequency=27.000000MHz, Output load=15pF, unless otherwise specified)

Following the table cannot test directly on characteristic when shipment, so it is a design guarantee.

Devenueter	Currential	Limit			ال الم ال	Conditions	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Duty	Duty	45	50	55	%	Measured at 1/2VDD	
Jitter 1 σ	JsSD		35		0000	Period Jitter 1 σ^{*2} ,	
JILLEI TO	J22D				psec	in Spread-Spectrum OFF	
Jitter P-P	JsABS		180		0000	Period Jitter MIN-MAX value ^{**2} ,	
Jiller P-P	JSADO		100	_	psec	in Spread-Spectrum OFF	
Jitter			180		0000	Cycle-to-Cycle Jitter,	
Cycle-to-Cycle	JsCyCy		160	—	psec	In ±0.50% Modulation	
Rise Time	Tr	_	1.2	—	nsec	Time between 0.2VDD and 0.8VDD	
Fall Time	Tf	_	0.7	_	nsec	Time between 0.8VDD and 0.2VDD	
Lock Up Time	Tlock	_	_	1	msec	<u>*3</u>	

^{#2} Jitter means center value when using Japan Tektronix : TDS7104 Digital Phosphor Oscilloscope.

*3 Time between voltage supply leads to 3.135V and output clock gets stable.

Spread-Spectrum Modulation Waveform

Modulation Waveform is triangular. Modulation Rate is selectable among $\pm 0.25\% / \pm 0.50\% / \pm 0.75\% / \pm 1.00\%$. In addition, Modulation Frequency is 34.5kHz without depending on Modulation Rate. (Figure 4 shows $\pm 0.50\%$ Modulation Waveform.)



Figure 4. Spread-Spectrum Modulation Waveform

●Typical Wave Forms (VDD=3.3v, Ta=25°C, Spread-Spectrum OFF setting)





TIME (1nsec/div.) Figure 8. CLKOUT Period-Jitter









●Typical Wave Forms (VDD=3.3v, Ta=25°C, Spread-Spectrum ON setting)



FREQUENCY (500kHz/div.) Figure 25. CLKOUT±0.25% Modulation Spectrum



FREQUENCY (500kHz/div.) Figure 26. CLKOUT±0.50% Modulation Spectrum



FREQUENCY (500kHz/div.) Figure 27. CLKOUT±0.75% Modulation Spectrum



FREQUENCY (500kHz/div.) Figure 28. CLKOUT±1.00% Modulation Spectrum

●Typical Wave Forms (VDD=3.3v, Ta=25°C, Spread-Spectrum ON setting)



TIME (20µsec/div.) Figure 29. CLKOUT±0.25% Modulation Waveform



 $\label{eq:time_time} \begin{array}{c} \text{TIME} \mbox{ (20} \mbox{ µsec/div.)} \\ \text{Figure 30. CLKOUT} \pm 0.50\% \mbox{ Modulation Waveform} \end{array}$



TIME (20µsec/div.) Figure 31. CLKOUT±0.75% Modulation Waveform



TIME (20µsec/div.) Figure 32. CLKOUT±1.00% Modulation Waveform



Modulation Frequency has a same characteristic despite a Modulation control. Modulation Rate has a same trend despite a control.







VCXO Crystal Pullability has been gathered from following the evaluation environment.

Evaluation board: 70mm x 70mm x 1.6mm, 4 layers, FR-4

Using parts : 27MHz Crystal (DSX321G · 8pF load) made in DAISHINKU CORP. RD=200 \, CL=4pF

VCXO Crystal Pullability modulates by a using crystal and a board condition. In order to use, should be checked matting with a final board condition.

Typical Application Circuit

In the case of Spread-Spectrum Modulation Rate = $\pm 0.75\%$ setting, 7Pin_MODSEL1 connects GND, and 8Pin_MODSEL2 connect Power supply directly following the diagram.

In the case of other Modulation Rate setting, should be changed connections as a Table of Spread-Spectrum Modulation (P3). (In the case of $\pm 0.50\%$ setting, it is no problem that 7Pin_MODSEL1 and 8Pin_MODSEL2 are OPEN Manages.)



Figure 48. Modulation Rate =±0.75% setting Typical Application Circuit

In the case of Spread-Spectrum OFF setting, 11Pin_SSON connect GND directly as the following diagram. (In the case of using Spread-Spectrum, it is no problem that 11Pin_SSON are OPEN Manages.)



Figure 49. Spread-Spectrum OFF setting Typical Application Circuit

Application Information

Basically, mount ICs to the printed circuit board for use. (If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)

Mount 0.1µF capacitors in the vicinity of the IC Pins between 2Pin_AVDD1, 3Pin_AVSS1, and 5Pin_AVDD2, 6Pin_AVSS2, and 12Pin_VSS, 13Pin_VDD respectively.

To obtain accurate frequency, confirm the Crystal-matching with the last board to get rid of a problem by a mass-production.

Depending on the conditions of the printed circuit board, mount an additional electrolytic capacitor between the power supply and GND terminal.

For EMI protection, it is effective to put ferrite beads in the origin of power supply to be fed to BU3087FV from the printed circuit board or to insert a capacitor (of 1Ω or less), which bypasses high frequency desired, between the power supply and the GND terminal.

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

Typical Application Circuit is recommendation, but in order to use, thoroughly check to be sure characteristic.

Power Dissipation

(SSOP-B16 package)



Figure 50. Power Dissipation Curve (Pd-Ta Curve)

●I/O Equivalence Circuit



●I/O Equivalence Circuit



Operational Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

BU3087FV

Ordering Information 8 7 F E 2 В U 3 0 V _ Part Number Package Packaging and forming specification FV: SSOP-B16 E2: Embossed tape and reel

Physical Dimension Tape and Reel Information

SSOP-B16



Marking Diagram



Revision History

Date	Revision	Changes
17.AUG.2012	001	New Release

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