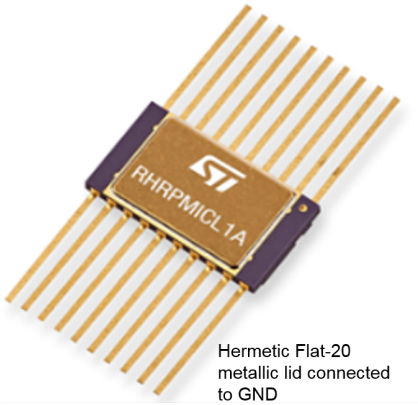
RHRPMICL1A

Datasheet

Rad-hard integrated current limiter



Hermetic Flat-20 metallic lid connected to GND

Maturity status link
RHRPMICL1A

Features

- Wide-range supply voltage: 8.5 - 90 V DC (Qualified in radiation at V_{CC} from 8.5 V to 52 V)
- Very low DC current: typ. 1.5 mA
- External current limitation setting
- 3 types of operation
  - Re-triggerable
  - Latched
  - Foldback
- Configurable trip-off and recovery times
- Smart current limitation for repetitive overload
- Embedded current sense
- Configurable undervoltage protection
- Floating ground
- Flat-20 hermetic package
- Radiation hardened
  - TID : 100 krad (Si) HDR, LDR
  - SEL and SEU free up to 78 MeV.cm²/mg
  - SET report available upon request
- QML-V qualified SMD 5962-17211
- Evaluation boards available

Description

The RHRPMICL1A is an integrated current limiter designed to work with an external P-channel power MOSFET.

It can be used as a universal solution to protect a power supply (from 8.5 V) from anomalous external current demand (for example, in case the load enters latch-up conditions).

It can protect or replace conventional fuses and can also be used to control redundant loads.

The RHRPMICL1A features 3 user-configurable operating modes (re-triggerable, latched, foldback), with different behaviors in case of overload/short-circuit events.

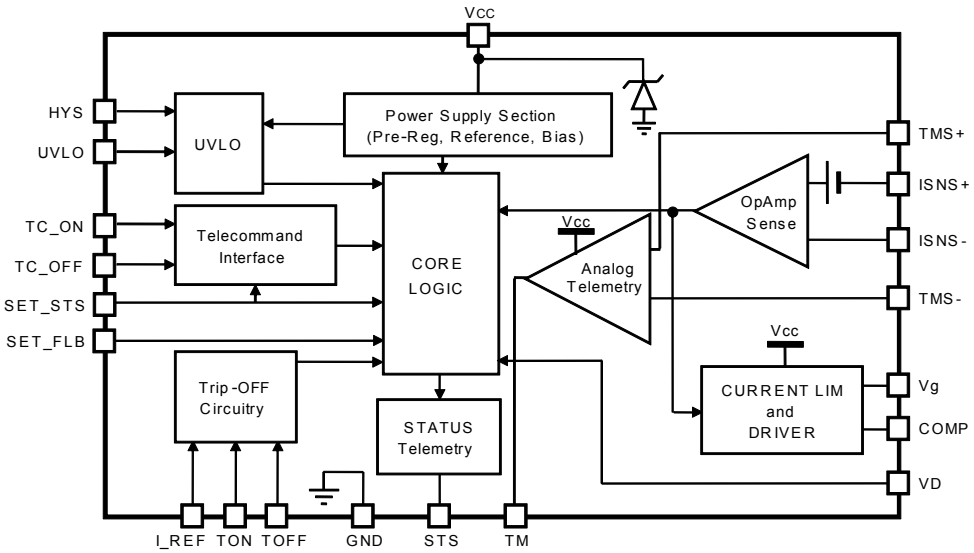
All key parameters of the application, including the current limit, the trip-off and recovery times and the undervoltage protection are user configurable, making the RHRPMICL1A suitable for a wide range of applications.

Telemetry pins (STS and TM) and telecommand pins (TC_ON and TC_OFF) allow the device respectively to be monitored and controlled and the power on the load to be managed properly.

The RHRPMICL1A is designed in ST's proprietary BCD6s-SOI technology to provide total dose and heavy ion radiation hardness. Housed in a hermetic Flat-20 package assembled in ST's QML-V certified facility, it is ideally suited for harsh environments.

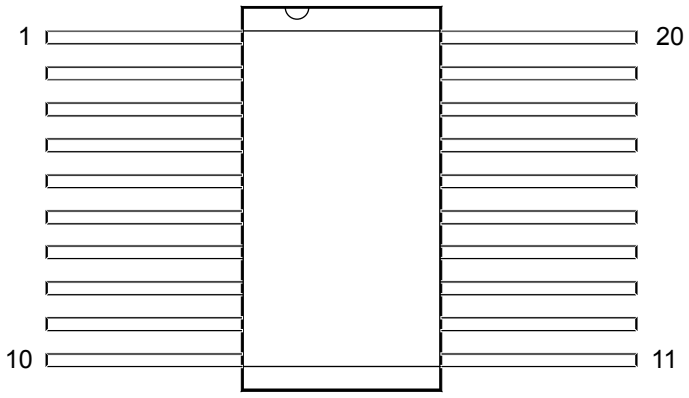
1 Block diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. **Pin connections (top view)**



Note: Metallic lid is connected to ground.

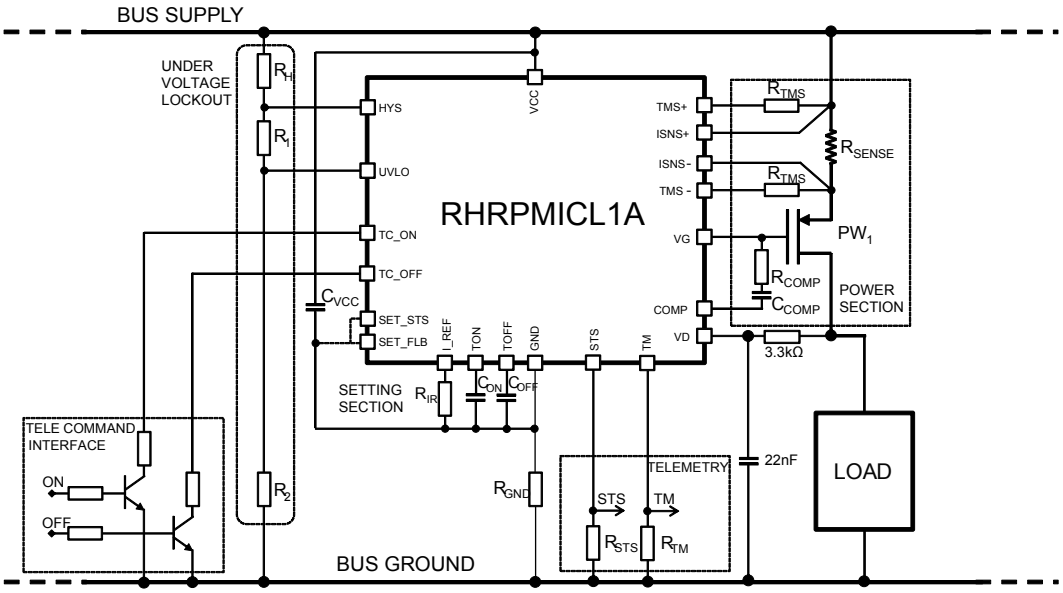
Table 1. **Pin description**

Pin	Name	Type	Description
1	SET_STS	Digital input	Configuration pin. If shorted to GND, the current limiter at power- up is OFF. If connected to V_{CC}, the current limiter at power-up is normally ON.
2	TC_OFF	Digital input	Telecommand interface input for OFF pulsed signal.
3	SET_FLB	Digital input	Configuration pin. If connected to V_{CC}, the foldback mode is enabled.
4	TON	Analog output	Used to set the trip-off time T_{ON}. A capacitor C_{ON} is connected between this pin and GND.
5	TOFF	Analog output	Used to set the recovery time T_{OFF}. This pin has a double functionality. If the C_{OFF} capacitor is connected between this pin and GND, it sets the T_{OFF} value in re-triggerable mode. If the pin is shorted-to-GND, the device is configured in latched mode.
6	I_REF	Analog onput/output	Used to set the current reference. An external high-precision resistor is connected between this pin and GND in order to set the current reference.
7	GND	Power supply	Ground. Return of the bias current and zero-voltage reference for all internal voltages. Connected to the main bus ground through a decoupling resistor to operate in floating ground configuration.
8	VD	Analog input	Sense pin of the external MOSFET drain voltage used to detect current limitation. A small series resistor can be useful to reduce power dissipation.
9	STS	Digital output	Telemetry digital status. A resistor has to be connected between the pin and the main bus ground.
10	TMS+	Analog input	Non-inverting input of the telemetry circuit. An accurate external resistor is connected between ISNS+ and this pin in order to guarantee the requested accuracy on the output source current for the analog telemetry.

Pin	Name	Type	Description
11	TMS-	Analog input	Inverting input of the telemetry circuit. An accurate external resistor is connected between ISNS- and this pin in order to guarantee the requested accuracy on the output source current for the analog telemetry.
12	TM	Analog output	Output source current for the analog telemetry. A resistor has to be connected between this pin and the main bus ground.
13	COMP	Analog output	Output pin for current limitation loop compensation.
14	Vg	Analog output	MOSFET gate driver output.
15	ISNS-	Analog input	Inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (negative) end of the external current sense resistor. Never leave this pin floating.
16	ISNS+	Analog input	Non-inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (positive) end of the external current sense resistor. Never leave this pin floating.
17	V_{CC}	Power supply	Supply input voltage.
18	HYS	Analog output	External setting of the UVLO hysteresis. A resistor has to be connected between the main bus and this pin.
19	TC_ON	Digital input	Telecommand interface input for ON pulsed signal.
20	UVLO	Analog input	External setting of the UVLO turn-on threshold. The pin has to be tied to the mid point of a resistor divider that senses the supply voltage vs. main bus ground.

3 Typical application diagram

Figure 3. Typical application circuit



Note: The resistors R_{GND}, R_{STS} and R_{TM} are critical for the safety of the application. Please refer to Section 8 Application guidelines.

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature	-65 to 150	°C
T_J	Maximum operating junction temperature	150	°C
V_{HBM}	ESD capability, human body model	2k	V
SET_STS	Digital input	-0.3 to (V_{CC} + 0.3)	V
TC_OFF	Digital input	-40 to (V_{CC} + 0.3)	V
SET_FLB	Digital input	-0.3 to (V_{CC} + 0.3)	V
TON	Analog output	-0.3 to +4.6	V
TOFF	Analog output	-0.3 to +4.6	V
I_REF	Analog input/output	-0.3 to +4.6	V
GND	Device ground	-	
VD	Analog input	-40 to (V_{CC} + 0.3)	V
STS	Digital output	-40 to (V_{CC} + 0.3)	V
TMS+	Analog input	-0.3to (VCC+0.3)	V
TMS-	Analog input	-0.3 to (V_{CC} + 0.3)	V
TM	Analog output	-40 to (V_{CC} + 0.3)	V
COMP	Analog output	-0.3 to (V_{CC} + 0.3)	V
Vg	Analog output	-40 to (V_{CC} + 0.3)	V
ISNS-	Analog input	-0.3 to (V_{CC} + 0.3)	V
ISNS+	Analog input	-0.3 to (V_{CC} + 0.3)	V
V_{CC}	Power supply	-0.3 to + 54.0	V
HYS	Analog output	-0.3 to (V_{CC} + 0.3)	V
TC_ON	Digital input	-40 to (V_{CC} + 0.3)	V
UVLO	Analog input	-0.3 to (V_{CC} + 0.3)	V

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	40	°C/W

5 Electrical characteristics

T_J = - 55 °C to 125 °C, V_{CC} = 37 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	System operating supply voltage		8.5		52	V
Supply current and UVLO						
V_Z	V_{CC} vs. GND internal clamp voltage		13.6	14.8	16	V
$I_{CC}ON$	Supply current, on-state	V_{CC} - GND < V_Z		1.5	3	mA
$I_{CC}OFF$	Supply current, off-state	V_{CC} - GND < V_Z		1.5	3	mA
V_{TH}	Undervoltage lockout turn-on threshold	R1 = 20 kΩ, R2 = 220 kΩ, Rh = 1.6 kΩ	28	30	32	V
	Undervoltage lockout hysteresis		1.6	1.8	2	V
V_{IREF}	Voltage reference to set the charging current for trip-off section	R_{I_REF} = 120 kΩ	1.2	1.256	1.3	V
Current limitation						
V_{LIM}	Current limitation sense voltage threshold (between ISNS+ and ISNS-)		90	100	110	mV
Driver						
V_gON	Gate voltage range, on state			V_{CC}- 12		
V_gOFF	Gate voltage range, off state				V_{CC}	V
I_g	Gate source current (1)	During a current limitation event		200		mA
Trip-OFF function						
T_{ON}	Trip-off time	R_{I_REF} = 120 kΩ C_{ON} = 10 nF	1.1	1.2	1.4	ms
T_{OFF}	Recovery time	R_{I_REF} = 120 kΩ C_{ON} = 10 nF C_{OFF} = 47 nF	100	112	140	ms
Switching times						
T_{DELAY}	Delay time (from TC_ON to Vout=0 to 10%)	Latched OFF configuration, I_{SENSE} = 5 mA (see Table 10. Device configuration truth table)		90		ms
T_{RISE}	Rise time (Vout from 10% to 90%)			60		
T_{FALL}	Fall time (Vout from 90% to 10%)			30		
$T_{STORAGE}$	Storage time (from TC_OFF to Vout= 10%)			70		
Telecommand						
V_{TC_ON} V_{TC_OFF}	Telecommand input voltage turn-on/off		2	2.8	3.6	V
T_{pulse}	Telecommand minimum pulse time		30	100		µs
T_{pulse_noise}	Telecommand immunity pulse time				10	µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Telemetry						
V_{TM}	Telemetry output voltage range	R_{SENSE} = 100 mΩ R_{TMS} = 5 kΩ R_{TM} = 240 kΩ I_{SENSE} = 500 mA	2.2	2.4	2.6	V
$V_{TM(OFF)}$	Telemetry output voltage range, off state	R_{SENSE} = 100 mΩ R_{TMS} = 5 kΩ R_{TM} = 240 kΩ I_{SENSE} = 0 mA		MGND		V
Status						
V_{STATUS}	STS output voltage range		4.4	5	5.6	V
$V_{STATUS(OFF)}$	STS output voltage range, off state	R_{STS} = 50 kΩ		MGND		

1. *Guaranteed by design.*

Note: The operating range of current limitation and load depends on the current capability of the power MOS. This range can be extended to higher values according to the current capability of the power MOS.

Undervoltage lockout threshold calculation (see Figure 3. Typical application circuit):

$V_{ON} = V_{TH} = 2.5\ V * ((R_1 + R_2) / R_1)$; $V_{OFF} = 2.5\ V * ((R_1 + R_2 + R_H) / (R_1 + R_H))$; $V_{HY} = V_{TH} - V_{OFF}$

MGND is the main bus ground voltage.

6 Radiations

6.1 Total ionizing dose (MIL-STD-883 test method 1019)

The products that are guaranteed in radiation within RHA QML-V system, fully comply with the MIL-STD-883 test method 1019 specification. The RHRPMICL1A is being RHA QML-V qualified, tested and characterized in full compliance with the MIL-STD-883 specification, both below 10 mrad/s (low dose rate) and between 50 and 300 rad/s (high dose rate).

Testing is performed in accordance with MIL-prf-38535 and the test method 1019 of the MIL-STD-883 for total ionizing dose (TID).

ELDRS characterization is performed in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.

Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Table 5. TID test results

Feature	Conditions	Max. value	Unit
Total-ionization dose immunity	50 rad(Si)/s high dose rate up to 100 krad(Si) Compliance with electrical specification	100	krad(Si)
	10 mrad(Si)/s low dose rate Compliance with electrical specification	100	
	Enhanced low dose rate sensitivity (ELDRS) Compliance with electrical specification	100	

6.2 Heavy ions

The heavy-ion trials are performed on qualification lots only. No additional test is performed. It has been performed according to single event effects test method and guidelines ESA/SCC basic specification number 25100 and ASTM F1192. SEL tests have been performed at UCL (BE). SET have been characterized in RADEF (FI). Table below summarizes the results of heavy ions tests.

The products does not feature any flip-flop nor registers and is therefore intrinsically SEU immune.

Table 6. Heavy ions results

Feature	Parameter	Conditions	Value		Unit
			Nom.	Max.	
SEL/SEB immunity	SEL/SEB linear energy transfer (LET)	Range ≥ 35 µm test on 4 parts at V_{CC} = 52 V. No destructive events	-	125	MeV.cm2/mg
SEU immunity	SEU linear energy transfer (LET) (1)		Immune		
SET performance	SET linear energy transfer threshold (LETth)	10 V < V_{CC} < 52 V	9	-	MeV.cm2/mg
	SET saturated cross section (2)		1.4x10-5	-	-

1. *The product does not include any register, flip-flop or memory cell. It is therefore intrinsically SEU immune.*
2. *Most of the events are trigged on VG signal, few on TM signal.*

7 Device description and operation

The RHRPMICL1A (integrated current limiter) is a versatile monolithic device designed for satellite applications and used as a high-side gate driver or intelligent power switch driver, to provide current limitation in power distribution systems in order to protect the main bus in case of excessive current demands.

The device can operate with a supply voltage ranging from 8.5 V to 52 V. An undervoltage lockout circuitry is implemented to guarantee appropriate power supply integrity. Because of the specificity of the harsh environment and the wide spectrum of the supply voltage that can be requested, this device can be configured to protect a broad variety of functional essential and non-essential loads fed by the power distribution unit.

Incase of overload, the device behavior changes according to its configured mode of operation:

- If the current limiter is configured in re-triggerable mode, after the trip-off time T_{ON}, the device switches off and remains in this state for a recovery time T_{OFF} that is externally programmable. Once this time elapses, the device switches cyclically on and off again while the overload persists, otherwise it recovers its normal operation mode if the overload disappears.
- If configured in foldback mode, in case of overload the device provides current limitation with a value decreasing with the output voltage, reaching a fixed and safe value even if a short-circuit persists.
- If configured in latched mode, the device itself provides current limitation capability for an externally configurable time T_{ON}, called trip-off time, and if the overcurrent condition exceeds this time, the device switches off. In this case, the device may be switched on again only through the telecommand pin or cycling OFF/ON the UVLO thresholds.

The core of the device consists of the driver block, designed to drive an external P-channel power MOSFET connected in high-side configuration. Current sensing, current limitation detection, remote control, telemetry and protection functions are also included allowing the design of high reliability systems.

The device is tailored to meet the need for complete control and protection of the loads, in those applications working in harsh environments, whether it is mandatory to secure the essential functionalities (e.g. on board computer, etc.) or not (instruments etc.). Thanks to the remote monitor and telecommand interface features, the RHRPMICL1A permits full control and partitioning of each load connected to the device.

7.1 Supply voltage, startup and undervoltage lockout

The device can be directly supplied with a voltage in the 8.5 V - 52 V range. A Zener diode chain is embedded in order to clamp the voltage level between V_{CC} and GND at about 15 V (typ. 14.8 V).

The device can be configured to start at power-up either in an OFF or ON state, depending on the configuration of the pin SET_STS.

Table 7. Power-up settings

SET_STS	Mode
GND	OFF @ power-up
VCC	ON @ power-up

If the device is configured ON at power-up (SET_STS pin is connected to V_{CC}), when the supply bus reaches the turn-on threshold, the device is ready to drive the power MOSFET. It is not necessary to receive the ON command by the telecommand interface to enable the device.

If the device is configured OFF at power-up (SET_STS pin is connected to GND), when the supply bus reaches the turn-ON threshold, the device waits for the ON command on the telecommand interface to start to switch on.

A UVLO circuit protects the device from an incorrect bias condition. The setting of the disconnection and reconnection thresholds (turn-OFF and turn-ON) is performed by means of the R_H-R_1-R_2 external resistor divider connected between V_{CC} and the main bus ground (MGND).

The connection point between R_1 and R_2 is tied to the ULVO pin Figure 3. Typical application circuit.

Hysteresis is implemented in order to avoid undesired oscillations caused by bus voltage transients. The hysteresis value can be set through the connection of the resistor R_H between V_{CC} and the HYS pin (Figure 3. Typical application circuit).

R_1, R_2 and R_H can be chosen using the following equations:

$$V_{ON} = 2.5 \times \frac{R_1 + R_2}{R_1} \quad (1)$$

$$V_{OFF} = 2.5 \times \frac{R_1 + R_2 + R_H}{R_1 + R_H} \quad (2)$$

$$V_{HYS} = V_{ON} - V_{OFF} \quad (3)$$

Where:

- V_{ON} is the undervoltage lockout turn-on threshold
- V_{OFF} is the undervoltage lockout turn-off threshold
- V_{HYS} is the undervoltage lockout hysteresis

Please, note that Equation 1 for V_{ON}, R_H is greater than 160 Ω. In fact, the hysteresis is realized by means an internal MOS that acts as a switch by shorting the resistor R_H (connected between pins HYS and V_{CC}) up to V_{CC}, once the turn-on threshold V_{ON} has been exceeded. Indeed, being a not ideal switch, its R_{DS_ON} is about 160 Ω and, as long as V_{ON} is not reached, this R_{DS_ON} acts in parallel to R_H. Therefore, in the Equation 1, the numerator should have a third addendum equivalent to (R_H || R_{DS_ON}) = R_H || 160 Ω. If R_H is one order of magnitude higher than 160 Ω at least, this contribution can be considered negligible and therefore the Equation 1 is still valid.

An internal masking time is implemented in order to ignore bus undervoltage events whose duration is lower than 50 µs. This allows preventing the device from turning off in case of glitches or transient noise occurring on the main supply bus. If a masking time value higher than 50 µs is needed, it is possible to connect an external capacitor between the main supply bus and pin UVLO.

Oncea UVLO event is triggered and recovered, the device restarts according to the configuration defined by the SET_STS pin.

7.2 Modes of operation

When an overcurrent event occurs, the device detects such a condition and starts a trip-off timer. The device drives the external MOSFET in order to limit the current across the load (current limitation mode) and if the overcurrent condition lasts more than the trip-off time T_{ON}, at the end of T_{ON} period the external MOSFET is turned OFF. Instead, if the overcurrent event persists for an interval shorter than T_{ON}, the device limits the current for the duration of the fault and recovers as soon as the overcurrent condition disappears (that is, the MOSFET is driven again to its low-ohmic status with the channel well-saturated).

The trip-off time T_{ON} can be set through an external capacitor C_{ON} connected between the pins T_{ON} and GND, as shown in the application diagram (Figure 3. Typical application circuit). The C_{ON} capacitoris charged with a constant current I_{REF} whose value is externally set by a proper resistor R_{IR} connected between the pin I_REF and GND, so that the trip-off T_{ON} time value is defined by the following equation.

$$T_{ON} = C_{ON} \times R_{IR} \quad (4)$$

The C_{ON} capacitor charging phase starts as soon as the overcurrent event is detected.

At the end of a current limitation period (either the T_{ON} timehas elapsed and consequently the MOSFET is switched OFF or the overcurrent event has disappeared), the discharging phase of the C_{ON} capacitor starts with a constant current whose value is 20 times smaller than the value of the charging phase. With this high charge/discharge ratio, if the overcurrent event occurs frequently and each time for a period lower than the pre-set trip-off time T_{ON}, the MOSFET turning-off is guaranteed (after a number of overcurrent events). In this way a sort of timing memory of successive and closer overcurrent events whose single duration is shorter than the trip-off time T_{ON} is performed, thus avoiding dangerous thermal stress to the MOSFET (hiccup mode).

The procedure used to recover from an overcurrent event can be latched or re-triggerable and depends on the way the T_{OFF} pin is connected.

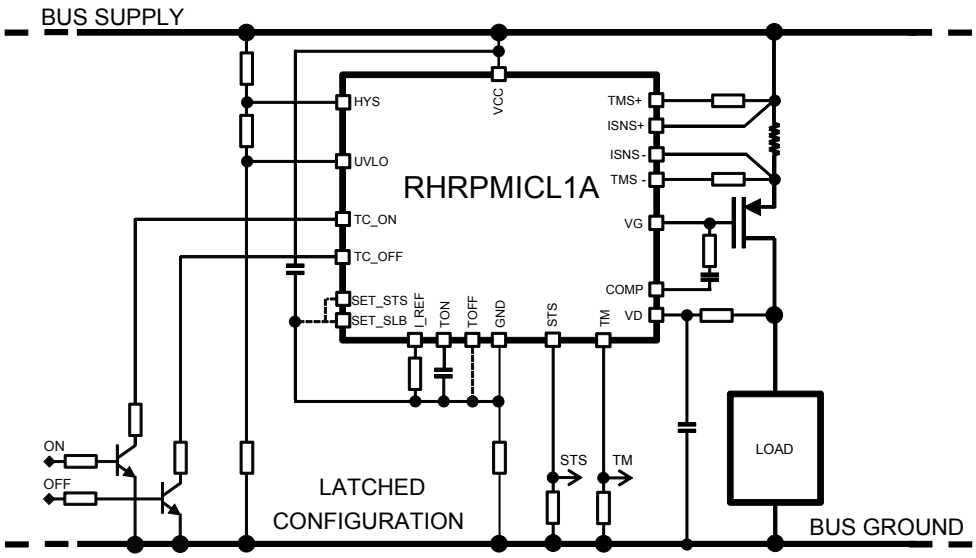
Table 8. T_{OFF} pin settings

T_{OFF}	Mode
GND	Latched
C_{OFF}	Re-triggerable

7.2.1 Latched mode

The device is configured as a latched current limiter (see figure below) when the T_{OFF} pin is shorted directly to GND. In this mode, if the duration of the overcurrent event is greater than the trip-off time, the external MOSFET is latched off and remains off until a reset is given through either the telecommand interface or a UVLO activation/deactivation cycle. When the device is configured as a latched current limiter, the use of the telecommand interface is required. Moreover, if such a configuration mode is set, it is possible to select the device startup mode between latched OFF (the device is OFF at power-up) and latched ON (the device is ON at power-up) using the SET_STS pin. The figure below refers to latched OFF startup mode selection (pin SET_STS shorted to GND), while in the latched ON startup mode the pin SET_STS must be shorted up to V_{CC}.

Figure 4. Typical application diagram with the RHRPMICL1A configured as latched current limiter, latched-OFF at start-up



Note: The resistors R_{GND}, R_{STS} and R_{TM} are critical for the safety of the application. Please refer to Section 8 Application guidelines.

7.2.2 Re-triggerable mode

The device is configured as a re-triggerable current limiter (see Figure 5. Typical application diagram with the RHRPMICL1A configured as re-triggerable current limiter) when an external capacitor C_{OFF} is connected between the T_{OFF} pin and GND. In re-triggerable mode, if the duration of the overcurrent is greater than the trip-off time T_{ON}, the external MOSFET is switched off (as when the latched mode is selected) but the MOSFET stays off for the recovery time T_{OFF}. When the T_{OFF} time elapses, the device tries to restart autonomously turning on again the MOSFET and, if the overcurrent condition has been removed, the system is able to recover its normal condition.

The trip-off time T_{ON}, as well as the recovery time T_{OFF}, can be externally set through the external capacitors C_{ON} and C_{OFF} respectively connected between the pins T_{ON} / T_{OFF} and GND, as shown in the application diagram with the RHRPMICL1A configured as a re-triggerable current limiter (Figure 5. Typical application diagram with the RHRPMICL1A configured as re-triggerable current limiter). The capacitor C_{OFF} is charged with a constant current whose value is a fraction (1/20) of I_{REF} (externally set by the resistor R_{IR} connected between the I_REF pin and GND). The C_{OFF} charging phase of capacitor C_{OFF} starts as soon as the T_{ON} time has elapsed, therefore the T_{OFF} time is equal to the charging time of capacitor C_{OFF} defined by:

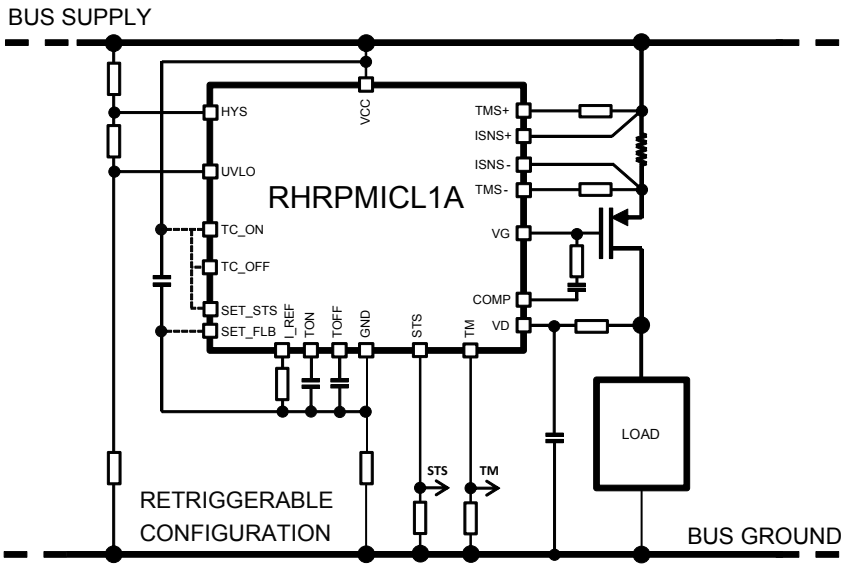
$$T_{OFF} = 20 \times R_{IR} \times C_{OFF} \quad (5)$$

For safety reasons the capacitor C_{OFF} is quickly discharged. T_{OFF} is generated not only after a current limitation event whose duration is greater than the T_{ON} time, but also after any event that turns off the device.

When the device is configured as a re-triggerable current limiter, the following settings are recommended:

- to select the option ON at power-up, connecting the SET_STS pin to V_{CC}
- to disable the telecommand interface, connecting the TC_ON and TC_OFF pins to V_{CC}

Figure 5. Typical application diagram with the RHRPMICL1A configured as re-triggerable current limiter



Note: The resistors R_{GND}, R_{STS} and R_{TM} are critical for the safety of the application. Please refer to Section 8 Application guidelines.

7.2.3 Foldback mode

The device can be configured as a foldback current limiter through the configuration pin SET_FLB (see Figure 6. Typical application diagram with the RHRPMICL1A configured as foldback current limiter).

Table 9. Foldback mode setting

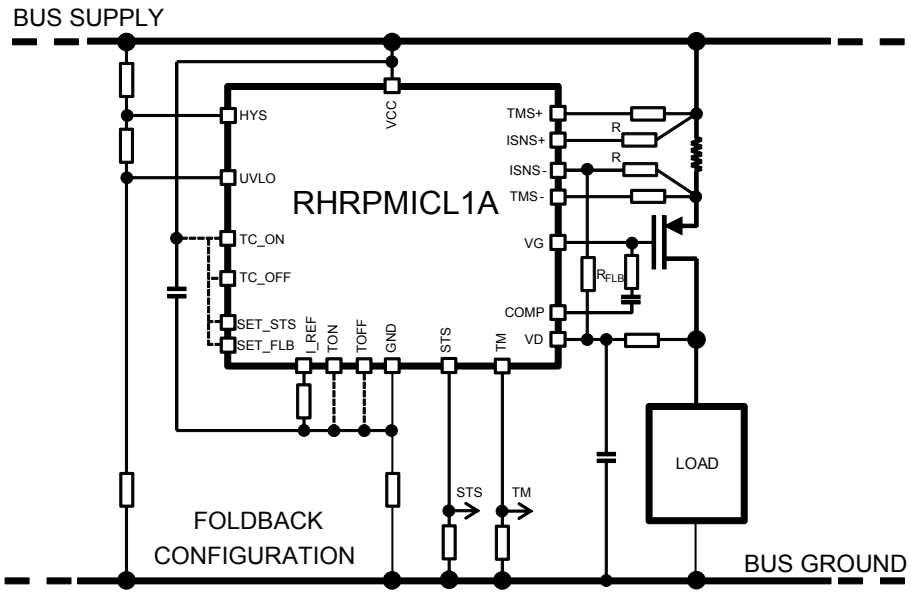
SET_FLB	Mode
GND	Foldback mode disabled
V_{CC}	Foldback mode enabled

A foldback current limiter is a special device that never turns off, otherwise the application could be compromised. When an overcurrent event is detected, the device implements the current limitation feature whose value is dependent on the output voltage, reaching a small and safe value even if a short-circuit on the load occurs and remains. If the foldback mode is selected, it is recommended:

- to select the option ON at power-up, connecting the SET_STS pin to V_{CC}
- to disable the trip-off functionality, connecting the T_{ON} and T_{OFF} pins to GND
- to disable the telecommand interface, connecting the TC_ON and TC_OFF pins to V_{CC}.

When configured as a foldback current limiter, additional resistors have to be connected between the pins VD and ISNS- and between each node of the RSENSE resistor and pins ISNS- and ISNS+ (see Figure 6. Typical application diagram with the RHRPMICL1A configured as foldback current limiter).

Figure 6. Typical application diagram with the RHRPMICL1A configured as foldback current limiter



Note: The resistors R_{GND}, R_{STS} and R_{TM} are critical for the safety of the application. Please refer to Section 8 Application guidelines

Table 10. Device configuration truth table

	SET_FLB	SET_STS	TC_ON	TC_OFF	TON	TOFF	Status at power-up
LATCHED OFF	0	0	Telecommand	Telecommand	C_{ON}	GND	OFF@ power-up
LATCHED ON	0	1	Telecommand	Telecommand	C_{ON}	GND	ON@ power-up
RE-TRIGGERABLE	0	1	V_{CC}	V_{CC}	C_{ON}	C_{OFF}	ON@ power-up
FOLDBACK	1	1	V_{CC}	V_{CC}	GND	GND	ON@ power-up

7.3 Current sense/limitation

The voltage drop on the external R_{SENSE} resistor (see Figure 3. Typical application circuit) is continuously monitored by means of the pins ISNS+ and ISNS- and is compared with a fixed 100 mV voltage threshold internally generated. If the voltage drop on R_{SENSE} exceeds 100 mV, it means that the current demand is becoming excessive and the timer starts to count the trip-off time T_{ON} and the device enters the current limitation mode. In such a condition the limitation control loop is enabled in order to force Vg to the proper voltage level, limiting the current to the load. A proper RC compensation network could be connected between the pins Vg and COMP in order to improve the loop stability.

The current limitation threshold can be externally set according to the application requirements by means of a suitable choice of the R_{SENSE} resistor. When configured as either re-triggerable or latched current limiter, it is:

$$I_{LIM} = 100\,mV / R_{SENSE} \tag{6}$$

Where I_{LIM} is the limitation current value.

Vice versa, the R_{SENSE} resistor can be chosen by:

$$R_{SENSE} = 100\,mV / I_{LIM} \tag{7}$$

Instead, if the device is configured as a foldback current limiter (see Figure 6. Typical application diagram with the RHRPMICL1A configured as foldback current limiter), it is:

$$I_{LIM} = \frac{100\,mV - \frac{R}{R_{FLB}}\left(V_{CC} - V_D\right)}{R_{SENSE}} \tag{8}$$

7.3.1 Repetitive overload events

In case of repetitive overload events, each one having a duration t < T_{ON}, a "memory" of the previous current limitation events is implemented in order to keep the junction temperature of the external MOSFET at safety level. This function, working in both latched and re-triggerable modes, is depicted in the following figures.

Figure 7. Behavior under repetitive overloads

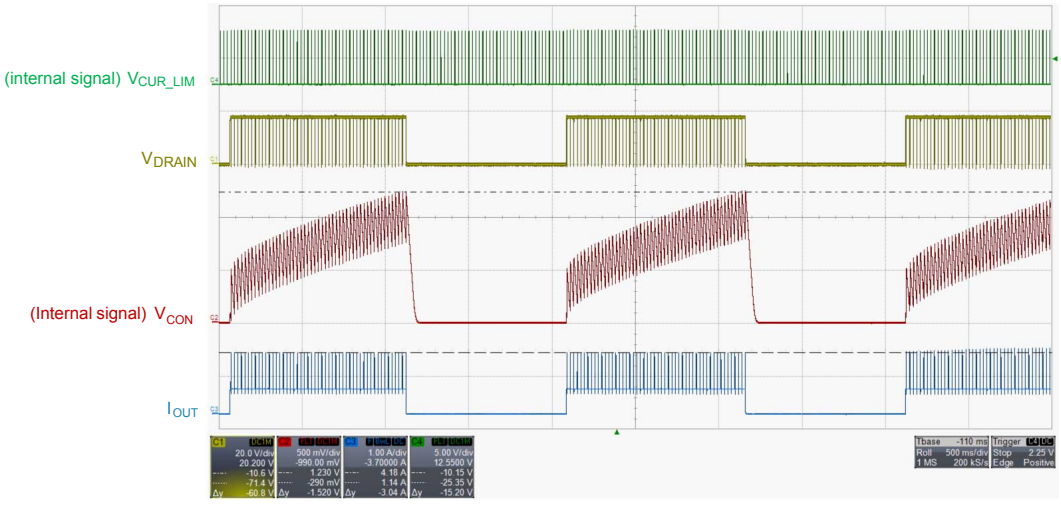
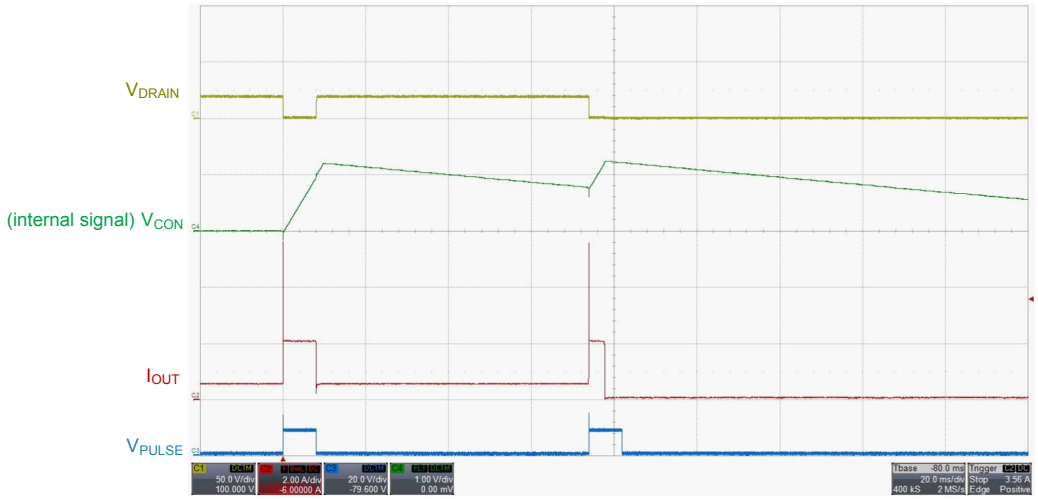


Figure 8. **Behavior under repetitive overloads (magnification)**



7.4 Gate driving

The driver circuit is designed to drive an external P-channel power MOSFET (connected in high-side configuration) providing on the pin Vg a voltage signal in the range V_{CC} down to (V_{CC} - 12 V).

When the device works in normal operating mode (which means the device is neither off nor in current limitation mode) the Vg node is pulled down and the gate of the external MOSFET is internally clamped about 12 V below the supply voltage V_{CC} making the channel of the MOSFET well-saturated.

- When the MOSFET has to be switched off, Vg is brought up to V_{CC}
- When the MOSFET is in current limitation mode, the level of Vg voltage is defined by the limitation control loop

7.5 Telecommand interface

The RHRPMICL1A can be enabled or disabled by means of two digital signals through the pin TC_ON and TC_OFF. If the voltage on the pin TC_ON is forced low for a typical pulse time of 100 µs, the device is switched ON. In the same way, a low voltage forced on the pin TC_OFF for a typical pulse time of 100 µs switches OFF the device. In order to have a more robust implementation, unwanted ON/OFF pulses having a short duration (lower than 10 µs) are ignored in order to have a sort of noise immunity of the telecommand system.

In case of contemporaneous application of the ON and OFF commands, the OFF command has the priority which means that in case of a failure of the telecommand interface resulting in a permanent ON state, it is possible always to switch off the device by sending an OFF command.

7.6 Floating ground configuration

As mentioned in Section 7.1 Supply voltage, startup and undervoltage lockout, a Zener diode chain is embedded in order to clamp the voltage level between V_{CC} and GND at about V_Z = 15 V (typ. 14.8 V).

If the operating supply bus is $V_{CC} < V_Z$, the Zener clamp is OFF and the total current consumption of the device is about 1.5 mA @ V_{CC} ~ 14.6 V, i.e. near the ON threshold for the clamp.

If the operating supply bus is $V_{CC} > V_Z$, the Zener clamp is ON and the current consumption of this Zener diode chain is added to the previous current consumption of the device.

In order to benefit from the floating ground feature and therefore to improve the device performance in terms of power line rejection, it is better to operate the device with the Zener clamp ON.

A good trade-off is to establish a total current consumption of 2 mA, therefore the floating ground resistor is sized according to the following resistor.

$$R_{GND} = \frac{V_{CC} - V_Z}{I_{CC}} \quad (9)$$

V_{CC} = system operating supply voltage

V_Z = V_{CC} vs. GND internal clamp voltage

I_{CC} = supply current whose recommend value is 2 mA

The implementation of the floating ground feature is mandatory in satellite applications in order to avoid the collapse of the bus supply vs. the bus ground, compromising the application as a result of a possible short of the supply line vs. ground inside the device.

In case of a short-circuit inside the device, the external R_{GND} resistor (Figure 3. Typical application circuit) connected between the GND pin and the main bus ground must sustain the overall voltage between the bus supply and ground. The power dissipation of this resistor has to be sized properly in order to be able to dissipate the power according to the steady-state value of the supply bus. Additional single point failure protection recommendations can be found in Section 8 Application guidelines.

7.7 Status telemetry

The status telemetry circuit gives information about the device status. This information can be retrieved by monitoring the STS output pin.

When an ON command is received through the TC_ON pin or the device has turned ON from an undervoltage event to a normal operation mode, the STS output is forced high

The STS output is forced low when one of the following events occurs:

- the device turns OFF the external MOSFET as a consequence of a current limitation event
- an OFF command is received through the TC_OFF pin to turn off the device
- an OFF command is received through the TC_OFF pin to reset a latch condition

Table 11. Telemetry digital status pin

STS	Mode
Low	Device is in OFF state
High	Deviceis in ON state

The STS is an open drain pin able to source a 100 µA fixed current, so that an external resistor R_{STS} (Figure 3. Typical application circuit) has to be connected between the pin STS and the main bus ground. The R_{STS} value has to be chosen depending on the desired high voltage level (V_{H_STS}) from the following equation.

$$R_{STS} = V_{H\_STS} / 100\ \mu A \quad (10)$$

7.8 Analog current sense telemetry

The telemetry circuit gives information about the current across the load. This circuit provides on the pin TM a source current whose value is proportional to the current flowing from the bus supply line to the load. The voltage drop on the external resistor R_{TM} (Figure 3. Typical application circuit), connected between the pin TM and the main bus ground, is proportional to the current load, thus performing a current/voltage conversion.

This function is implemented by sensing the voltage drop on the external R_{SENSE} resistor through the R_{TMS} resistors connected to the pins TMS+ and TMS-. As it is:

$$I_{RTM} = I_{RSENSE} \times \frac{R_{SENSE}}{R_{TMS}} \quad (11)$$

Subsequently:

$$R_{TM} = \frac{V_{TM}}{I_{RTM}} = \frac{V_{TM}}{I_{SENSE}} \times \frac{R_{TMS}}{R_{SENSE}} \quad (12)$$

Where V_{TM} is the voltage drop on the R_{TM} external resistor that has to be monitored to have information on the corresponding I_{RSENSE} current.

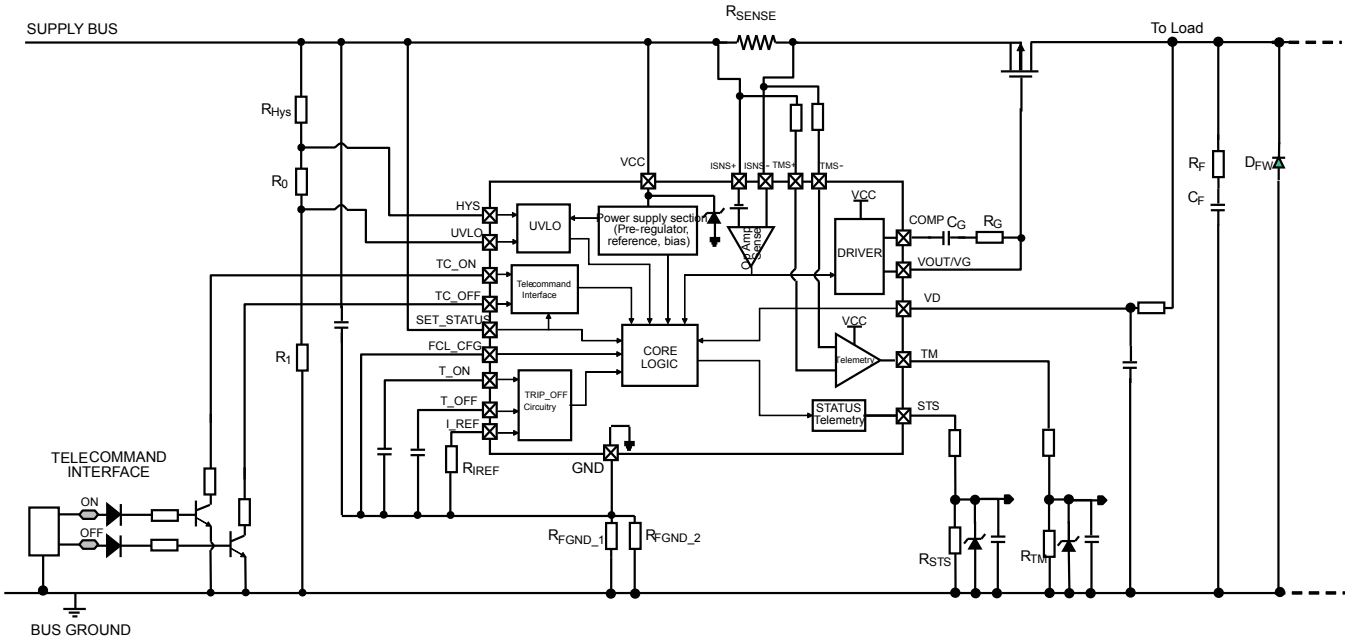
The resistors connected to TMS+ and TMS- should have high accuracy in order to minimize the offset on V_{TM} generated by not matched values.

8 Application guidelines

When a floating ground configuration is being operated, it is recommended to protect the application from single point failures of the resistor R_{FGND} connected between GND and BUS GROUND and the telemetry resistors (R_{STS} and R_{TM}). In fact, in case of failure of these resistors, damage may occur to the device itself and to the other devices connected to the same bus.

The figure below shows a typical implementation of the protection described above.

Figure 9. Recommended typical application schematic with single failure protection



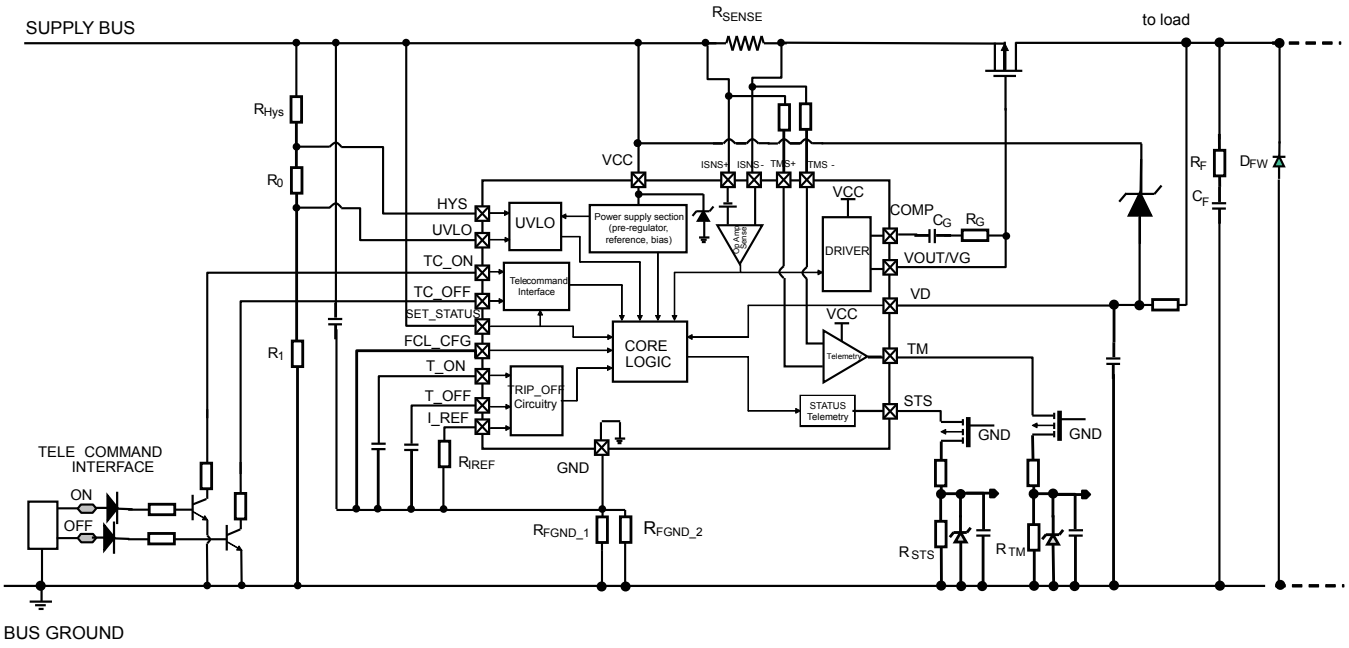
8.1 Guidelines for operation at high voltage

Even if the device has been tested and characterized in radiation up to V_{CC} = 52 V, from the electrical point of view, it is able to withstand up to ~ 90 V between BUS_SUPPLY and BUS GROUND.

Nevertheless, it is possible, by adding some external components, to work with a bus supply higher than 90 V, as described in the following figure.

Under radiation the following application guidelines are recommended for bus supply higher than 52 V.

Figure 10. Schematic for operation at bus voltages higher than 90 V



The resistors in series to the pull-down transistors of the telecommand circuitry (telecommand interface) are sized in order to guarantee that pins TC_ON and TC_OFF never go to ~ - 75 V under GND, i.e. the value of the substrate reference of the device.

The telemetry pins (TM and STS) are connected to BUS GROUND through the external HV P-CH transistors used in cascode configuration, with gate connected on GND.

The pin V_D is suitably clamped (for example through a Zener diode between V_{CC} and V_D) in order to avoid that this pin goes to ~ - 75 V under GND when the device is in the OFF state or in case of a short-circuit.

9 Layout guidelines

The RHRPMICL1A simultaneously handles fast switching and medium voltage, which implies specific attention to the layout. Furthermore, proper layout allows mitigating a heavy ion effect, in particular SET. We recommend that the user refers as much as possible to the layout guidelines of the EVAL-RHRICL1xV1 demonstration board.

The first priority when components, are placed has to be given to the power section (current path from input, through current sense resistor and high-side switch, toward output), minimizing the length of each connection and loop as short as possible.

Also, the path of the gate driver signal (driving ON/OFF the high-side switch) must present the lowest resistance as possible. A power resistor might be required in series to this path to protect the integrated gate driver.

To minimize noise and voltage spikes (also EMI and losses) power connections must be a part of a power plane and implemented using wide and thick conductor traces. The loop must be minimized. The inductance effect and, consequently, leading to ringing of the tracks can be minimized by making it as short as possible. The number of vias must be minimized to reduce the related parasitic effect.

A capacitor on V_{CC}, as well as the capacitors connected to the digital pins, should be placed as close as possible to the IC to reduce possible loop and parasitic inductance.

Small signal components and connections to critical nodes (e.g. TC_ON/OFF, ISNS+ and ISNS-) of the application are also important. In fact, the symmetry of the path may impact the sampled value.

To improve heat dissipation, place a copper area under the IC. This copper area may be connected with other layers (if available) through vias to improve the thermal conductivity. The combination of a copper pad, copper plane and vias under the driver allows the device to reach its best thermal performance.

It is important to ensure that the power devices, including the IC, have a thermal path compatible with the power dissipated. It is advisable to mount both the IC and the high-side switch on dedicated heatsinks (for example, the device should be soldered on the copper area of the PCB, which is in strict thermal contact to an aluminium frame) gluing each part to the frame (without using any screws for the power MOSFET).

The material used to glue could be the resin ME7158 (space approved resin). Moreover, two small FR4 spacers could be added in order to ensure the electrical isolation of the package of the device from the frame.

Finally, for reliability reasons it is advisable to use more than one resistor (series connected) between the device and the main bus ground whose total value is the one obtained by application design considerations.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 Flat-20 package information

Figure 11. Flat-20 package outline

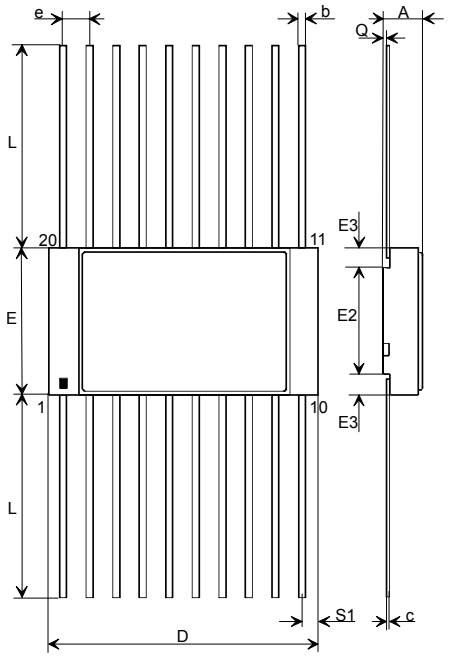


Table 12. Flat-20 ceramic hermetic flat package mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.91		2.21	0.075		0.087
b	0.38		0.48	0.015		0.019
c	0.076		0.152	0.003		0.006
D	12.83		13.08	0.505		0.515
E	6.99		7.24	0.275		0.285
E2	5.05	5.21	5.36	0.199	0.205	0.211
E3		0.95			0.037	
e	1.14		1.40	0.045		0.055
L	6.35		9.39	0.250		0.370
Q	0.25			0.010		
S1		0.55			0.021	

11 Ordering information

Table 13. Order codes

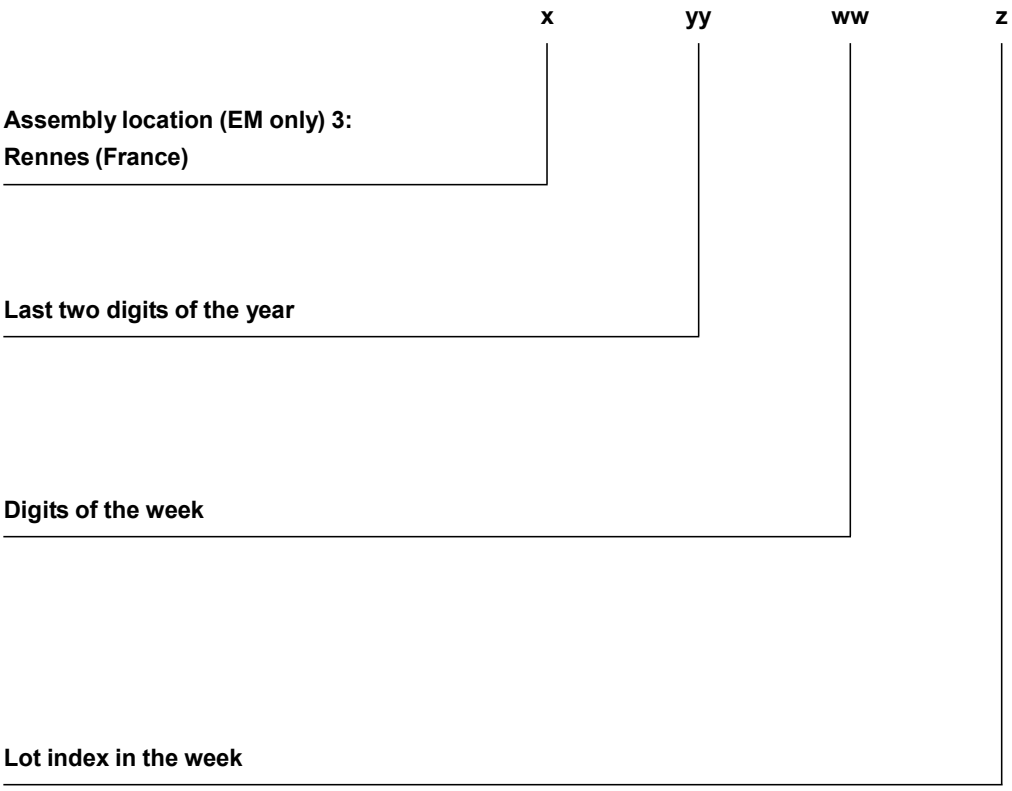
Order code [1]	Quality level	SMD	Package	Lead finish	Marking [2]	Mass	Packing
RH-PMICL1AKX	Evaluation model		Flat-20	Gold	RH-PMICL1AKX	0.7 g	Strip pack
RH-PMICL1AK1	Engineering model				RH-PMICL1AK1		
RHRPMICL1AK01V	QML-V	5962-17211			5962R1721101VXC		
RHRPMICL1AK02V				Solder dip	5962R1721101VXA		
RHRPMICL1AD2V			Die version	-	-	-	-

1. *Contact ST sales office for information about specific conditions for product in die form and other quality levels*
2. *Specific marking only. The full marking includes in addition:*
   - *For the Engineering Models: ST logo, date code; country of origin (FR)*
   - *For flight parts: ST logo, date code, country of origin (FR), ESA logo, serial number of the part within the assembly lot*

12 Shipping details

12.1 Date code

The date code is structured as described below:
EM xyywwz
QML-V Flight yywwz
Where:



12.2 Documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Note: Please, contact ST for details on the documentation of other quality levels.

Table 14. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including : Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to the TN1181 on engineering models ST Rennes assembly lot ID
QML-V Flight	Certificate of conformance including Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Pre-cap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 15. **Document revision history**

Date	Version	Changes
12-Jul-2018	1	Initial release.
26-Mar-2019	2	Updated: - Description pin 16 in Table 1. Pin description. - TOFF Min. and Max. values in Table 4. Electrical characteristics. Added sentence in Section 7.8 Analog current sense telemetry. Minor text changes in Section 8 Application guidelines.
01-Oct-2019	3	Updated Features, Table 4. Electrical characteristics, Table 5. TID test results and Table 13. Order codes. Updated Figure 9. Recommended typical application schematic with single failure protection and Figure 10. Schematic for operation at bus voltages higher than 90 V.

Contents

List of tables

List of figures

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.