bq25898C I^{2}C 控制单节 3A 充电器实现高输入电压采用紧凑型 DSBGA 封装

1 特性

- 作为从充电器运行，在双充电器操作下提供快速充电
- 配置简单，物料清单 (BOM) 极低
- 高效率 3A、1.5MHz 开关模式降压充电器
  - 充电效率高达 92%（3A 充电电流下）和 94%（2A 充电电流下）
  - 针对高电压输入 (9V/12V) 进行了优化
  - 低功耗 PFM 模式，适用于轻负载操作
- 单个输入，支持 USB 输入和可调高压适配器
  - 支持 3.9V 至 14V 输入电压范围
  - 输入电流限制（100mA 至 3.25A，分辨率为 50mA），支持 USB2.0、USB3.0 标准和高压适配器
  - 宽输入动态电源管理 (DPM) 范围
- 借助 5mΩ 电池放电金属氧化物半导体场效应晶体管 (MOSFET) 实现最高电池放电效率，放电电流高达 9A电池 MOSFET
- 默认禁用充电
- 集成 ADC，用于系统监视（输入、系统和电池电压、温度和充电电流）
- 灵活的自主和 I^{2}C 模式，可实现最优系统性能
- 远程电池感测
- 高集成度，包括所有 MOSFET、电流感测和环路补偿
- 高精度
  - ±0.5% 充电电压调节
  - ±5% 充电电流调节
  - ±7.5% 输入电流调节
- 安全
  - 热调节和热关断
  - 输入 UVLO/过压保护
  - 电池 OVP
  - 安全定时器

2 应用

- 智能手机
- 平板电脑
- 便携式网络设备

3 说明

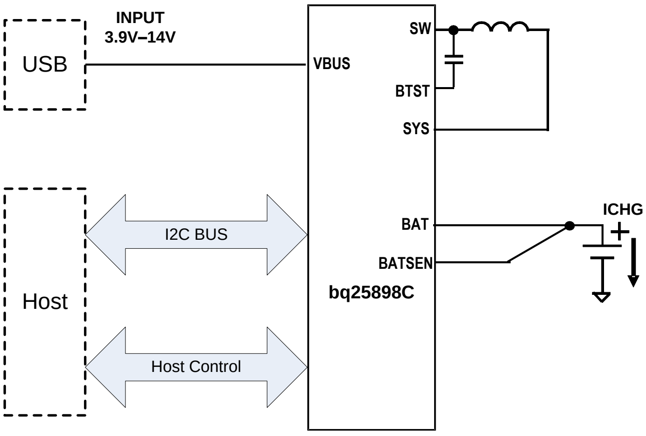
bq25898C 是一款适用于单节锂离子电池和锂聚合物电池的高度集成型开关模式电池充电管理和系统电源路径管理器件。该器件支持高输入电压充电。其低阻抗电源路径对开关模式运行效率进行了优化、缩短了电池充电时间并延长了放电阶段的电池使用寿命。具有充电和系统设置的 I2C 串行接口使得该器件成为真正具有灵活性的解决方案。bq25898C 采用 2.8mm x 2.5mm 42 焊球 DSBGA 封装。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
bq25898C	DSBGA (42)	2.80mm x 2.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



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• 已更改 集成 ADC，用于系统监视特性	1
• 已更改 “充电已禁用”更改为“快速充电和预充电均已禁用”	3
• 已更改 PG 已更改为 $\overline{\text{PG}}$（在“说明”中）	3
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5 说明 （续）

bq25898C 是一款适用于单节锂离子电池和锂聚合物电池的高度集成型 3A 开关模式电池充电管理器件。作为一款经济高效的微型器件，它还可以配置为从充电器，以在双充电器应用中提供快速 充电的输出电流传感电阻器和运算放大器而得以实现。

该器件 支持 高输入电压快速充电，适用于各类智能手机、平板电脑和便携式设备。其低阻抗电源路径对开关模式运行效率进行了优化、缩短了电池充电时间并延长了放电阶段的电池使用寿命。该解决方案高度集成输入反向阻断场效应晶体管 (FET)（RBFET，Q1）、高侧开关 FET（HSFET，Q2）、低侧开关 FET（LSFET，Q3）以及充电电流感测电路。它还集成了自举二极管以进行高侧栅极驱动和电池监视，从而简化系统设计。具有充电和系统设置的 I2C 串行接口使得此器件成为一个真正地灵活解决方案。

该器件支持多种输入源，包括标准 USB 主机端口、USB 充电端口以及兼容 USB 的可调节高电压适配器。为了设定默认输入电流限值，该器件获取系统检测电路（如 USB PHY 器件）中的结果。该器件符合 USB 2.0 和 USB 3.0 电源规范，具有输入电流和电压调节功能。

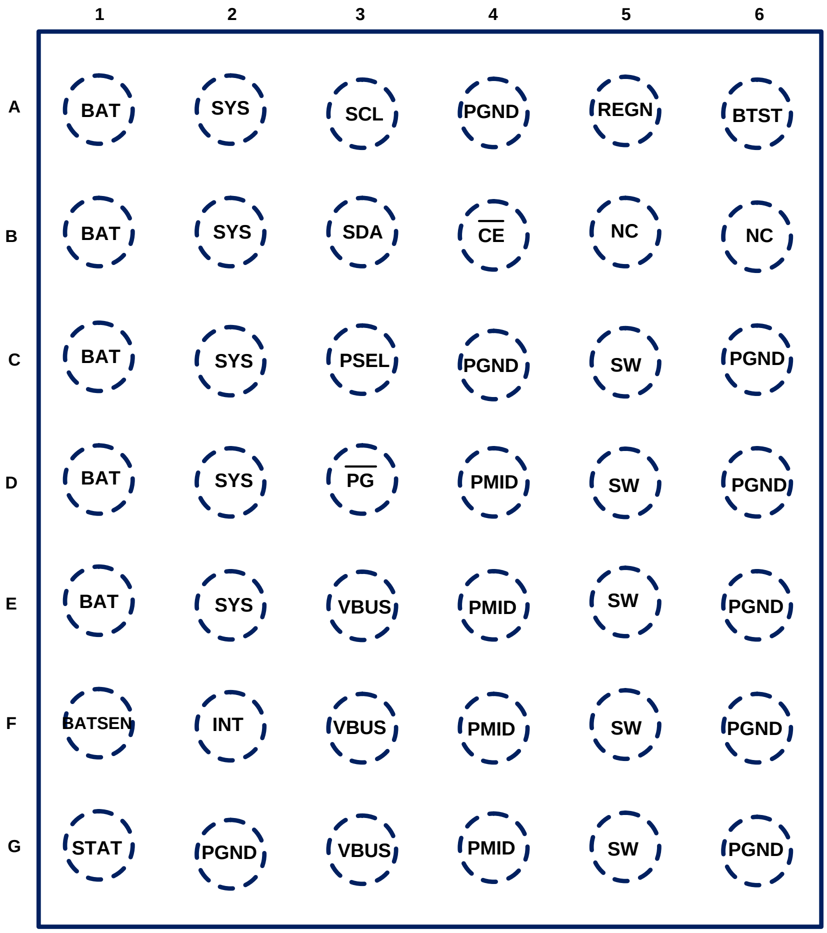
默认充电电流设置为 0mA（快速充电和预充电均已禁用）。启用充电后，器件可在软件控制下启动并完成一个充电周期。

此充电器提供针对电池充电和系统运行的多种安全 特性 ，其中包括充电安全定时器和过压/过流保护。当结温超过 120°C（可设定）时，热调节减少充电电流。STAT 输出报告充电状态和任何故障条件。$\overline{\text{PG}}$ 输出指示电源是否正常。当故障发生时，INT 会立即通知主机。

该器件采用 2.80mm x 2.50mm 42 焊球 DSBGA 封装。

6 Pin Configuration and Functions

YFF Package
42-Pin DSBGA
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VBUS	E3-G3	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-uF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
PSEL	C3	DI	Power source selection input. High indicates a USB host source and Low indicates an adapter source.
$\overline{\text{PG}}$	D3	DO	Open drain active low power good indicator. Connect to the pull up rail via 10-kohm resistor. LOW indicates a good input source if the input voltage is within VVBUS_OP, above SLEEP mode threshold (VSLEEPZ), and current limit is above IBATSRC (30mA).
STAT	G1	DO	Open-drain interrupt output. Connect to the INT to a logic rail via 10-kohm resistor. The INT pin sends active low, 256-us pulse to host to report charger device status and fault.
SCL	A3	DI	I2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	B3	DIO	I2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INT	F2	DO	Open-drain Interrupt Output. Connect the INT to a logic rail via 10-kΩ resistor. The INT pin sends active low, 256-µs pulse to host to report charger device status and fault.
$\overline{\text{CE}}$	B4	DI	Active low charge enable pin. Battery charging is enabled when CHG_CONFIG = 1 and CE pin = Low. CE pin must be pulled High or Low.
NC	B5-B6		No connect. Float the pin.
BAT	A1-E1	P	Battery connection point to the positive terminal of the battery pack. The internal current sensing circuitry is connected between SYS and BAT. Connect a 10uF closely to the BAT pin.

(1) DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

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Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SYS	A2-E2	P	Converter output connection point. The internal current sensing circuitry is connected between SYS and BAT. Connect a 20uF closely to the SYS pin.
PGND	C4,C6-G6,A4,G2	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	C5-G5	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047μF bootstrap capacitor from SW to BTST.
BTST	A6	P	PWM high side driver positive supply. Internally, the BTST is connected to the cathode of the boost-strap diode. Connect the 0.047μF bootstrap capacitor from SW to BTST.
REGN	A5	P	PWM low side driver positive supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7μF (10 V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC.
PMID	D4-G4	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Given the total input capacitance, put 1μF on VBUS to PGND, and the rest capacitance on PMID to PGND.
BATSEN	F1	AI	Remote battery sense input. The typical pin resistance is 800 kΩ. Connect as close to battery as possible.

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	VALUE
Voltage range (with respect to GND)	VBUS (converter not switching)	–2	22	V
	PMID (converter not switching)	–0.3	22	V
	STAT	–0.3	20	V
	$\overline{\text{PG}}$	–0.3	7	V
	PSEL	–0.3	7	V
	BTST	–0.3	20	V
	SW	–3	16	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SDA, SCL, INT, REGN, $\overline{\text{CE}}$	–0.3	7	V
	BTST TO SW	–0.3	7	V
	PGND to GND	–0.3	0.3	V
	BATSEN	–0.3	7	V
Output sink current	INT, STAT		6	mA
	$\overline{\text{PG}}$		6	mA
Junction temperature		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	3.9	14[1]	V
I_{IN}	Input current (VBUS)		3.25	A
I_{SYS}	Output current (SW)		3	A
V_{BAT}	Battery voltage		4.608	V
I_{BAT}	Fast charging current		3	A
	Discharging current with internal MOSFET		Up to 6 (continuos)	A
			9 (peak) (Up to 1 sec duration)	A
T_A	Operating free-air temperature range	–40	85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

7.4 Thermal Information

THERMAL METRIC[1]		bq25898C	UNIT
		YFF (DSBGA)	
		42-BALL	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.5	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.2	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.2 V, $V_{(VBUS)} < V_{(UVLO)}$, leakage between BAT and VBUS			5	µA
		High-Z Mode, No VBUS, BATFET Disabled (REG09[5] = 1), Battery Monitor Disabled, T_J < 85°C		12	23	µA
		High-Z Mode, No VBUS, BATFET Enabled (REG09[5] = 0), Battery Monitor Disabled, T_J < 85°C		32	60	µA
$I_{(VBUS\_HIZ)}$	Input supply current (VBUS) in buck mode when High-Z mode is enabled	$V_{(VBUS)}$= 5 V, High-Z Mode, No Battery, Battery Monitor Disabled		15	35	µA
		$V_{(VBUS)}$= 12 V, High-Z Mode, No Battery, Battery Monitor Disabled		25	50	µA
$I_{(VBUS)}$	Input supply current (V_{BUS}) in buck mode	$V_{BUS} > V_{(UVLO)}$, $V_{BUS} > V_{BAT}$, Converter not switching		1.5	3	mA
		$V_{BUS} > V_{(UVLO)}$, $V_{BUS} > V_{BAT}$, Converter switching, V_{BAT} = 3.2V, I_{SYS} = 0A		3		mA
		$V_{BUS} > V_{(UVLO)}$, $V_{BUS} > V_{BAT}$, Converter switching, V_{BAT} = 3.8 V, I_{SYS} = 0 A		3		mA
VBUS/BAT POWER UP						
$V_{(VBUS\_OP)}$	VBUS operating range		3.9		14	V
$V_{(VBUS\_UVLOZ)}$	VBUS for active I^2C, no battery		3.6			V
$V_{(SLEEP)}$	Sleep mode falling threshold		25	65	120	mV
$V_{(SLEEPZ)}$	Sleep mode rising threshold		130	250	370	mV
$V_{(ACOV)}$	VBUS over-voltage rising threshold		13.9		14.6	V
	VBUS over-voltage falling threshold		13.3		13.9	V
t_{ACOV_RISING}	ACOV rising deglitch	V_{VBUS} rising		1		µs

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Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ACOV\_FALLING}$	ACOV falling deglitch	V_{VBUS} falling		1		ms
$V_{BAT(UVLOZ)}$	Battery for active I^2C, no VBUS		2.3			V
$V_{BAT(DPL)}$	Battery depletion falling threshold		2.15		2.5	V
$V_{BAT(DPLZ)}$	Battery depletion rising threshold		2.35		2.7	V
$V_{(VBUSMIN)}$	Bad adapter detection threshold			3.8		V
$I_{(BADSRC)}$	Bad adapter detection current source			30		mA
POWER-PATH MANAGEMENT						
V_{SYS}	Typical system regulation voltage	$I_{(SYS)}$ = 0 A, $V_{BAT} > V_{SYS(MIN)}$, BATFET Disabled (REG09[5]=1)		V_{BAT}+ 50 mV		V
		Isys = 0 A, $V_{BAT} < V_{SYS(MIN)}$, BATFET Disabled (REG09[5]=1)		$V_{SYS(MIN)}$ + 250 mV		V
$V_{SYS(MIN)}$	Minimum DC system voltage output	$V_{BAT} < V_{SYS(MIN)}$, SYS_MIN = 3.5 V (REG03[3:1] = 101), I_{SYS}= 0 A	3.60	3.75		V
$V_{SYS(MAX)}$	Maximum DC system voltage output	V_{BAT} = 4.35 V, SYS_MIN = 3.5 V (REG03[3:1] = 101), I_{SYS}= 0 A		4.40	4.42	V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET(RBFET) on-resistance between VBUS and PMID	T_J = -40°C - 85°C		28	40	mΩ
		T_J = -40°C - 125°C		28	47	mΩ
$R_{ON(HSFET)}$	Top switching MOSFET (HSFET) on-resistance between PMID and SW	T_J = -40°C - 85°C		24	33	mΩ
		T_J = -40°C - 125°C		24	40	mΩ
$R_{ON(LSFET)}$	Bottom switching MOSFET (LSFET) on-resistance between SW and GND	T_J = -40°C - 85°C		12	18	mΩ
		T_J = -40°C - 125°C		12	21	mΩ
$V_{(FWD)}$	BATFET forward voltage in supplement mode	BAT discharge current 10 mA		30		mV
BATTERY CHARGER						
$V_{BAT(REG\_RANGE)}$	Typical charge voltage range		3.840		4.608	V
$V_{BAT(REG\_STEP)}$	Typical charge voltage step			16		mV
$V_{BAT(REG)}$	Charge voltage resolution accuracy	V_{BAT} = 4.208 V (REG06[7:2] = 010111) or V_{BAT} = 4.352 V (REG06[7:2] = 100000) T_J = -40°C - 85°C	-0.5%		0.5%	
$I_{(CHG\_REG\_RANGE)}$	Typical fast charge current regulation range		0		3008	mA
$I_{(CHG\_REG\_STEP)}$	Typical fast charge current regulation step			64		mA
$I_{(CHG\_REG\_ACC)}$	Fast charge current regulation accuracy	V_{BAT}= 3.1 V or 3.8 V, I_{CHG} = 256 mA T_J = -40°C - 85°C	-20%		20%	
		V_{BAT}= 3.1 V or 3.8 V, I_{CHG} = 1792 mA T_J = -40°C - 85°C	-5%		5%	
$V_{BAT(LOWV)}$	Battery LOWV falling threshold	Fast charge to precharge, BATLOWV (REG06[1]) = 1	2.6	2.8	2.9	V
	Battery LOWV rising threshold	Precharge to fast charge, BATLOWV (REG06[1]) = 1 (Typical 200-mV hysteresis)	2.8	3.0	3.15	V
	Battery LOWV falling threshold	Fast charge to precharge, BATLOWV (REG06[1]) = 0	2.5	2.6	2.7	V
	Battery LOWV rising threshold	Precharge to fast charge, BATLOWV (REG06[1]) = 0 (Typical 200-mV hysteresis)	2.7	2.8	2.9	V
$I_{(PRECHG\_RANGE)}$	Precharge current range		64		1024	mA
$I_{(PRECHG\_STEP)}$	Typical precharge current step			64		mA
$I_{(PRECHG\_ACC)}$	Precharge current accuracy	V_{BAT} = 2.6 V, I_{PRECHG} = 256 mA	–20%		20%	
$I_{(TERM\_RANGE)}$	Termination current range		64		1024	mA
$I_{(TERM\_STEP)}$	Typical termination current step			64		mA
$I_{(TERM\_ACC)}$	Termination current accuracy	I_{TERM} = 256 mA, $I_{CHG} \le$ 1344 mA T_J = -20°C - 85°C	-20%		20%	
		I_{TERM} = 256 mA, $I_{CHG} >$ 1344 mA T_J = -20°C - 85°C	-20%		20%	
$V_{(SHORT)}$	Battery short voltage	VBAT falling		2.0		V
$V_{(SHORT\_HYST)}$	Battery short voltage hysteresis	VBAT rising		200		mV
$I_{(SHORT)}$	Battery short current	VBAT < 2.2 V		110		mA
$V_{(RECHG)}$	Recharge threshold below V_{BATREG}	V_{BAT} falling, VRECHG (REG06[0] = 0) = 0		100		mV
		V_{BAT} falling, VRECHG (REG06[0] = 0) = 1		200		mV

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Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ON(BATFET)}$	SYS-BAT MOSFET (BATFET) on-resistance	T_J = 25°C		5	7	mΩ
		T_J = -40°C - 125°C		5	10	mΩ
R_{BATSEN}	BATSEN input resistance			800		kΩ
INPUT VOLTAGE / CURRENT REGULATION						
$V_{IN(DPM\_RANGE)}$	Typical input voltage regulation range		3.9		15.3	V
$V_{IN(DPM\_STEP)}$	Typical input voltage regulation step			100		mV
$V_{IN(DPM\_ACC)}$	Input voltage regulation accuracy	VINDPM = 4.4 V, 7.8 V, 10.8 V	-3%		3%	
$I_{IN(DPM\_RANGE)}$	Typical input current regulation range		100		3250	mA
$I_{IN(DPM\_STEP)}$	Typical input current regulation step			50		mA
$I_{IN(DPM100\_ACC)}$	Input current 100mA regulation accuracy V_{BAT} = 5V, current pulled from SW	IINLIM (REG00[5:0]) = 100 mA	85	90	100	mA
$I_{IN(DPM\_ACC)}$	Input current regulation accuracy V_{BAT} = 5V, current pulled from SW	USB150, IINLIM (REG00[5:0]) = 150 mA	125	135	150	mA
		USB500, IINLIM (REG00[5:0]) = 500 mA	440	470	500	mA
		USB900, IINLIM (REG00[5:0]) = 900 mA	750	825	900	mA
		Adapter 1.5 A, IINLIM (REG00[5:0]) = 1500 mA	1300	1400	1500	mA
$I_{IN(START)}$	Input current regulation during system start up	V_{SYS} = 2.2 V, IINLIM (REG00[5:0]) ≥ 200 mA			200	mA
BAT OVER-VOLTAGE/CURRENT PROTECTION						
$V_{BAT(OVP)}$	Battery over-voltage threshold	V_{BAT} rising, as percentage of $V_{BAT(REG)}$		104%		
$V_{BAT(OVP\_HYST)}$	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of $V_{BAT(REG)}$		2%		
$I_{BAT(FET\_OCP)}$	System over-current threshold		9			A
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	REG08[1:0] = 11		120		°C
T_{SHUT}	Thermal shutdown rising temperature	Temperature rising		160		°C
$T_{SHUT(HYS)}$	Thermal shutdown hysteresis	Temperature falling		30		°C
PWM						
F_{SW}	PWM switching frequency, and digital clock	Oscillator frequency	1.32		1.68	MHz
D_{MAX}	Maximum PWM duty cycle			97%		
REGN LDO						
$V_{(REGN)}$	REGN LDO output voltage	$V_{(VBUS)}$ = 9 V, $I_{(REGN)}$ = 40 mA	5.6	6	6.4	V
		$V_{(VBUS)}$ = 5 V, $I_{(REGN)}$ = 20 mA	4.7	4.8		V
$I_{(REGN)}$	REGN LDO current limit	$V_{(VBUS)}$ = 9 V, $V_{(REGN)}$ = 3.8 V	50			mA
ANALOG-TO-DIGITAL CONVERTER (ADC)						
RES	Resolution	Rising threshold		7		bits
$V_{BAT(RANGE)}$	Typical battery voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$	2.304		4.848	V
		$V_{(VBUS)} < V_{BAT} + V_{(SLEEP)}$	V_{SYS_MIN}		4.848	V
$V_{(BAT\_RES)}$	Typical battery voltage resolution			20		mV
$V_{(SYS\_RANGE)}$	Typical system voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$	2.304		4.848	V
		$V_{(VBUS)} < V_{BAT} + V_{(SLEEP)}$	V_{SYS_MIN}		4.848	V
$V_{(SYS\_RES)}$	Typical system voltage resolution			20		mV
$V_{(VBUS\_RANGE)}$	Typical V_{VBUS} voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$	2.6		15.3	V
$V_{(VBUS\_RES)}$	Typical V_{VBUS} voltage resolution			100		mV
$I_{BAT(RANGE)}$	Typical battery charge current range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ and $V_{BAT} > V_{BAT(SHORT)}$	0		3.008	A
$I_{BAT(RES)}$	Typical battery charge current resolution			50		mA
LOGIC I/O PIN ($\overline{CE}$, PSEL)						
V_{IH}	Input high threshold level		1.3			V
V_{IL}	Input low threshold level				0.4	V
$I_{IN(BIAS)}$	High level leakage current	Pull-up rail 1.8 V			1	µA
LOGIC I/O PIN (INT, STAT, $\overline{PG}$)						
V_{OL}	Output low threshold level	Sink Current = 5 mA, Sink current			0.4	V
I_{OUT_BIAS}	High level leakage current	Pull-up rail 1.8 V			1	µA
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SCL and SDA	Pull-up rail 1.8 V	1.3			V
V_{IL}	Input low threshold level	Pull-up rail 1.8 V			0.4	V

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Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low threshold level	Sink Current = 5 mA, Sink current			0.4	V
I_{BIAS}	High level leakage current	Pull-up rail 1.8 V			1	µA

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{BADSRC}	Bad adapter detection duration			30		msec
BAT OVER-VOLTAGE PROTECTION						
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		µs
BATTERY CHARGER						
t_{RECHG}	Recharge deglitch time			20		msec
BATTERY MONITOR						
t_{CONV}	Conversion time	CONV_RATE(REG02[6]) = 0		8	1000	msec
I2C INTERFACE						
f_{SCL}	SCL clock frequency				400	KHz
DIGITAL CLOCK and WATCHDOG TIMER						
f_{LPDIG}	Digital low power clock	REGN LDO disabled	18	30	45	KHz
f_{DIG}	Digital clock	REGN LDO enabled	1320	1500	1680	KHz
t_{WDT}	Watchdog reset time	WATCHDOG (REG07[5:4])=11, REGN LDO disabled	100	160		sec
		WATCHDOG (REG07[5:4])=11, REGN LDO enabled	136	160		sec

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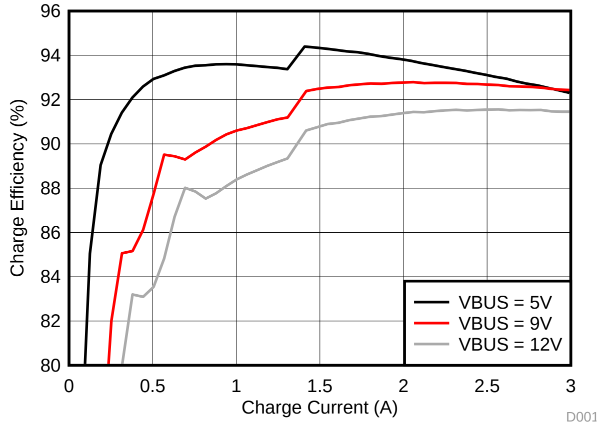
7.7 Typical Characteristics



VBAT = 3.8 V DCR = 10 mΩ

图 1. Charge Efficiency vs Charge Current

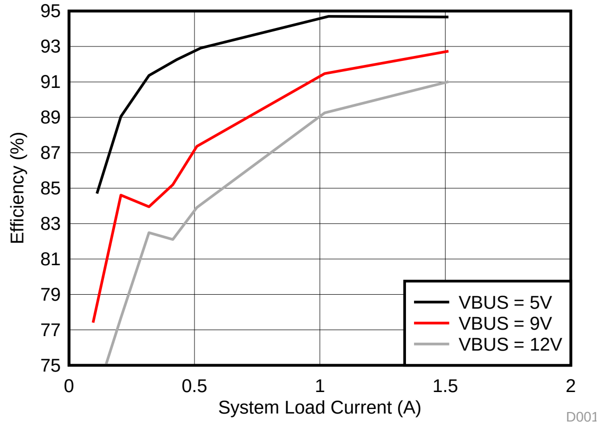
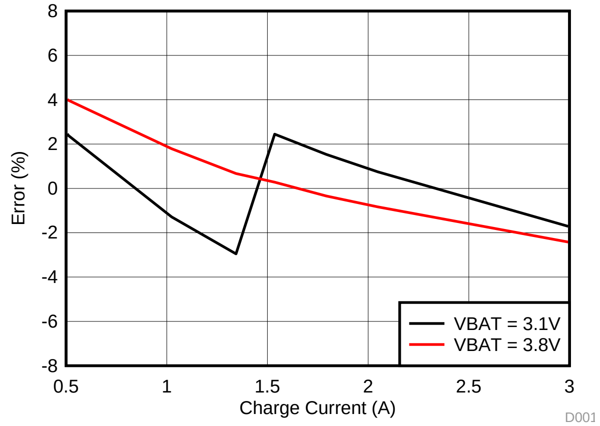
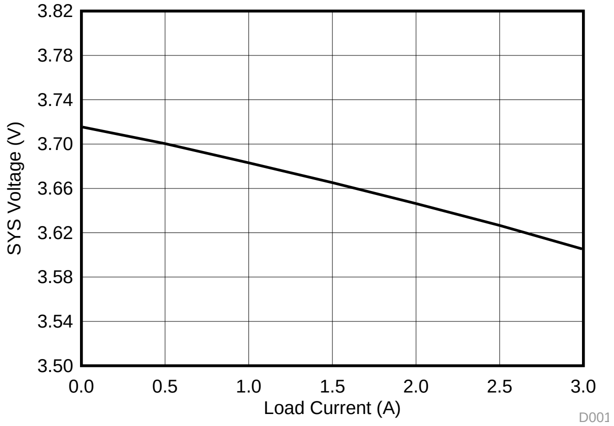


图 2. System Light Load Efficiency vs System Light Load Current



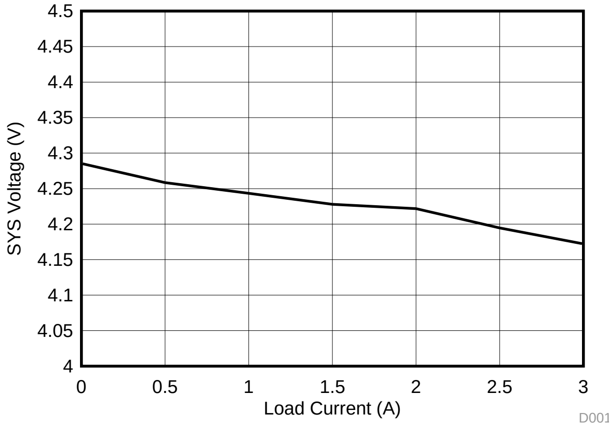
VBUS = 5 V

图 3. Charge Current Accuracy vs Charge Current I^2C Setting



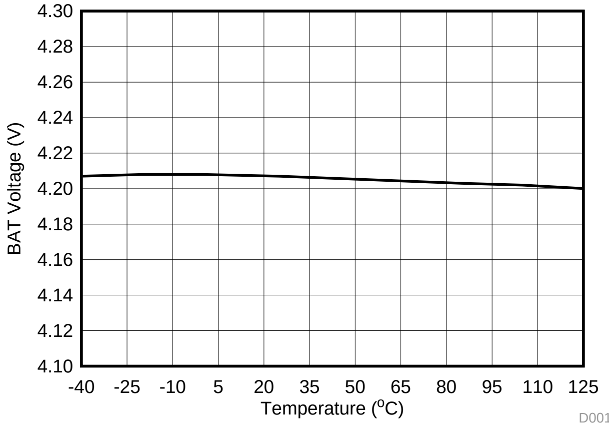
VBAT = 2.6 V VBUS = 5 V SYSMIN = 3.5 V

图 4. SYS Voltage Regulation vs System Load Current



VBAT = 4.2 V

图 5. SYS Voltage Regulation vs System Load Current



VBUS = 5 V

图 6. BAT Voltage vs Temperature

Typical Characteristics (接下页)

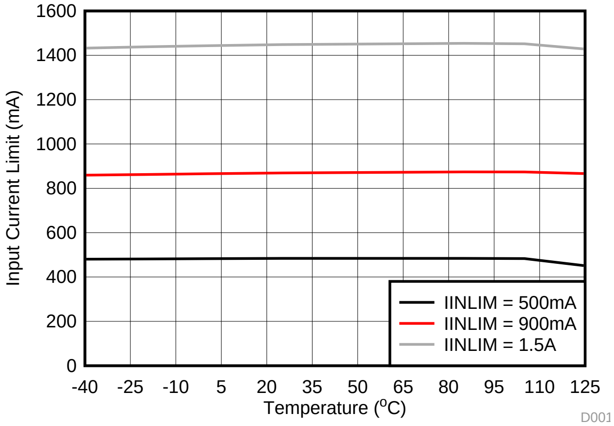


图 7. Input Current Limit vs Temperature

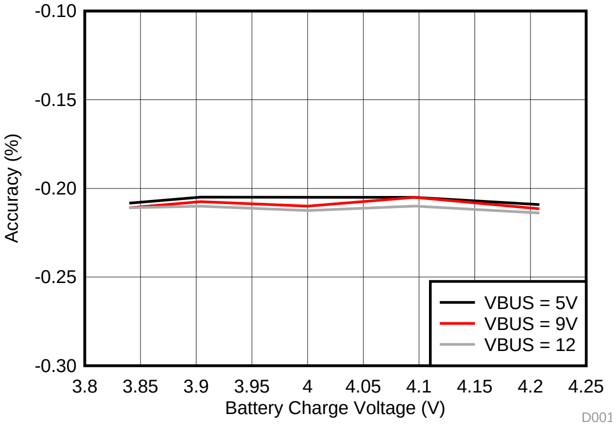


图 8. Charge Voltage Accuracy

8 Detailed Description

The device is a highly integrated 3-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It is highly integrated with the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2) , low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4). The device also integrates the boostrap diode for the high-side gate drive.

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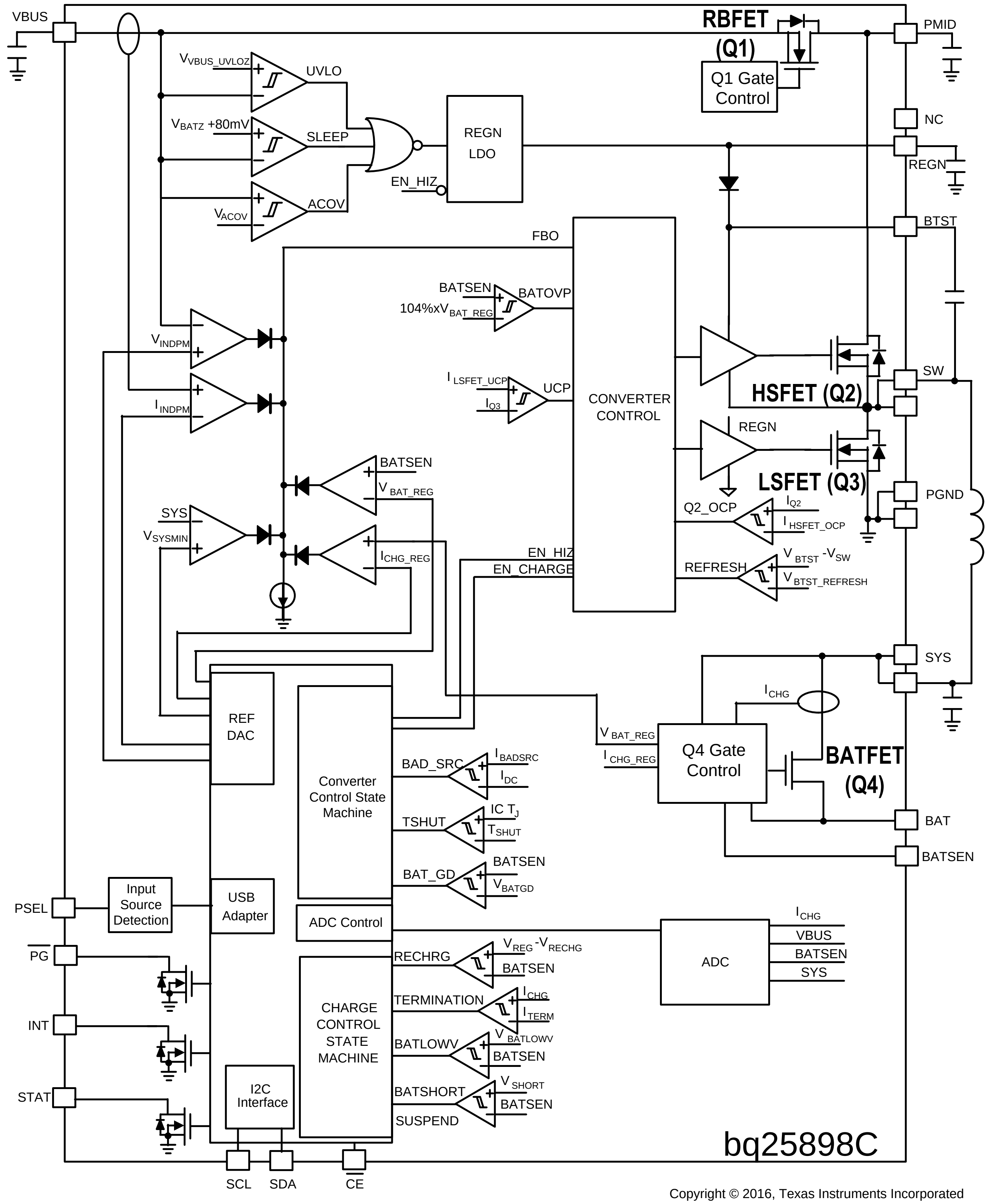
8.1 Functional Block Diagram



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8.2 Feature Description

8.2.1 Device Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS rises above V_{VBUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ} , the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

8.2.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DPLZ}), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted (IBAT > I_{BATFET_OCP}), the device turns off BATFET immediately until the input source plugs in again to re-enable BATFET.

8.2.3 Device Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started when AUTO_DPDM_EN bit is set. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. *Input Source Type Detection* based on PSEL to set default Input Current Limit (IINLIM) register and input source type
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

8.2.3.1 Power Up REGN Regulation (LDO)

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid.

1. VBUS above V_{VBUS_UVLOZ}
2. VBUS above $V_{BAT} + V_{SLEEPZ}$ in buck mode
3. After 220 ms delay is completed

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

8.2.3.2 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to start the buck converter.

1. VBUS voltage below V_{ACOV}
2. VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the INT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

8.2.3.3 Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the charger device runs *Input Source Type Detection* when AUTO_DPDM_EN bit is set.

After input source type detection, an INT pulse is asserted to the host. In addition, the following registers and pin are changed:

Feature Description (接下页)

1. Input Current Limit (IINLIM) register is changed to set current limit
2. PG_STAT bit is set

The host can over-write IINLIM register to change the input current limit if needed. The charger input current is always limited by the lower of IINLIM register at all-time.

When AUTO_DPDM_EN is disabled, the *Input Source Type Detection* is bypassed. The Input Current Limit (IINLIM) register, VBUS_STAT, and SPD_STAT bits are unchanged from previous values.

8.2.3.3.1 PSEL Pin Sets Input Current Limit

The bq25898C has PSEL interface for input current limit setting to interface with USB PHY. It directly takes the USB PHY device output to decide whether the input is USB host or charging port. To implement USB100 in the system, the host can enter HiZ mode by setting EN_HIZ bit after 2 min charging with 500 mA input current limit.

表 1. bq25898C Result

INPUT DETECTION	BAT VOLTAGE	PSEL PIN	INPUT CURRENT LIMIT (IINLIM)	SDP_STAT	VBUS_STAT
USB SDP (USB500)	X	High	500 mA	1	001
Adapter	X	Low	1.5 A		010

8.2.3.3.2 Force Input Current Limit Detection

In host mode, the host can force the device to run by setting FORCE_DPDM bit. After the detection is completed, FORCE_DPDM bit returns to 0 by itself and Input Result is updated.

8.2.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V – 14 V) for high voltage charging and provides two methods to set Input Voltage Limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM (FORCE_VINDPM=1)

   By setting FORCE_VINDPM bit to 1, the VINDPM threshold setting algorithm is disabled. Register VINDPM is writable and allows host to set the absolute threshold of VINDPM function.
2. Relative VINDPM based on VINDPM_OS registers (FORCE_VINDPM=0) (Default)

When FORCE_VINDPM bit is 0 (default), the VINDPM threshold setting algorithm is enabled. The VINDPM register is read only and the charger controls the register by using VINDPM Threshold setting algorithm. The algorithm allows a wide range of adapter (V_{VBUS_OP}) to be used with flexible VINDPM threshold.

After Input Voltage Limit Threshold is set, an INT pulse is generated to signal to the host.

8.2.3.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current limit is forced to the lower of 200 mA or IINLIM register setting. After the system rises above 2.2 V, the device limits input current to the IILIM register.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

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8.2.4 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.2.4.1 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IINLIM or IDPM_LIM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT (VINDPM) and/or IDPM_STAT (IINDPM) is/are set high. 图 9 shows the DPM response with 9V/1.2A adapter, 3.2-V battery, 2.8-A charge current and 3.4-V minimum system voltage setting.

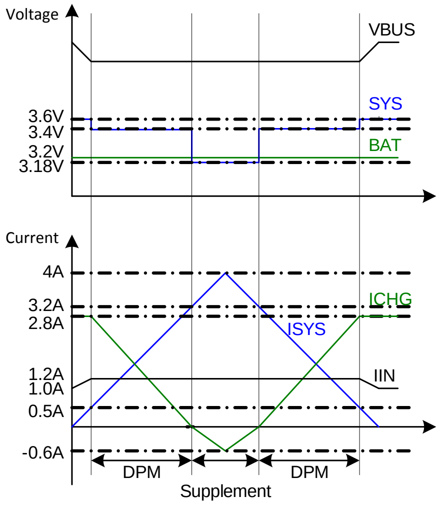

图 9. DPM Response

8.2.5 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3-A charge current for high capacity battery. The 5-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

8.2.5.1 Autonomous Charging Cycle

With battery charging enabled (CHG_CONFIG bit = 1, $\overline{CE}$ pin is low, and REG04[6:0] is not set to 0 mA), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in . The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

表 2. Charging Parameter Default Setting

DEFAULT MODE	bq25898C
Charging Voltage	4.208 V
Charging Current	0 A (charge disable)
Pre-charge Current	0 mA (precharge disabled)
Termination Current	256 mA

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表 2. Charging Parameter Default Setting (接下页)

DEFAULT MODE	bq25898C
Safety Timer	12 hour

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by setting CHG_CONFIG bit, /CE pin is low and ICHG register is not 0 mA
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device not in DPM mode or thermal regulation. When a full battery voltage is discharged below recharge threshold (threshold selectable via VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, either toggle $\overline{\text{CE}}$ pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT_DIS bit. In addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

8.2.5.2 Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and regulates current / voltage.

表 3. Charging Current Setting

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	CHRG_STAT
< 2 V	$I_{BATSHORT}$	–	01
2 V – 3 V	I_{PRECHG}	0 mA (precharge disabled)	01
> 3 V	I_{CHG}	0 (charge disabled)	00

If the charger device is in DPM regulation or thermal regulation during charging, the charging current can be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

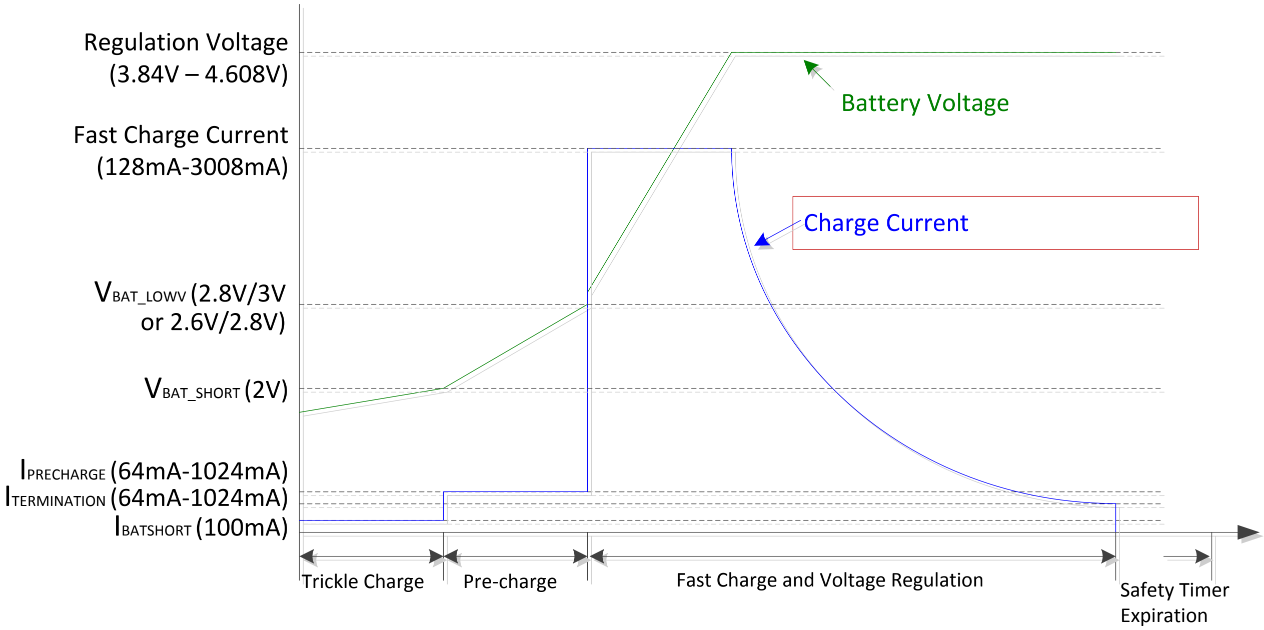

图 10. Battery Charging Profile

8.2.5.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage .

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

8.2.5.4 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 4 hours when the battery is below $V_{BATLOWV}$ threshold. The user can program fast charge safety timer through I^2C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled via I2C by setting EN_TIMER bit.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

8.2.6 Battery Monitor

The device includes a battery monitor to provide measurements of VBUS voltage, battery voltage, system voltage, thermistor ratio, and charging current, and charging current based on the device's modes of operation. The measurements are reported in Battery Monitor Registers (REG0E-REG12). The battery monitor can be configured as two conversion modes by using CONV_RATE bit: one-shot conversion (default) and 1 second continuous conversion.

For one-shot conversion (CONV_RATE = 0), the CONV_START bit can be set to start the conversion. During the conversion, the CONV_START is set and it is cleared by the device when conversion is completed. The conversion result is ready after t_{CONV} (maximum 1 second).

For continuous conversion (CONV_RATE = 1), the CONV_RATE bit can be set to initiate the conversion. During active conversion, the CONV_START is set to indicate conversion is in progress. The battery monitor provides conversion result every 1 second automatically. The battery monitor exits continuous conversion mode when CONV_RATE is cleared.

When battery monitor is active, the REGN power is enabled and can increase device quiescent current.

表 4. Battery Monitor Modes of Operation

PARAMETER	REGISTER	MODES OF OPERATION		
		CHARGE MODE	DISABLE CHARGE MODE	BATTERY ONLY MODE
Battery Voltage (V_{BAT})	REG0E	Yes	Yes	Yes
System Voltage (V_{SYS})	REG0F	Yes	Yes	Yes
VBUS Voltage (V_{VBUS})	REG11	Yes	Yes	NA
Charge Current (I_{BAT})	REG12	Yes	NA	NA

8.2.7 Status Outputs ($\overline{PG}$, STAT, and INT)

8.2.7.1 Power Good Indicator ($\overline{PG}$)

In bq25898C, the $\overline{PG}$ goes LOW to indicate a good input source when:

1. VBUS above V_{VBUS_UVLO}
2. VBUS above battery (not in sleep)
3. VBUS below V_{ACOV} threshold
4. VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
5. Completed *Input Source Type Detection*

8.2.7.2 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as shown in . The STAT pin function can be disable by setting STAT_DIS bit.

表 5. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input overvoltage, timer fault, input or system overvoltage)	blinking at 1 Hz

8.2.7.3 Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256-µs INT pulse.

- USB/adapter source identified (through PSEL detection)
- Good input source detected
  - VBUS above battery (not in sleep)
  - VBUS below V_{ACOV} threshold
  - VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Input removed
- Charge Complete
- Any FAULT event in REG0C

When a fault occurs, the charger device sends out INT and keeps the fault state in REG0C until the host reads the fault register. Before the host reads REG0C and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG0C two times consecutively. The 1st read reports the pre-existing fault register status and the 2nd read reports the current fault register status.

8.2.8 Thermal Regulation and Thermal Shutdown

8.2.8.1 Thermal Protection in Buck Mode

The device monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device lowers down the charge current. The wide thermal regulation range from 60ºC to 120ºC allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT}. The fault register CHRG_FAULT is set to 10 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is below T_{SHUT_HYS}.

8.2.9 Voltage and Current Monitoring in Buck

8.2.9.1 Voltage and Current Monitoring in Buck Mode

The device closely monitors the input and system voltage, as well as HSFET current for safe buck mode operations.

8.2.9.1.1 Input Overvoltage (ACOV)

The input voltage for buck mode operation is V_{VBUS_OP}. If VBUS voltage exceeds V_{ACOV}, the device stops switching immediately. During input over voltage (ACOV), the fault register CHRG_FAULT bits sets to 01. An INT is asserted to the host.

8.2.9.1.2 System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. When SYSOVP is detected, the converter stops immediately to clamp the overshoot.

8.2.10 Battery Protection

8.2.10.1 Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

8.2.10.2 Battery Over-Discharge Protection

When battery is discharged below V_{BAT_DPL}, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at VBUS. When an input source is plugged in, the BATFET turns on. Thy is charged with $I_{BATSHORT}$ (typically 100 mA) current when the VBAT < V_{SHORT}, or precharge current as set in IPRECHG register when the battery voltage is between V_{SHORT} and $V_{BATLOWV}$.

8.2.11 Serial Interface

The device uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG14. Register read beyond REG14 (0x14) returns 0xFF. The I^2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

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8.2.11.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

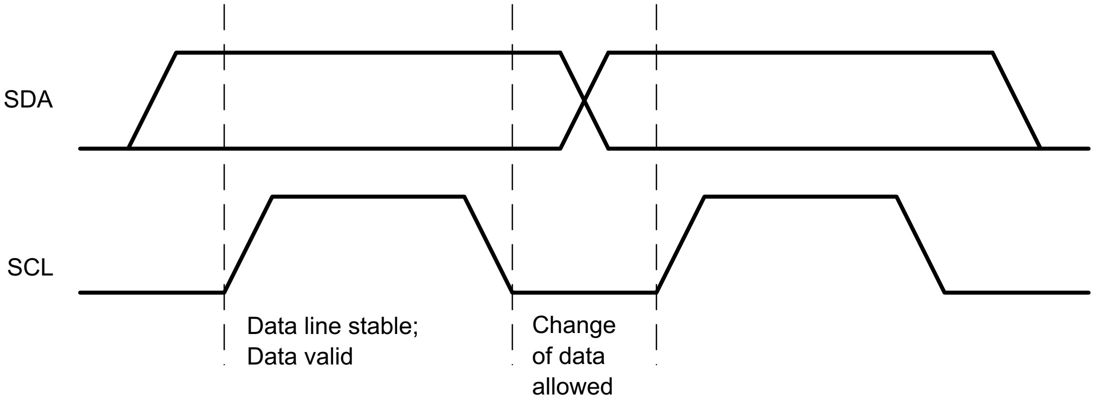

图 11. Bit Transfer on the I²C Bus

8.2.11.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

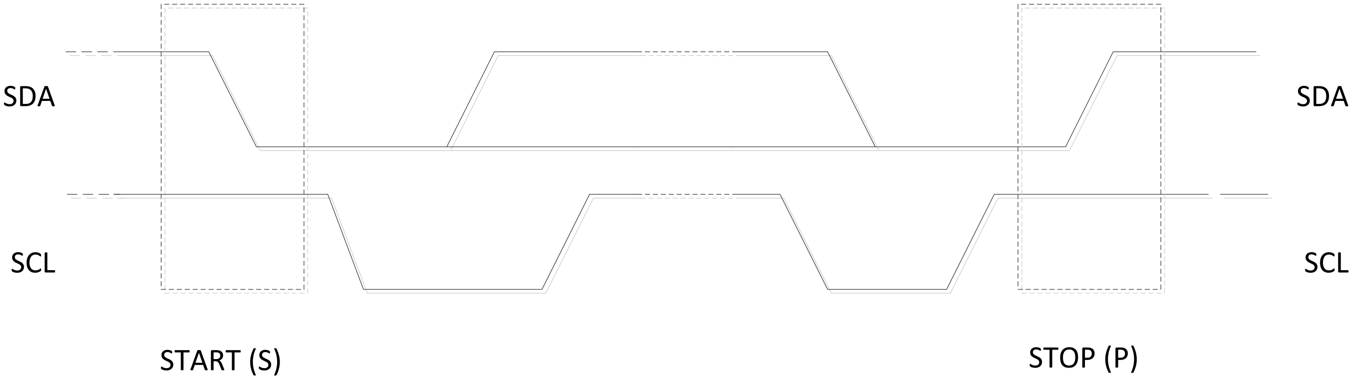

图 12. START and STOP conditions

8.2.11.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

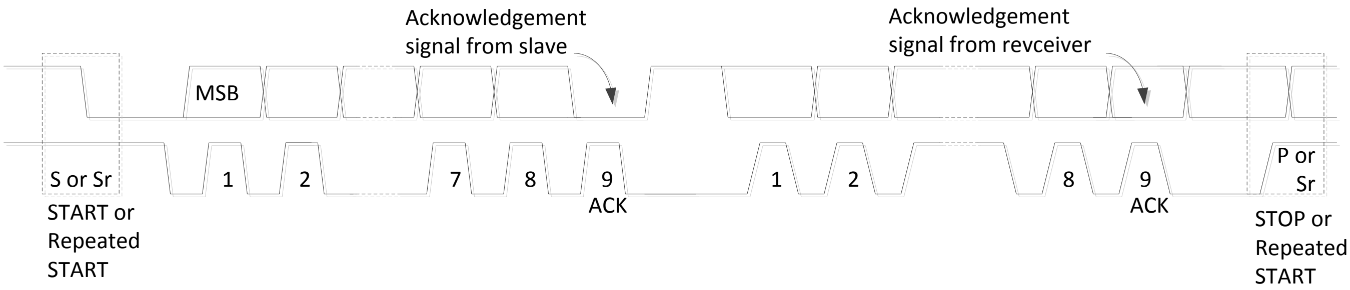

图 13. Data Transfer on the I^2C Bus

8.2.11.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.2.11.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

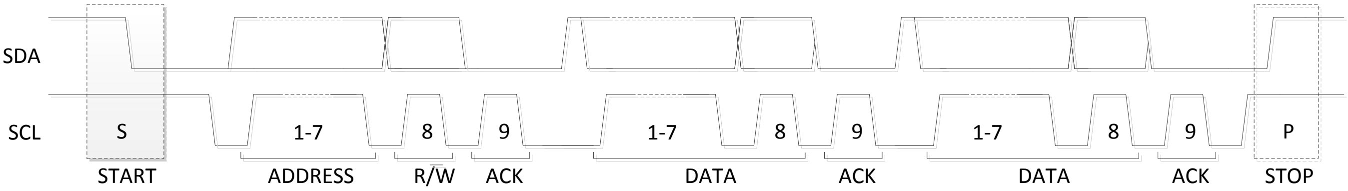

图 14. Complete Data Transfer

8.2.11.6 Single Read and Write

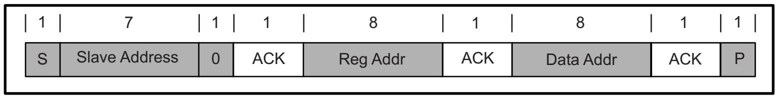

图 15. Single Write

图 16. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.2.11.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG14 except REG0C.

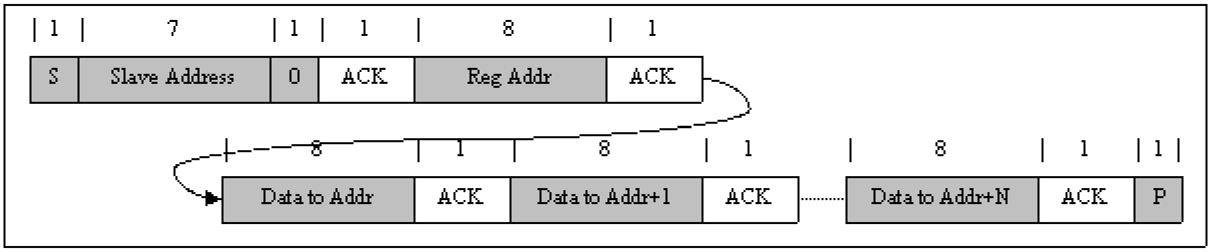

图 17. Multi-Write

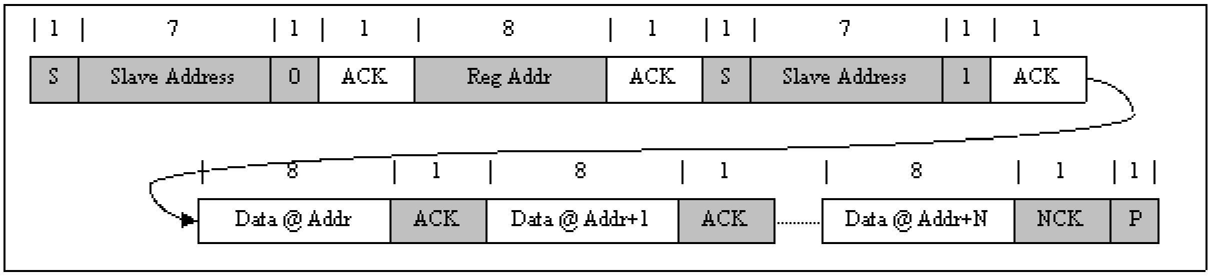

图 18. Multi-Read

REG0C is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG0C reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG0C for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. In addition, REG0C does not support multi-read and multi-write.

8.3 Device Functional Modes

8.3.1 Host Mode and Default Mode

The device is a host controlled charger. The device cannot operate in default mode without host management because default charge current is set to 0 mA (charge disabled).

All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

When the watchdog timer (WATCHDOG_FAULT bit = 1) is expired, the device returns to default mode and all registers are reset to default values except IINLIM, VINDPM, VINDPM_OS bits.

Device Functional Modes (接下页)

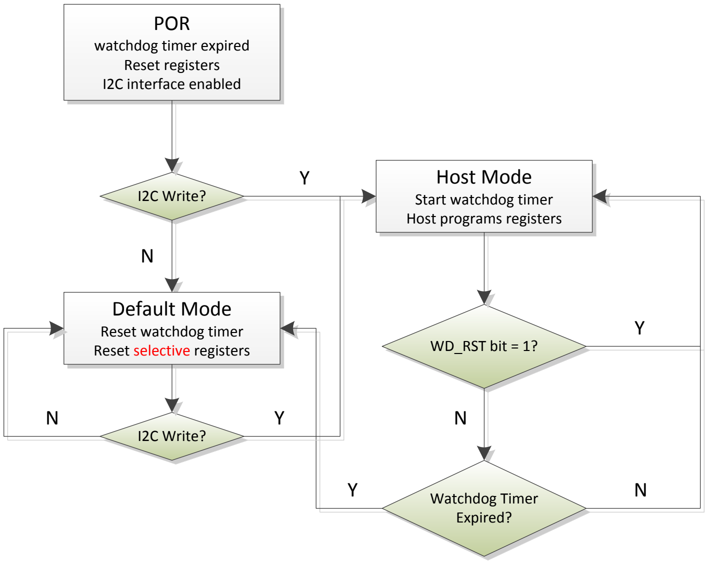

图 19. Watchdog Timer Flow Chart

8.4 Register Map

I2C Slave Address: 6BH (1101011B + R/$\overline{W}$)

8.4.1 REG00

图 20. REG00

7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 6. REG00

Bit	Field	Type	Reset	Description	
7	EN_HIZ	R/W	by REG_RST by Watchdog	Enable HIZ Mode 0 – Disable (default) 1 – Enable	
6	Reserved	R	N/A	Reserved Always reads 1	
5	IINLIM[5]	R/W	by REG_RST	1600mA	Input Current Limit Offset: 100mA Range: 100mA (000000) – 3.25A (111111) Default:011100 (1500mA) (Actual input current limit is the lower of I2C or ILIM pin) IINLIM bits are changed automatically after input source type detection is completed
4	IINLIM[4]	R/W	by REG_RST	800mA	
3	IINLIM[3]	R/W	by REG_RST	400mA	
2	IINLIM[2]	R/W	by REG_RST	200mA	
1	IINLIM[1]	R/W	by REG_RST	100mA	
0	IINLIM[0]	R/W	by REG_RST	50mA	

8.4.2 REG01

图 21. REG01

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R	R	R	R	R	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7. REG01

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved, Always read 0
6	Reserved	R	N/A	Reserved, Always read 0
5	Reserved	R	N/A	Reserved, Always read 0
4	Reserved	R	N/A	Reserved, Always read 0
3	Reserved	R	N/A	Reserved, Always read 0
2	Reserved	R	N/A	Reserved, Always read 0
1	Reserved	R	N/A	Reserved, Always read 0
0	VDPM_OS	R/W	by REG_RST	VINDPM offset threshold Default 600mV (1) 0 - 400mA offset 1 - 600mA offset

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8.4.3 REG02

图 22. REG02

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R/W	R/W	R	R	R	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8. REG02

Bit	Field	Type	Reset	Description
7	CONV_START	R/W	by REG_RST by Watchdog	ADC Conversion Start Control 0 – ADC conversion not active (default). 1 – Start ADC Conversion This bit is read-only when CONV_RATE = 1. The bit stays high during ADC conversion and during input source detection.
6	CONV_RATE	R/W	by REG_RST by Watchdog	ADC Conversion Rate Selection 0 – One shot ADC conversion (default) 1 – Start 1s Continuous Conversion
5	Reserved	R	N/A	Reserved, Always read 0
4	Reserved	R	N/A	Reserved, Always read 0
3	Reserved	R	N/A	Reserved, Always read 0
2	Reserved	R	N/A	Reserved, Always read 0
1	FORCE_DPDM	R/W	by REG_RST by Watchdog	Force PSEL Detection 0 – Not in PSEL detection (default) 1 – Force PSEL detection
0	AUTO_DPDM_EN	R/W	by REG_RST	Automatic Detection Enable 0 –Disable PSEL detection when VBUS is plugged-in 1 –Enable PEL detection when VBUS is plugged-in (default)

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8.4.4 REG03

图 23. REG03

7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0
R	R/W	R	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9. REG03

Bit	Field	Type	Reset	Description	
7	Reserved	R	N/A	Reserved Always read 0	
6	WD_RST	R/W	by REG_RST by Watchdog	I2C Watchdog Timer Reset 0 – Normal (default) 1 – Reset (Back to 0 after timer reset)	
5	Reserved	R	N/A	Reserved Always read 0	
4	CHG_CONFIG	R/W	by REG_RST by Watchdog	Charge Enable Configuration 0 - Charge Disable 1- Charge Enable (default)	
3	SYS_MIN[2]	R/W	by REG_RST	0.4V	Minimum System Voltage Limit Offset: 3.0V Range 3.0V-3.7V Default: 3.5V (101)
2	SYS_MIN[1]	R/W	by REG_RST	0.2V	
1	SYS_MIN[0]	R/W	by REG_RST	0.1V	
0	Reserved	R	N/A	Reserved Always read 0	

8.4.5 REG04

图 24. REG04

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 10. REG04

Bit	Field	Type	Reset	Description	
7	Reserved	R	N/A	Reserved Always reads 0	
6	Reserved	R	N/A	Reserved Always reads 0	
5	ICHG[5]	R/W	by REG_RST by Watchdog	2048mA	Fast Charge Current Limit Offset: 0mA Range: 0mA (000000) – 3008mA (101111) Default: 0mA (000000) Note: ICHG=000000 (0mA) disables both fast charge and precharge ICHG > 101111 (3008mA) is clamped to register value 101111 (3008mA)
4	ICHG[4]	R/W	by REG_RST by Watchdog	1024mA	
3	ICHG[3]	R/W	by REG_RST by Watchdog	512mA	
2	ICHG[2]	R/W	by REG_RST by Watchdog	256mA	
1	ICHG[1]	R/W	by REG_RST by Watchdog	128mA	
0	ICHG[0]	R/W	by REG_RST by Watchdog	64mA	

8.4.6 REG05

图 25. REG05

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 11. REG05

Bit	Field	Type	Reset	Description	
7	IPRECHG[3]	R/W	by REG_RST by Watchdog	512mA	Precharge Current Limit Offset: 64mA Range: 64mA – 1024mA Default: 0mA when REG04[5:0] = 000000
6	IPRECHG[2]	R/W	by REG_RST by Watchdog	256mA	
5	IPRECHG[1]	R/W	by REG_RST by Watchdog	128mA	
4	IPRECHG[0]	R/W	by REG_RST by Watchdog	64mA	
3	ITERM[3]	R/W	by REG_RST by Watchdog	512mA	Termination Current Limit Offset: 64mA Range: 64mA – 1024mA Default: 256mA (0011)
2	ITERM[2]	R/W	by REG_RST by Watchdog	256mA	
1	ITERM[1]	R/W	by REG_RST by Watchdog	128mA	
0	ITERM[0]	R/W	by REG_RST by Watchdog	64mA	

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8.4.7 REG06

图 26. REG06

7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 12. REG06

Bit	Field	Type	Reset	Description	
7	VREG[5]	R/W	by REG_RST by Watchdog	512mV	Charge Voltage Limit Offset: 3.840V Range: 3.840V – 4.608V (110000) Default: 4.208V (010111) Note: VREG > 110000 (4.608V) is clamped to register value 110000 (4.608V)
6	VREG[4]	R/W	by REG_RST by Watchdog	256mV	
5	VREG[3]	R/W	by REG_RST by Watchdog	128mV	
4	VREG[2]	R/W	by REG_RST by Watchdog	64mV	
3	VREG[1]	R/W	by REG_RST by Watchdog	32mV	
2	VREG[0]	R/W	by REG_RST by Watchdog	16mV	
1	BATLOWV	R/W	by REG_RST by Watchdog	Battery Precharge to Fast Charge Threshold 0 – 2.8V 1 – 3.0V (default)	
0	VRECHG	R/W	by REG_RST by Watchdog	Battery Recharge Threshold Offset (below Charge Voltage Limit) 0 – 100mV (V_{RECHG}) below VREG (REG06[7:2]) (default) 1 – 200mV (V_{RECHG}) below VREG (REG06[7:2])	

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8.4.8 REG07

图 27. REG07

7	6	5	4	3	2	1	0
1	0	0	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 13. REG07

Bit	Field	Type	Reset	Description
7	EN_TERM	R/W	by REG_RST by Watchdog	Charging Termination Enable 0 – Disable 1 – Enable (default)
6	STAT_DIS	R/W	by REG_RST by Watchdog	STAT Pin Disable 0 – Enable STAT pin function (default) 1 – Disable STAT pin function
5	WATCHDOG[1]	R/W	by REG_RST by Watchdog	I2C Watchdog Timer Setting 00 – Disable watchdog timer 01 – 40s (default) 10 – 80s 11 – 160s
4	WATCHDOG[0]	R/W	by REG_RST by Watchdog	
3	EN_TIMER	R/W	by REG_RST by Watchdog	Charging Safety Timer Enable 0 – Disable 1 – Enable (default)
2	CHG_TIMER[1]	R/W	by REG_RST by Watchdog	Fast Charge Timer Setting 00 – 5 hrs 01 – 8 hrs 10 – 12 hrs (default) 11 – 20 hrs
1	CHG_TIMER[0]	R/W	by REG_RST by Watchdog	
0	Reserved	R	N/A	Reserved always reads 1

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8.4.9 REG08

图 28. REG08

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R	R	R	R	R	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 14. REG08

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved Always reads 000
6	Reserved	R	N/A	
5	Reserved	R	N/A	
4	Reserved	R	N/A	Reserved Always reads 000
3	Reserved	R	N/A	
2	Reserved	R	N/A	
1	TREG[1]	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold 00 – 60°C 01 – 80°C 10 – 100°C 11 – 120°C (default)
0	TREG[0]	R/W	by REG_RST by Watchdog	

8.4.10 REG09

图 29. REG09

7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0
R	R/W	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 15. REG09

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved Always reads 0
6	TMR2X_EN	R/W	by Watchdog	Safety Timer Setting during DPM or Thermal Regulation 0 – Safety timer not slowed by 2X during input DPM or thermal regulation 1 – Safety timer slowed by 2X during input DPM or thermal regulation (default)
5	BATFET_DIS	R/W	by REG_RST	Force BATFET off to enable ship mode with t_{SM_DLY} delay time 0 – Allow BATFET turn on (default) 1 – Force BATFET off
4	Reserved	R	N/A	Reserved Always reads 0
3	Reserved	R	N/A	Reserved Always reads 0
2	Reserved	R	N/A	Reserved Always reads 1
1	Reserved	R	N/A	Reserved Always reads 0
0	Reserved	R	N/A	Reserved Always reads 0

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8.4.11 REG0A

图 30. REG0A

7	6	5	4	3	2	1	0
0	1	1	1	0	1	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 16. REG0A

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved Always reads 0
6	Reserved	R	N/A	Reserved Always reads 1
5	Reserved	R	N/A	Reserved Always reads 1
4	Reserved	R	N/A	Reserved Always reads 1
3	Reserved	R	N/A	Reserved Always reads 0
2	Reserved	R	N/A	Reserved Always reads 1
1	Reserved	R	N/A	Reserved Always reads 0
0	Reserved	R	N/A	Reserved Always reads 0

8.4.12 REG0B

图 31. REG0B

7	6	5	4	3	2	1	0
x	x	x	x	x	x	1	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 17. REG0B

Bit	Field	Type	Reset	Description
7	VBUS_STAT[2]	R	N/A	VBUS Status register 000: No Input 001: USB Host SDP 010: Adapter (3.25A) 111: N/A Note: Software current limit is reported in IINLIM register
6	VBUS_STAT[1]	R	N/A	
5	VBUS_STAT[0]	R	N/A	
4	CHRG_STAT[1]	R	N/A	Charging Status 00 – Not Charging 01 – Pre-charge (< $V_{BATLOWV}$) 10 – Fast Charging 11 – Charge Termination Done
3	CHRG_STAT[0]	R	N/A	
2	PG_STAT	R	N/A	Power Good Status 0 – Not Power Good 1 – Power Good
1	Reserved	R	N/A	Reserved
0	VSYS_STAT	R	N/A	VSYS Regulation Status 0 – Not in VSYSMIN regulation (BAT > VSYSMIN) 1 – In VSYSMIN regulation (BAT < VSYSMIN)

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8.4.13 REG0C

图 32. REG0C

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 18. REG0C

Bit	Field	Type	Reset	Description
7	WATCHDOG_FAULT	R	N/A	Watchdog Fault Status Status 0 – Normal 1- Watchdog timer expiration
6	Reserved	R	N/A	Reserved
5	CHRG_FAULT[1]	R	N/A	Charge Fault Status 00 – Normal 01 – Input fault (VBUS > V_{ACOV} or VBAT < VBUS < $V_{VBUSMIN}$(typical 3.8V)) 10 - Thermal shutdown 11 – Charge Safety Timer Expiration
4	CHRG_FAULT[0]	R	N/A	
3	BAT_FAULT	R	N/A	Battery Fault Status 0 – Normal 1 – BATOVP (VBAT > V_{BATOVP})
2	Reserved	R	N/A	Reserved
1	Reserved	R	N/A	Reserved
0	Reserved	R	N/A	Reserved

8.4.14 REG0D

图 33. REG0D

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 19. REG0D

Bit	Field	Type	Reset	Description	
7	FORCE_VINDPM	R/W	by REG_RST	VINDPM Threshold Setting Method 0 – Run Relative VINDPM Threshold (default) 1 – Run Absolute VINDPM Threshold	
6	VINDPM[6]	R/W	by REG_RST	6400mV	Absolute VINDPM Threshold Offset: 2.6V Range: 3.9V (0001101) – 15.3V (1111111) Default: 4.4V (0010010) Note: Value < 0001101 is clamped to 3.9V (0001101) Register is read only when FORCE_VINDPM=0 and can be written by internal control based on relative VINDPM threshold setting Register can be read/write when FORCE_VINDPM = 1
5	VINDPM[5]	R/W	by REG_RST	3200mV	
4	VINDPM[4]	R/W	by REG_RST	1600mV	
3	VINDPM[3]	R/W	by REG_RST	800mV	
2	VINDPM[2]	R/W	by REG_RST	400mV	
1	VINDPM[1]	R/W	by REG_RST	200mV	
0	VINDPM[0]	R/W	by REG_RST	100mV	

8.4.15 REG0E

图 34. REG0E

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 20. REG0E

Bit	Field	Type	Reset	Description	
7	THERM_STAT	R	N/A	Thermal Regulation Status 0 – Normal 1 – In Thermal Regulation	
6	BATV[6]	R	N/A	1280mV	ADC conversion of Battery Voltage (V_{BAT})
5	BATV[5]	R	N/A	640mV	
4	BATV[4]	R	N/A	320mV	
3	BATV[3]	R	N/A	160mV	
2	BATV[2]	R	N/A	80mV	
1	BATV[1]	R	N/A	40mV	
0	BATV[0]	R	N/A	20mV	

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8.4.16 REG0F

图 35. REG0F

7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 21. REG0F

Bit	Field	Type	Reset	Description	
7	Reserved	R	N/A	Reserved: Always reads 0	
6	SYSV[6]	R	N/A	1280mV	ADC conversion of System Voltage (V_{SYS})
5	SYSV[5]	R	N/A	640mV	
4	SYSV[4]	R	N/A	320mV	
3	SYSV[3]	R	N/A	160mV	
2	SYSV[2]	R	N/A	80mV	
1	SYSV[1]	R	N/A	40mV	
0	SYSV[0]	R	N/A	20mV	

8.4.17 REG11

图 36. REG11

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 22. REG11

Bit	Field	Type	Reset	Description	
7	VBUS_GD	R	N/A	VBUS Good Status 0 – Not VBUS attached 1 – VBUS Attached	
6	VBUSV[6]	R	N/A	6400mV	ADC conversion of VBUS voltage (V_{BUS}) Offset: 2.6V Range 2.6V (0000000) – 15.3V (1111111) Default: 2.6V (0000000)
5	VBUSV[5]	R	N/A	3200mV	
4	VBUSV[4]	R	N/A	1600mV	
3	VBUSV[3]	R	N/A	800mV	
2	VBUSV[2]	R	N/A	400mV	
1	VBUSV[1]	R	N/A	200mV	
0	VBUSV[0]	R	N/A	100mV	

8.4.18 REG12

图 37. REG12

7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 23. REG12

Bit	Field	Type	Reset	Description	
7	Reserved	R	N/A	Always reads 0	
6	ICHGR[6]	R	N/A	3200mA	ADC conversion of Charge Current (I_{BAT}) when $V_{BAT} > V_{BATSHORT}$ Offset: 0mA Range 0mA (0000000) – 6350mA (1111111) Default: 0mA (0000000) Note: This register returns 0000000 for $V_{BAT} < V_{BATSHORT}$
5	ICHGR[5]	R	N/A	1600mA	
4	ICHGR[4]	R	N/A	800mA	
3	ICHGR[3]	R	N/A	400mA	
2	ICHGR[2]	R	N/A	200mA	
1	ICHGR[1]	R	N/A	100mA	
0	ICHGR[0]	R	N/A	50mA	

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8.4.19 REG13

图 38. REG13

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 24. REG13

Bit	Field	Type	Reset	Description	
7	VDPM_STAT	R	N/A	VINDPM Status 0 – Not in VINDPM 1 – VINDPM	
6	IDPM_STAT	R	N/A	IINDPM Status 0 – Not in IINDPM 1 – IINDPM	
5	IDPM_LIM[5]	R	N/A	1600mA	Input Current Limit in effect
4	IDPM_LIM[4]	R	N/A	800mA	
3	IDPM_LIM[3]	R	N/A	400mA	
2	IDPM_LIM[2]	R	N/A	200mA	
1	IDPM_LIM[1]	R	N/A	100mA	
0	IDPM_LIM[0]	R	N/A	50mA	

8.4.20 REG14

图 39. REG14

7	6	5	4	3	2	1	0
0	x	0	0	1	1	0	1
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 25. REG14

Bit	Field	Type	Reset	Description
7	REG_RST	R/W	N/A	Register Reset 0 – Keep current register setting (default) 1 – Reset to default register value and reset safety timer Note: Reset to 0 after register reset is completed
6	Reserved	R	N/A	Reserved
5	PN[2]	R	N/A	Device Configuration 001: bq25898C
4	PN[1]	R	N/A	
3	PN[0]	R	N/A	
2	Reserved	R	N/A	Reserved Always reads 1
1	DEV_REV[1]	R	N/A	Device Revision: 01
0	DEV_REV[0]	R	N/A	

9 Application and Implementation

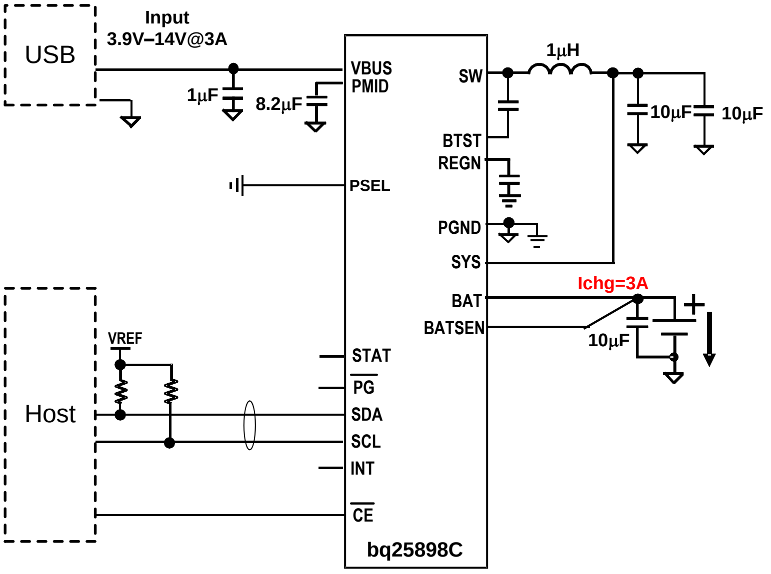
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the device configured as an I^{2}C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application Diagram



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VREF is the pull up voltage of I2C communication interface

图 40. bq25898C Application Diagram as Slave Charger

9.2.1 Design Requirements

For this design example, use the parameters shown in 表 26.

表 26. Design Parameters

PARAMETER	VALUE
Input voltage range	3.9 V to 14 V
Input current limit	1.5 A
Fast charge current	3000 mA
Output voltage	4.208 V

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9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{BAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \qquad (1)$$

The inductor ripple current depends on input voltage (V_{BUS}), duty cycle ($D = V_{BAT}/V_{VBUS}$), switching frequency (fs) and inductance (L):

$$I_{RIPPLE} = \frac{V_{BUS} \times D \times (1-D)}{f s \times L} \qquad (2)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.2 Buck Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{PMID} occurs where the duty cycle is closest to 50% and can be estimated by 公式 3:

$$I_{PMID} = I_{CHG} \times \sqrt{D \times (1 - D)} \qquad (3)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25 V rating or higher capacitor is preferred for up to 14-V input voltage. 8.2-µF capacitance is suggested.

9.2.2.3 System Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

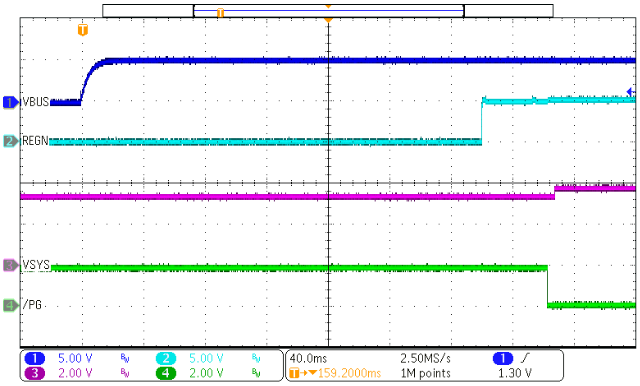
$$I_{CSYS} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \qquad (4)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{SYS}}{8\, LC_{SYS} f s^2} \left(1 - \frac{V_{SYS}}{V_{BUS}} \right) \qquad (5)$$

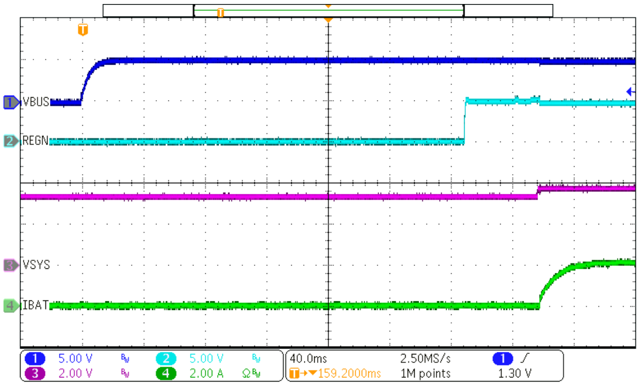
At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC. The charger device has internal loop compensator. To get good loop stability, 1-µH and minimum of 20-µF output capacitor is recommended. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.

9.2.3 Application Curves



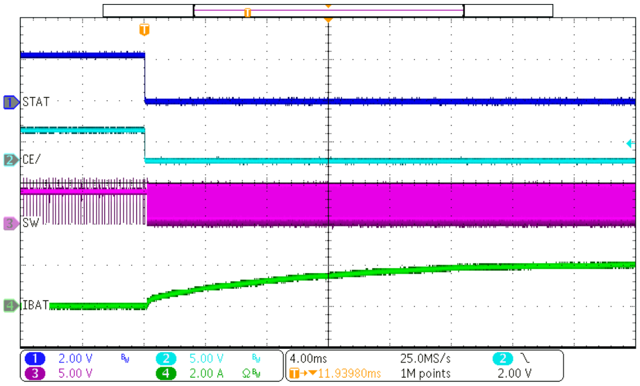
VBAT = 3.2 V, VBUS = 5 V

图 41. Power Up with Charge Disabled



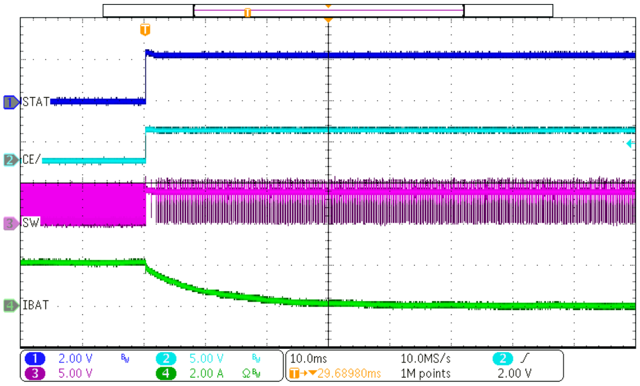
VBAT = 3.2 V, VBUS = 5 V

图 42. Power Up with Charge Enabled



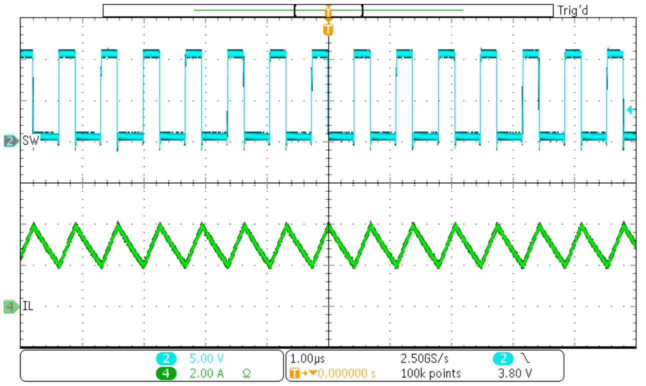
VBUS = 5 V

图 43. Charge Enable



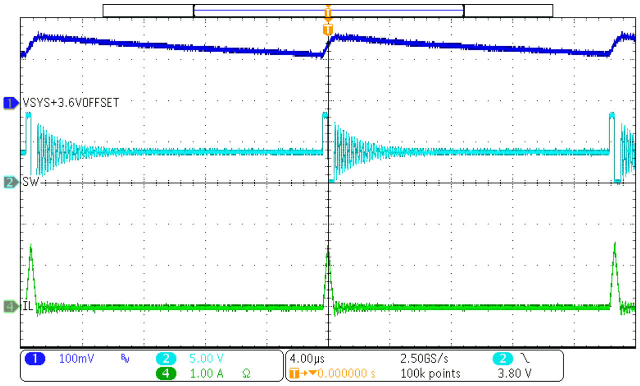
VBUS = 5 V

图 44. Charge Disable



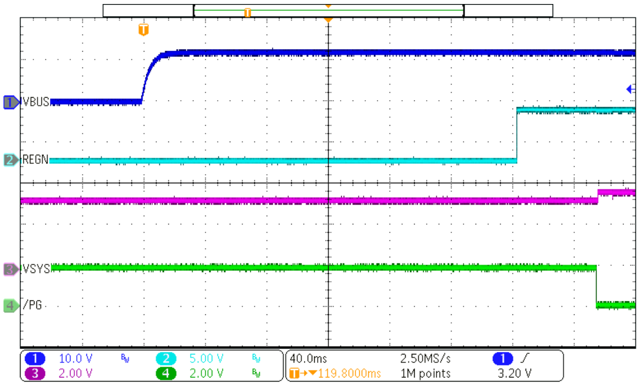
VBUS = 12 V VBAT = 3.8 V ICHG = 3 A

图 45. PWM Switching Waveform



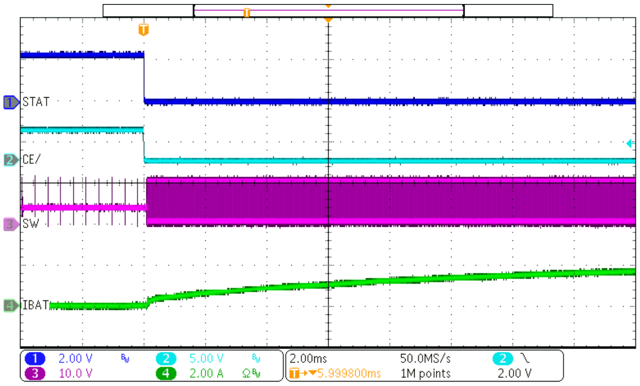
VBUS = 9V I_{SYS} = 20 mA, Charge Disable
No Battery

图 46. PFM Switching Waveform



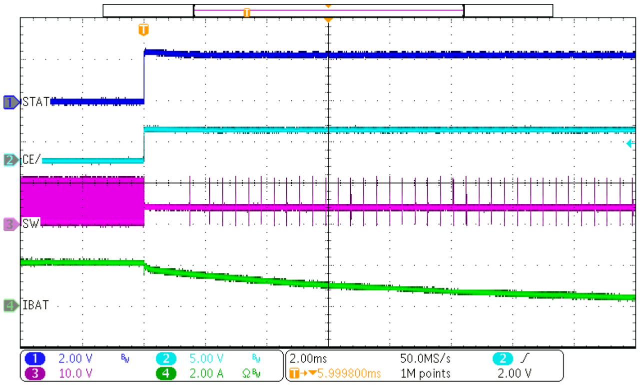
VBAT = 3.2 V VBUS = 12 V

图 47. Power Up with Charge Disabled



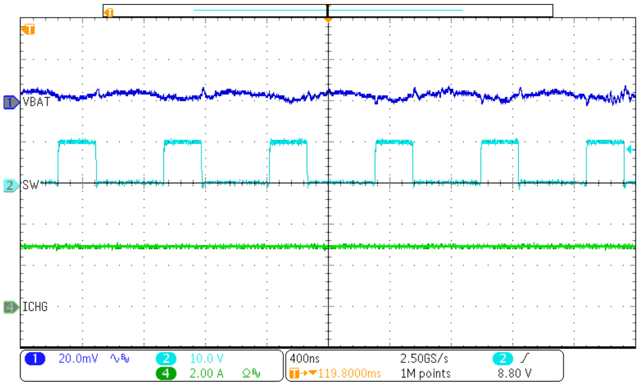
VBUS = 12 V

图 48. Charge Enable



VBUS = 12 V

图 49. Charge Disable



VBUS = 12 V VBAT = 3.8 V ICHG = 3 A

图 50. PWM Switching Waveform

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10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 14 V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see 图 51) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Put output capacitor near to the inductor and the IC.
3. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
4. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
5. Connect all grounds together to reduce PCB size and improve thermal dissipation.
6. Avoid ground planes in parallel with high frequency traces in other layers.

11.2 Layout Example

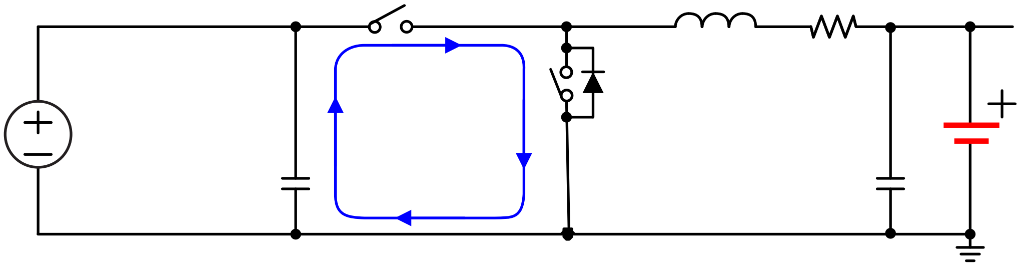

图 51. High Frequency Current Path

12 器件和文档支持

12.1 器件支持

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25898CYFFR	ACTIVE	DSBGA	YFF	42	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898C	Samples
BQ25898CYFFT	ACTIVE	DSBGA	YFF	42	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ25898C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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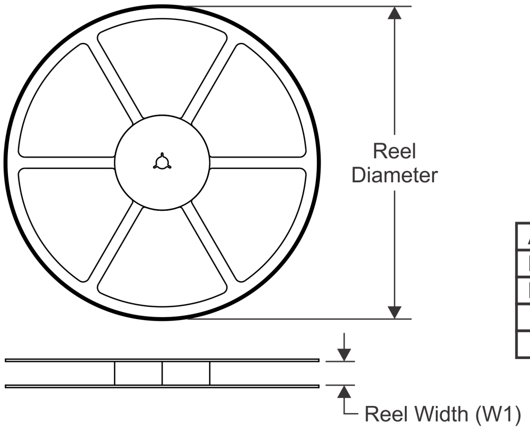
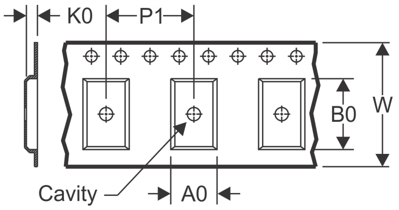
TAPE AND REEL INFORMATION

REEL DIMENSIONS

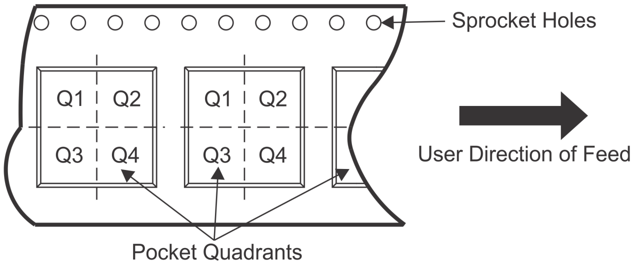


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

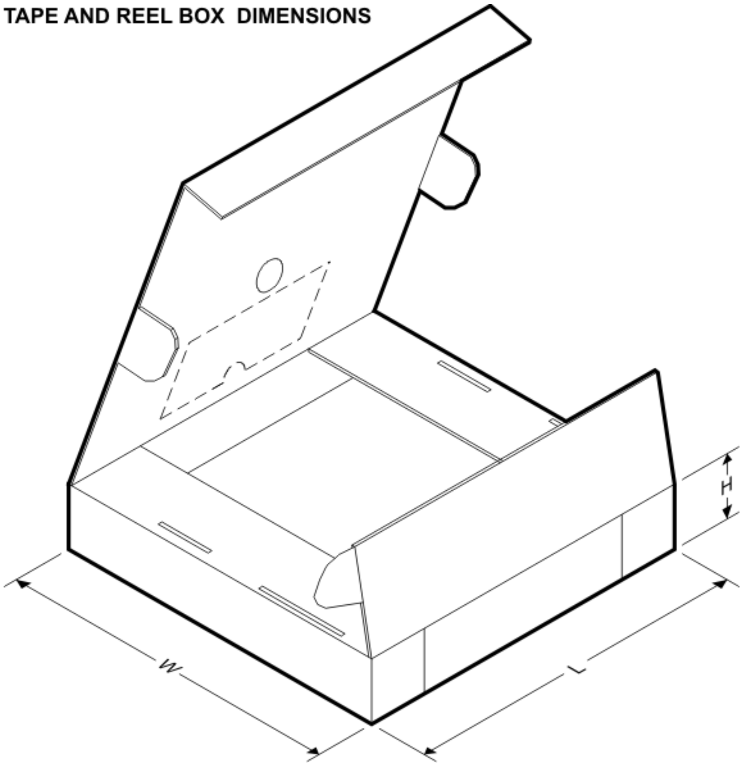
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

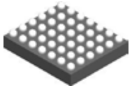
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25898CYFFR	DSBGA	YFF	42	3000	180.0	8.4	2.66	2.95	0.81	4.0	8.0	Q1
BQ25898CYFFT	DSBGA	YFF	42	250	180.0	8.4	2.66	2.95	0.81	4.0	8.0	Q1
BQ25898CYFFT	DSBGA	YFF	42	250	180.0	8.4	2.66	2.95	0.81	4.0	8.0	Q1

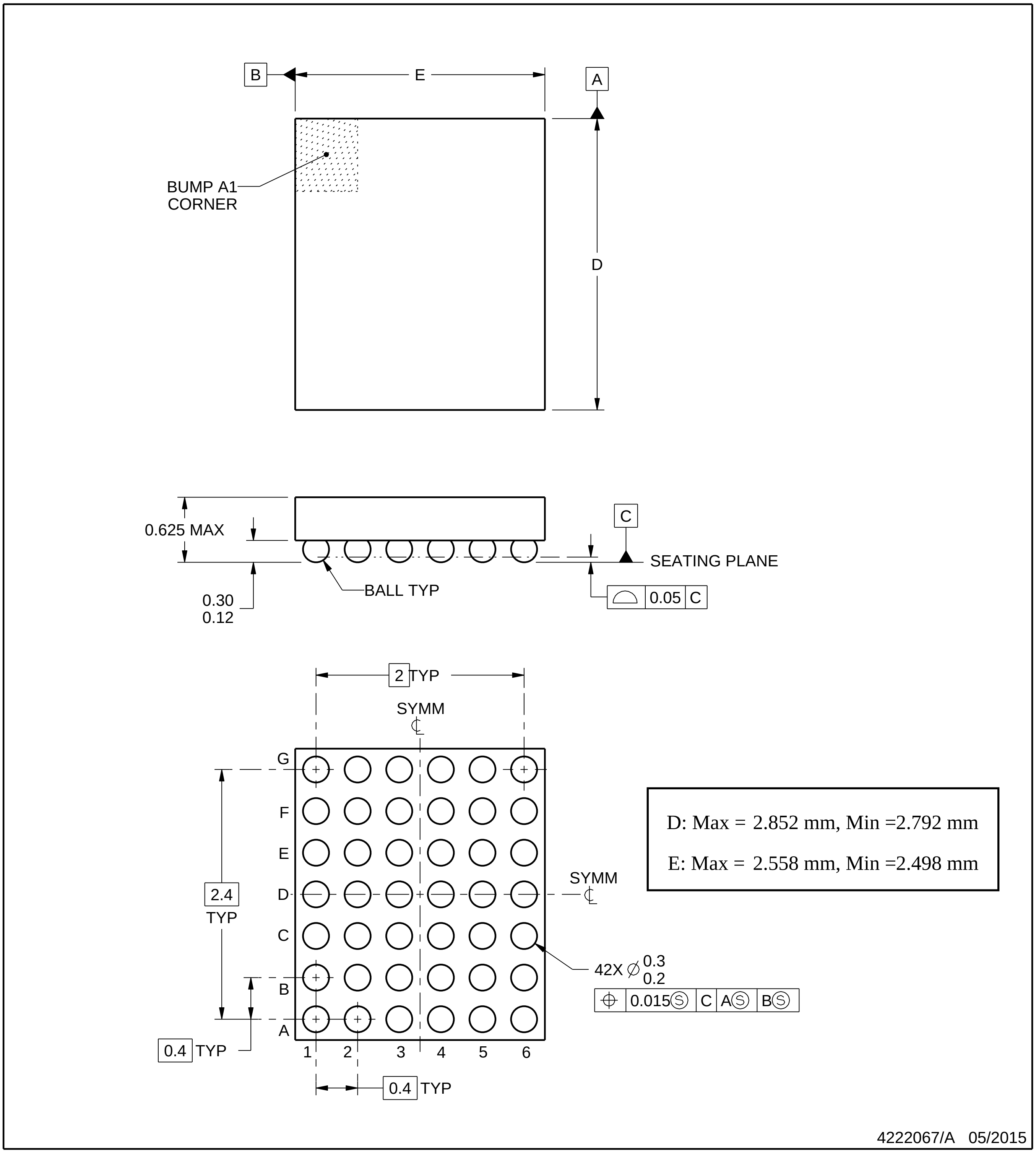
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

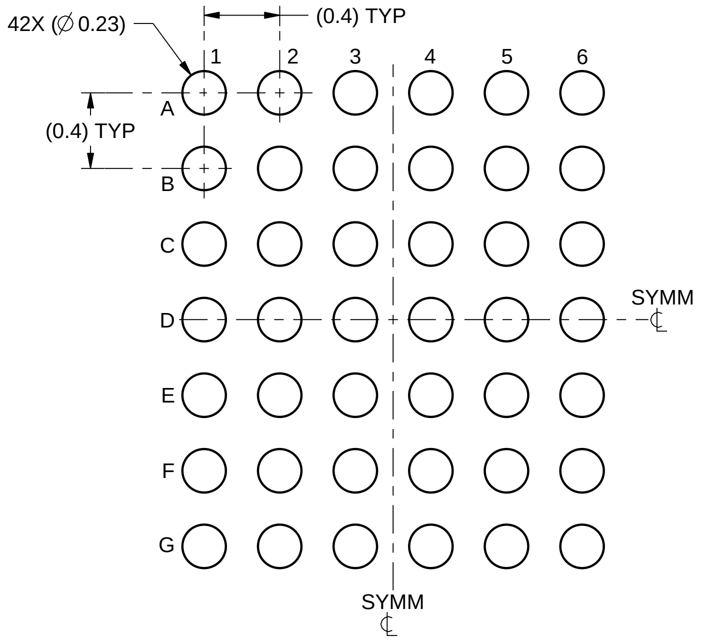
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25898CYFFR	DSBGA	YFF	42	3000	182.0	182.0	20.0
BQ25898CYFFT	DSBGA	YFF	42	250	182.0	182.0	20.0
BQ25898CYFFT	DSBGA	YFF	42	250	182.0	182.0	20.0



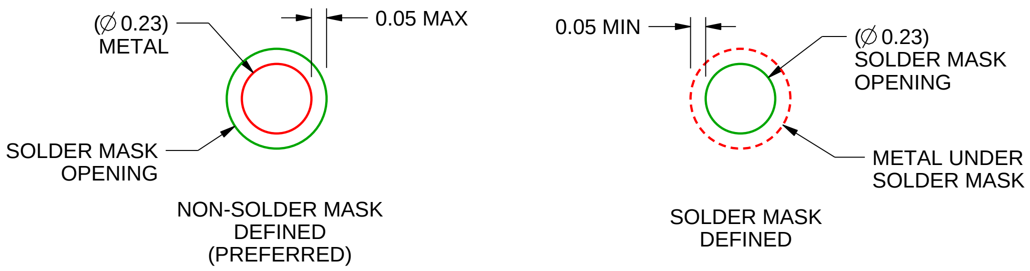


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X

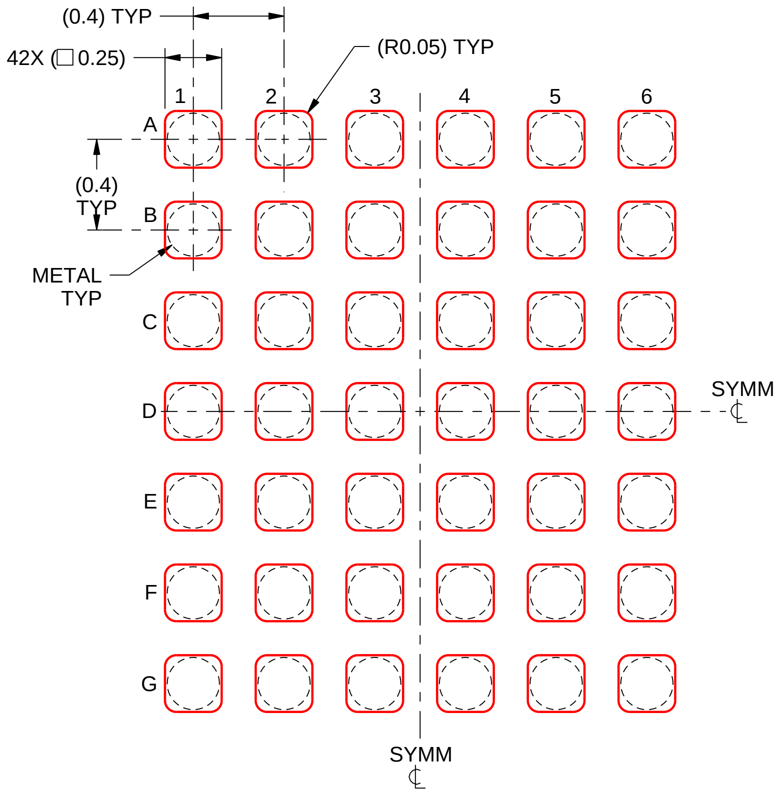


SOLDER MASK DETAILS
NOT TO SCALE

4222067/A 05/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222067/A 05/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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