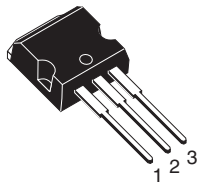
STI55NF03L

N-channel 30 V, 0.01 Ω, 55 A, I²PAK STripFET™ II Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STI55NF03L	30 V	< 0.013 Ω	55 A

- Optimized for high switching operation
- Low gate charge
- Logic level gate drive



I²PAK

Application

- Switching applications
  - Automotive

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps allowing remarkable manufacturing reproducibility.

Figure 1. Internal schematic diagram

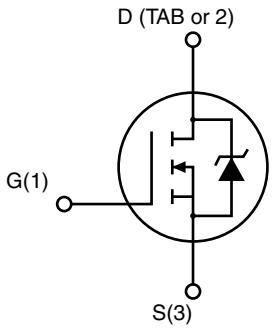


Table 1. Device summary

Order code	Marking	Package	Packaging
STI55NF03L	55NF03L	I²PAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	± 16	V
I_D	Drain current (continuous) at T_C = 25 °C	55	A
I_D	Drain current (continuous) at T_C = 100 °C	39	A
I_{DM} (1)	Drain current (pulsed)	220	A
P_{TOT}	Total dissipation at T_C = 25 °C	80	W
	Derating factor	0.53	W/°C
E_{AS} (2)	Single pulse avalanche energy	120	mJ
T_{stg}	Storage temperature	– 60 to 175	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2. Starting T_j = 25 °C, I_D= 32.5 A, V_{DD}= 45 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.875	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating,T_C=125 °C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.5		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 27.5 A V_{GS} = 4.5 V, I_D = 27.5 A		0.01 0.013	0.013 0.02	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		1265		pF
C_{oss}	Output capacitance			435		pF
C_{rss}	Reverse transfer capacitance			115		pF
Q_g	Total gate charge	V_{DD} = 24V, I_D = 55 A, V_{GS} = 4.5 V *(see Figure 14)*		20	27	nC
Q_{gs}	Gate-source charge			7		nC
Q_{gd}	Gate-drain charge			10		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 15 V, I_D = 27.5 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 13)*		28 400		ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time	V_{DD} = 15 V, I_D = 27.5 A R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 13)*		25 50		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				55	A
I_{SDM} (1)	Source-drain current (pulsed)				220	A
V_{SD} (2)	Forward on voltage	I_{SD} = 55 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 55 A, V_{DD} = 30 V di/dt = 100 A/µs, T_j = 150 °C *(see Figure 15)*		70 160 4.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

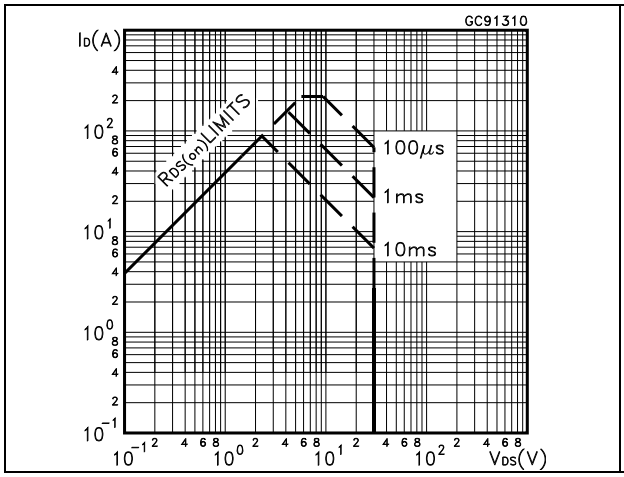


Figure 3. Thermal impedance

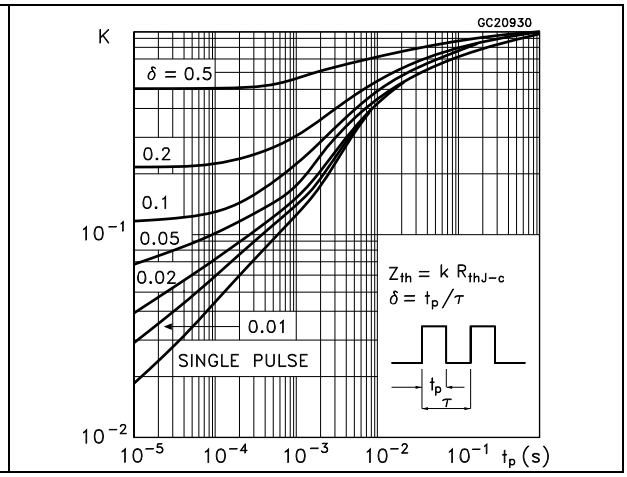


Figure 4. Output characteristics

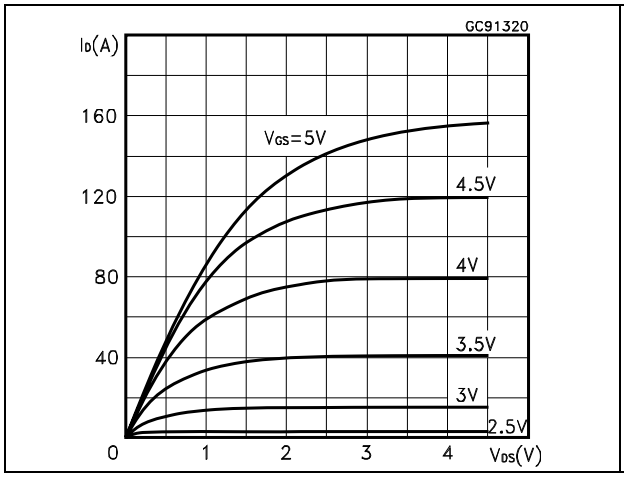


Figure 5. Transfer characteristics

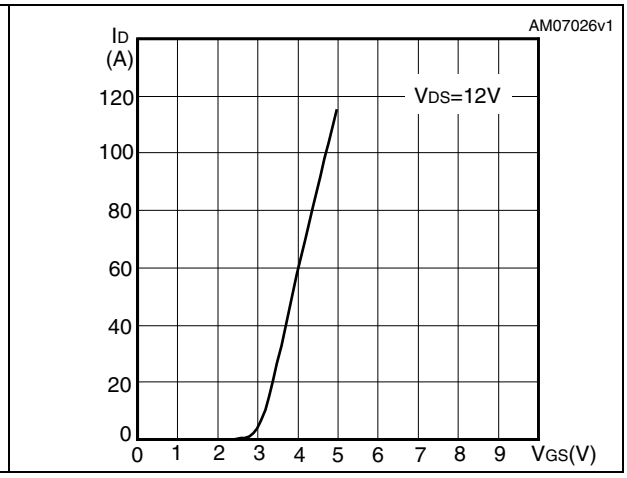


Figure 6. Normalized B_{VDSS} vs temperature

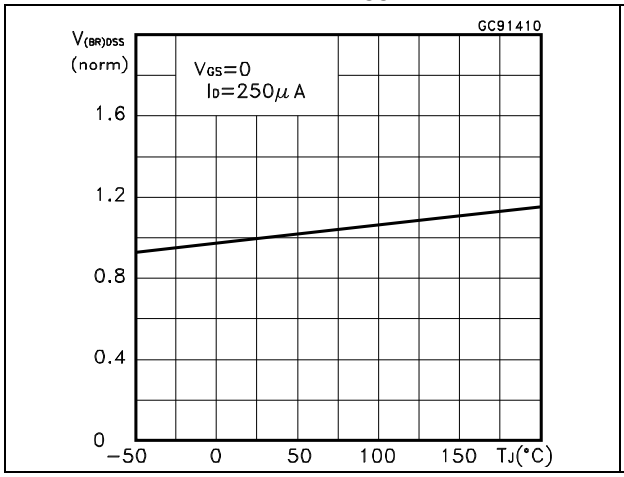


Figure 7. Static drain-source on resistance

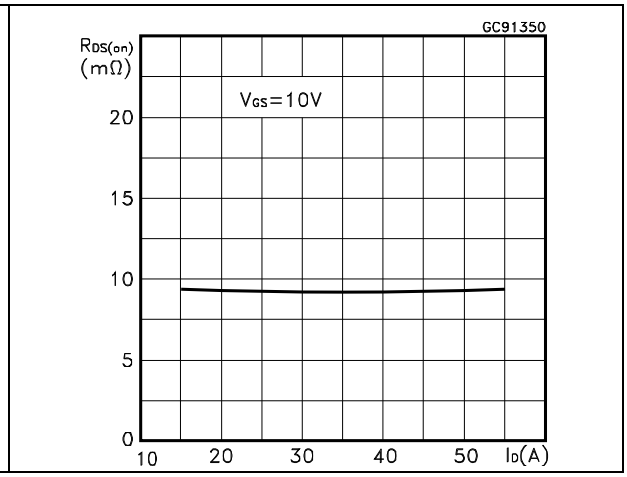


Figure 8. Gate charge vs gate-source voltage

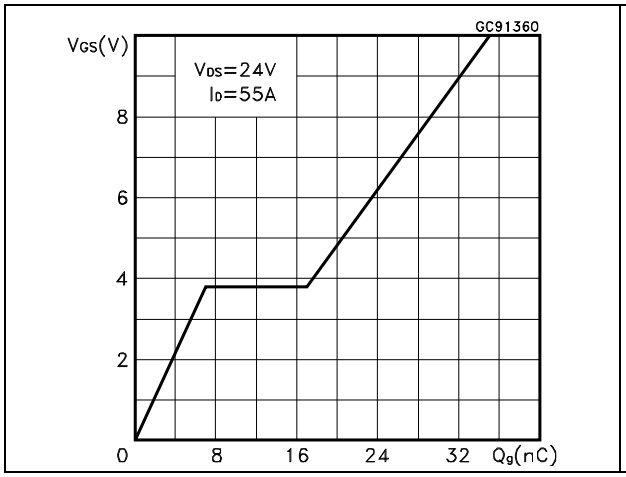


Figure 9. Capacitance variations

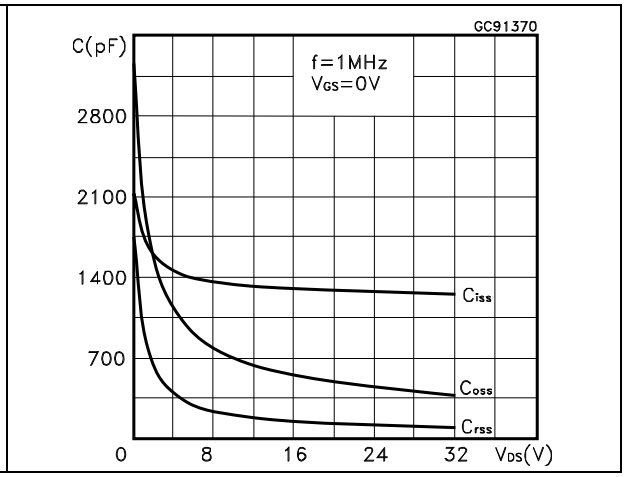


Figure 10. Normalized gate threshold voltage vs temperature

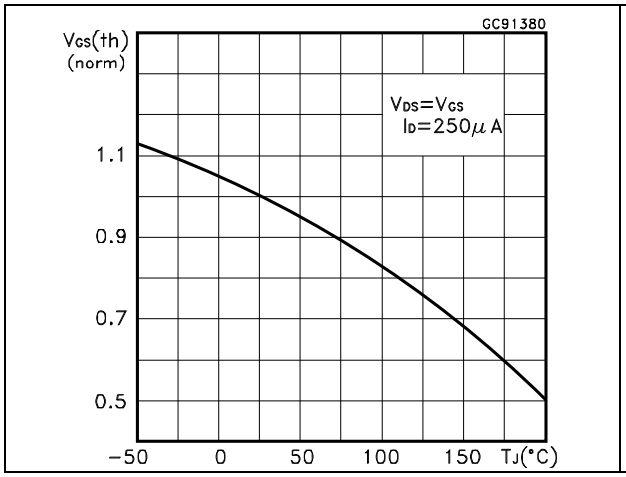


Figure 11. Normalized on resistance vs temperature

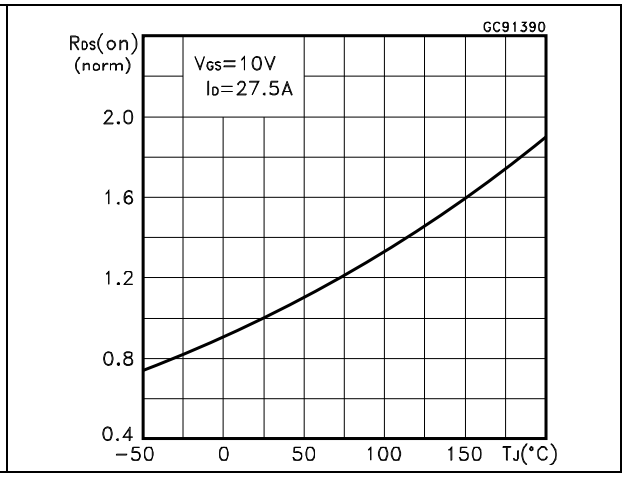
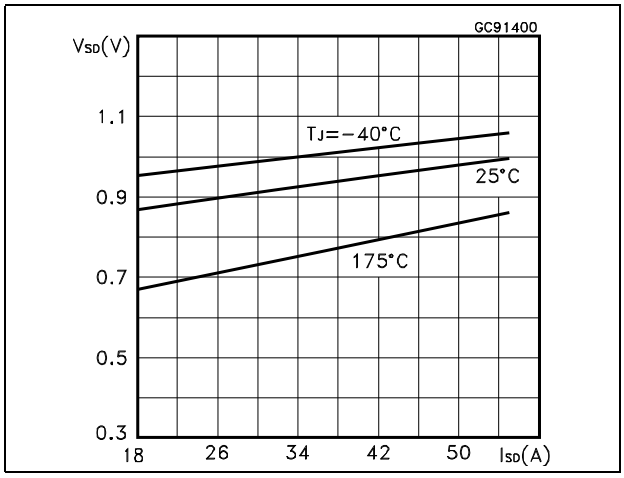


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

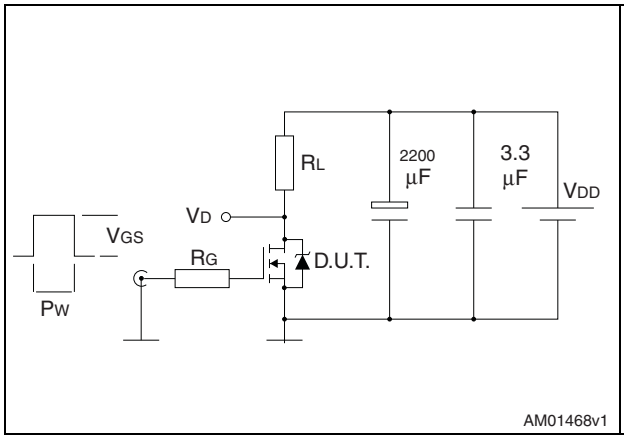


Figure 14. Gate charge test circuit

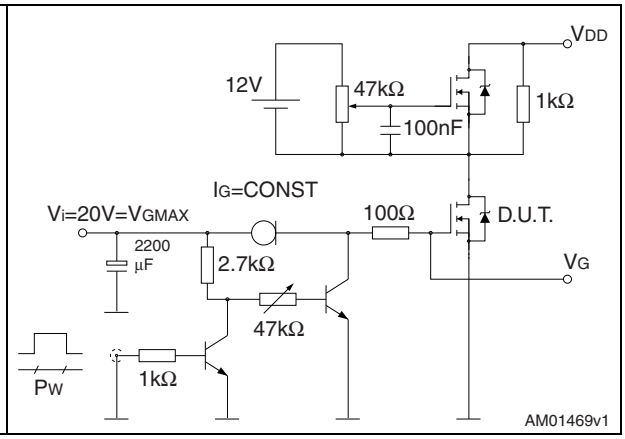


Figure 15. Test circuit for inductive load switching and diode recovery times

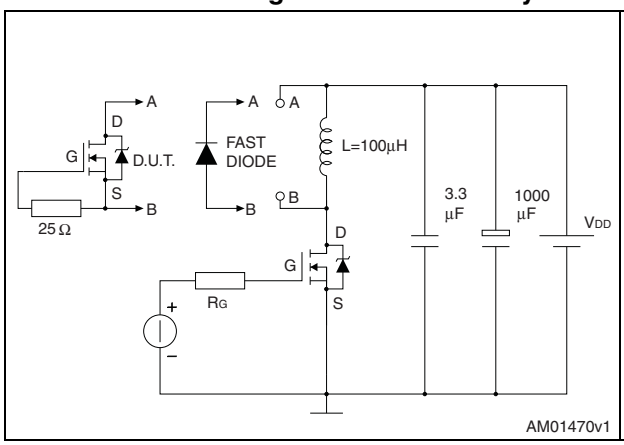


Figure 16. Unclamped inductive load test circuit

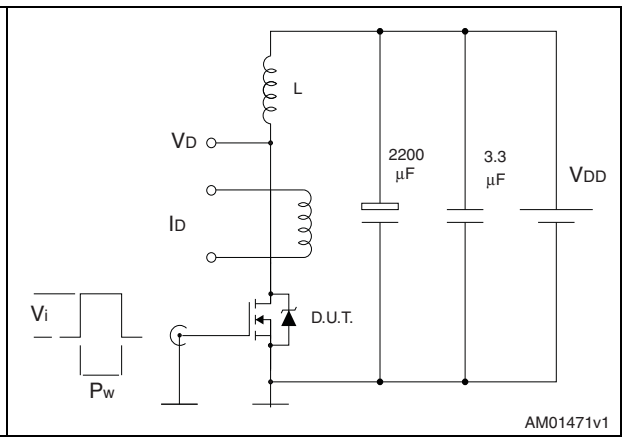


Figure 17. Unclamped inductive waveform

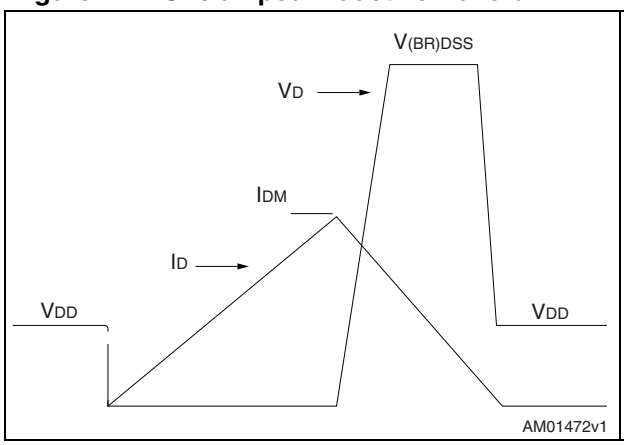
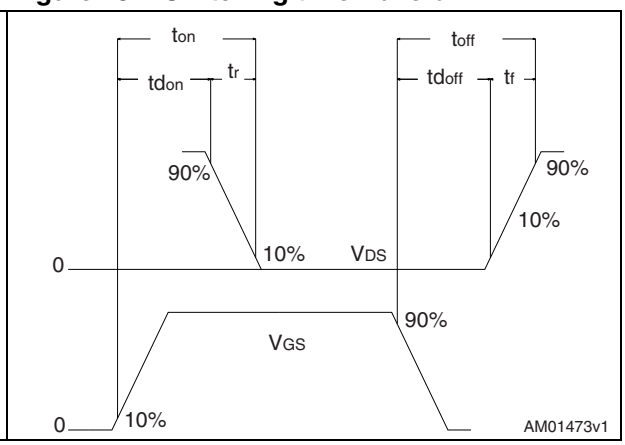


Figure 18. Switching time waveform



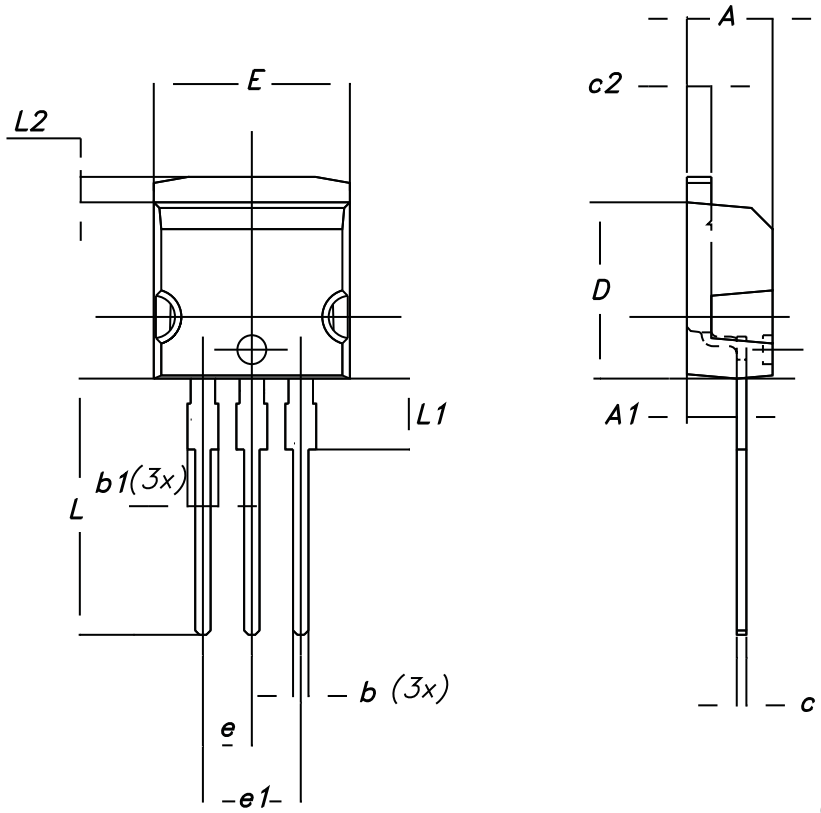
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 19. I²PAK (TO-262) drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
18-May-2011	1	First release

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