



TPS54202 4.5V 至 28V 输入、2A 输出、 同步降压转换器

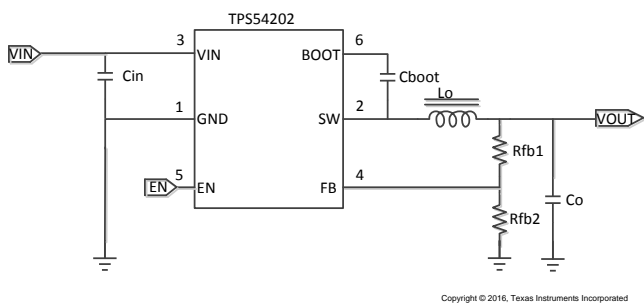
1 特性

- 4.5V 至 28V 的宽输入电压范围
- 集成 148mΩ 和 78 mΩ 金属氧化物半导体场效应晶体管 (MOSFET)，持续输出电流为 2A
- 关断电流低至 2μA，静态电流为 45μA
- 内部 5ms 软启动
- 500kHz 固定开关频率
- 高级 Eco-mode™ 脉冲跳跃
- 峰值电流模式控制
- 内部回路补偿
- 采用断续模式为两个 MOSFET 提供过流保护
- 过压保护
- 热关断
- 小外形尺寸晶体管 (SOT)-23 (6) 封装

2 应用

- 12V 和 24V 分布式电源总线供电
- 工业应用
 - 白色家电
- 消费类应用
 - 音频
 - 机顶盒 (STB)、数字电视 (DTV)
 - 打印机

简化电路原理图



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3 说明

TPS54202 是一款输入电压范围为 4.5V 至 28V 的 2A 同步降压转换器。该器件包含两个集成式开关场效应晶体管 (FET) 并且具备内部回路补偿和 5ms 内部软启动功能，可降低组件数。

通过集成 MOSFET 并采用 SOT-23 封装，TPS54202 获得了高功率密度，并且在印刷电路板 (PCB) 上的占用空间非常小。

高级 Eco-mode 实现可最大限度地提高轻负载效率并降低功率损耗。

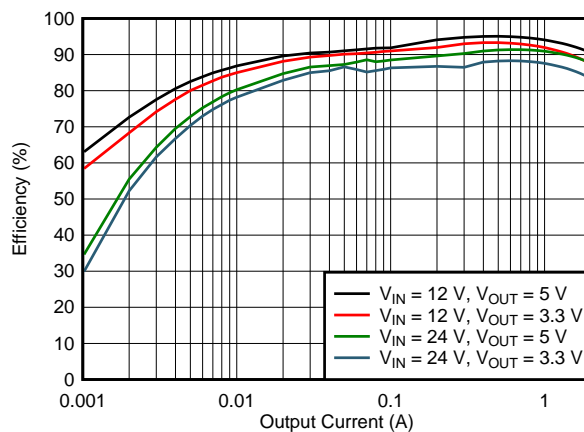
高侧 MOSFET 上的逐周期电流限制功能可在过载条件下保护转换器并通过防止电流失控的低侧 MOSFET 续流电流限制功能实现功能增强。当过流持续时间超出预设时间时，将触发断续模式保护功能。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS54202	SOT-23 (6)	1.60mm x 2.90mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

效率与输出电流间的关系



D100



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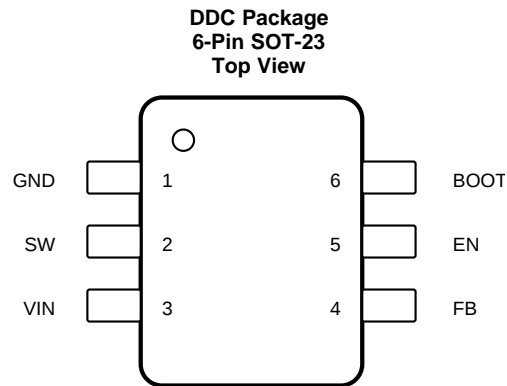
4 修订历史记录

Changes from Original (April 2016) to Revision A

Page

• Added Note 1 to Table 2	15
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5 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
BOOT	6	O	Supply input for the high-side NFET gate drive circuit. Connect a 0.1-μF capacitor between BOOT and SW pins.
EN	5	I	This pin is the enable pin. Float the EN pin to .
FB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
GND	1	–	Ground pin. Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	–	Input voltage supply pin. The drain terminal of high-side power NFET.

(1) O = Output; I = Input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage range, V_I	VIN	−0.3	30	V
	EN	−0.3	7	V
	FB	−0.3	7	V
Output voltage range, V_O	BOOT-SW	−0.3	7	V
	SW	−0.3	30	V
	SW (20 ns transient)	−5	30	V
Operating junction temperature, T_J		−40	150	°C
Storage temperature range, T_{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I Input voltage range	VIN	4.5	28	V
	EN	−0.1	7	V
	FB	−0.1	7	V
V_O Output voltage range	BOOT-SW	−0.1	7	V
	SW	−0.1	28	V
T_J Operating junction temperature		−40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS54202	UNIT
		DDC (SOT23)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report, .

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = 4.5\text{ V}$ to 28 V , (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		4.5		28	V
I_Q	Non switching quiescent current	$EN = 5\text{ V}$, $V_{FB} = 1\text{ V}$		45		μA
I_{OFF}	Shut down current	$EN = \text{GND}$		2		μA
$V_{IN(UVLO)}$	VIN under voltage lockout	Rising V_{IN}	3.9	4.2	4.4	V
		Falling V_{IN}	3.4	3.7	3.9	V
	Hysteresis		400	480	560	mV
ENABLE (EN PIN)						
$V_{(EN_RISING)}$	Enable threshold	Rising				V
$V_{(EN_FALLING)}$		Falling				V
$I_{(EN_HYS)}$	Hysteresis current	$V_{EN} = 1.5\text{ V}$				μA
FEEDBACK AND ERROR AMPLIFIER						
V_{FB}	Feedback Voltage	$V_{IN} = 12\text{ V}$	0.581	0.596	0.611	V
PULSE SKIP MODE						
$I_{(SKIP)}^{(1)}$	Pulse skip mode peak inductor current threshold	$V_{IN} = 24\text{ V}$, $V_{OUT} = 5\text{ V}$, $L = 15\text{ }\mu\text{H}$		300		mA
POWER STAGE						
$R_{(HSD)}$	High-side FET on resistance	$T_A = 25^{\circ}\text{C}$, $V_{BST} - SW = 6\text{ V}$		148		$\text{m}\Omega$
$R_{(LSD)}$	Low-side FET on resistance	$T_A = 25^{\circ}\text{C}$, $V_{IN} = 12$		78		$\text{m}\Omega$
CURRENT LIMIT						
$I_{(LIM_HS)}$	High side current limit		2.5	3.2	3.9	A
$I_{(LIM_LS)}$	Low side source current limit		2	3	4	A
OSCILLATOR						
F_{sw}	Centre switching frequency		390	500	590	kHz
OVER TEMPERATURE PROTECTION						
Thermal Shutdown ⁽¹⁾	Rising temperature			155		$^{\circ}\text{C}$
	Hysteresis			10		$^{\circ}\text{C}$
	Hiccup time			32768		Cycles

(1) Not production tested

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
OVER CURRENT PROTECTION					
t_{HIC_WAIT}	Hiccup up wait time		512		Cycles
$t_{HIC_RESTART}$	Hiccup up time before restart		16384		Cycles
t_{SS}	Soft-start time		5		mS
ON TIME CONTROL					
$t_{MIN_ON}^{(1)}$	Minimum on time, measured at 90% to 90% and 1-A loading		110		ns

(1) Not production tested

6.7 Typical Characteristics

$V_{IN} = 12$, unless otherwise specified

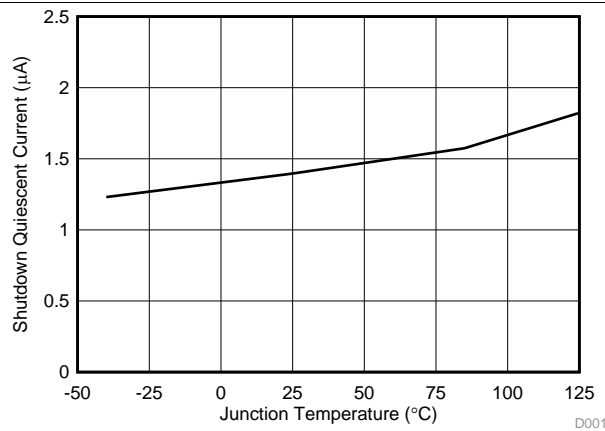


Figure 1. Shutdown Quiescent Current vs Junction Temperature

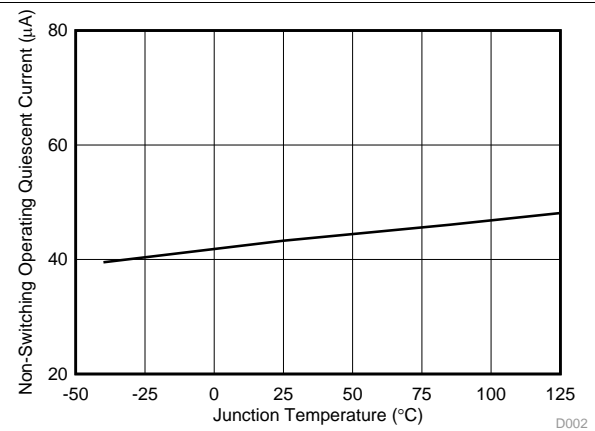


Figure 2. Non-Switching Operating Quiescent Current vs Junction Temperature

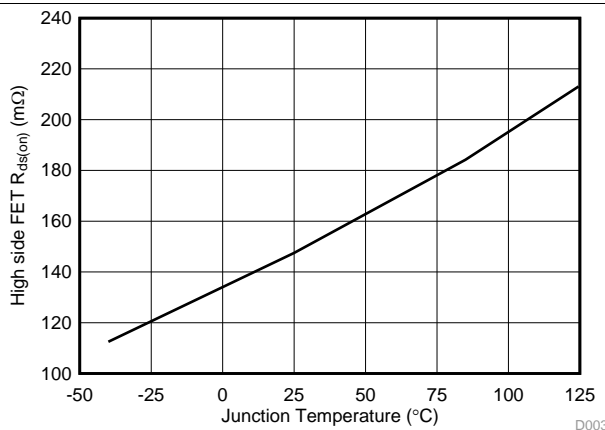


Figure 3. High-Side Resistance vs Junction Temperature

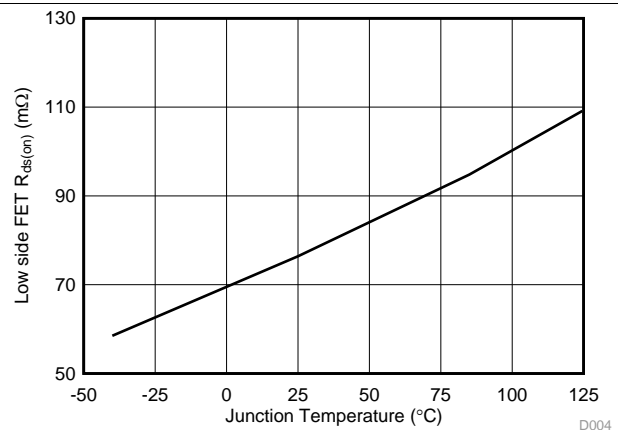


Figure 4. Low-Side FET On Resistance vs Junction Temperature

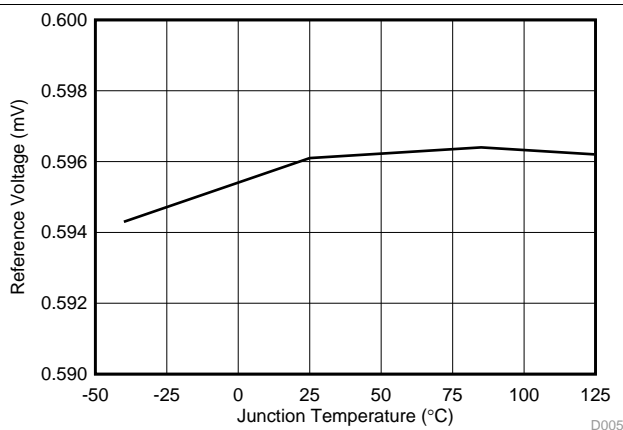


Figure 5. Reference Voltage vs Junction Temperature

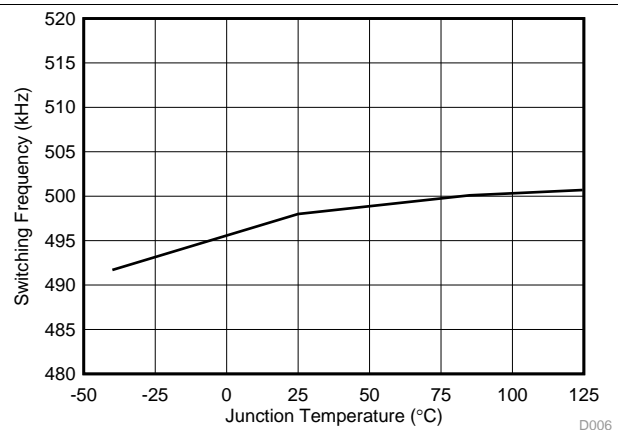


Figure 6. Centre Switching Frequency vs Junction Temperature

Typical Characteristics (continued)

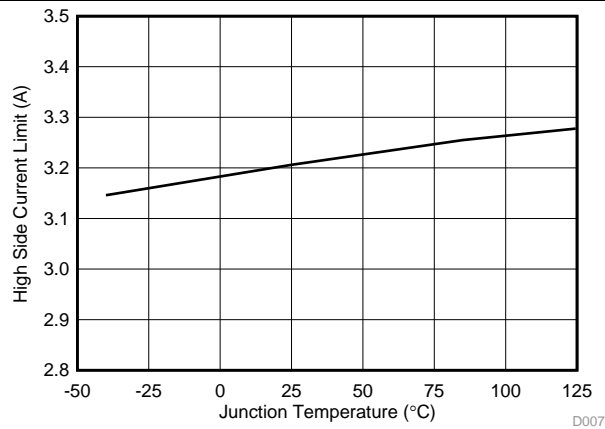


Figure 7. High-Side Current Limit Threshold vs Junction Temperature

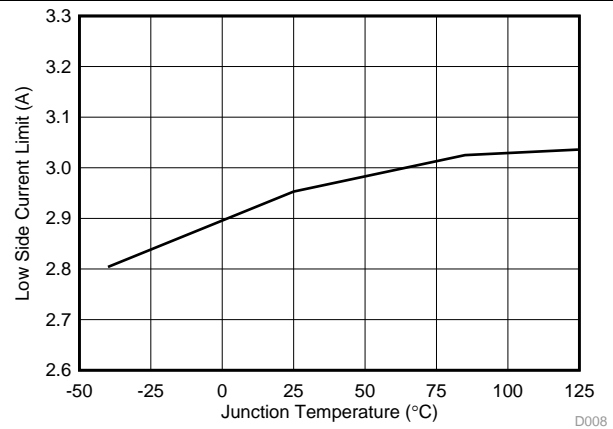


Figure 8. Low-Side Current Limit Threshold vs Junction Temperature

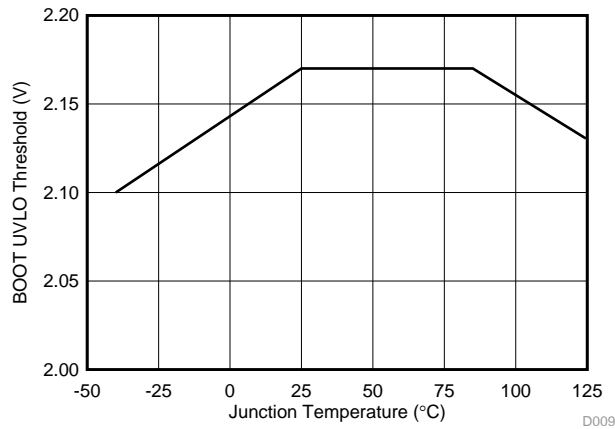


Figure 9. BOOT-SW UVLO Threshold vs Junction Temperature

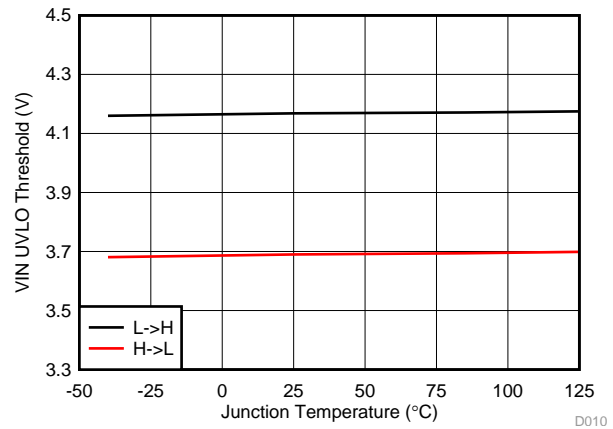


Figure 10. VIN UVLO Threshold vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS54202 device is a 28-V, 2-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant-frequency, peak current mode control which reduces output capacitance. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

The switching frequency is fixed to 500 kHz.

The device begins switching at VIN equal to 4.5 V. The operating current is 45 μ A typically when not switching and under no load. When the device is disabled, the supply current is 2 μ A typically.

The integrated 148-m Ω high-side MOSFET and 78-m Ω allow for high efficiency power supply designs with continuous output currents up to 2 A.

The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically.

The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 108% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 104%.

The device has internal 5-ms soft-start time to minimize inrush currents.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the error amplifier output voltage level, the high side power switch is turned off and the low-side power switch is turned on. The error amplifier output voltage increases and decreases as the output current increases and decreases. The device implements a current-limit by clamping the error amplifier voltage to a maximum level and also implements a minimum clamp for improved transient-response performance.

7.3.2 Pulse Skip Mode

The TPS54202 is designed to operate in pulse skipping mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 300 mA typically, the device enters pulse skipping mode. When the device is in pulse skipping mode, the error amplifier output voltage is clamped which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 300 mA and exit pulse skip mode. Since the integrated current comparator catches the peak inductor current only, the average load current entering pulse skipping mode varies with the applications and external output filters.

7.3.3 Error Amplifier

The device has a trans-conductance amplifier as the error amplifier. The error amplifier compares the FB voltage to the lower of the internal soft-start voltage or the internal -V voltage reference. The transconductance of the error amplifier is 240 μ A/V typically. The frequency compensation components are placed internal between the output of the error amplifier and ground.

Feature Description (continued)

7.3.4 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents sub-harmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

7.3.5 Safe Startup into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than FB pin voltage.

7.3.6 Voltage Reference

The voltage reference system produces a precise $\pm 2.5\%$ voltage-reference over temperature by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.596 V.

7.3.7 Adjusting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 100 k Ω for the upper resistor divider, use [Equation 1](#) to calculate the output voltage. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$$V_{OUT} = V_{ref} \times \left[\frac{R2}{R3} + 1 \right] \quad (1)$$

7.3.8 Internal Soft-Start

The TPS54202 device uses the internal soft-start function. The internal soft start time is set to 5 ms typically.

7.3.9 Bootstrap Voltage (BOOT)

The TPS54202 has an integrated boot regulator and requires a 0.1- μ F ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V typically.

7.3.10 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

7.3.10.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the internal COMP voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off.

7.3.11 Output Overvoltage Protection (OVP)

The TPS54202 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the FB pin voltage and internal thresholds. When the FB pin voltage goes above $108\% \times V_{ref}$, the high-side MOSFET will be forced off. When the FB pin voltage falls below $104\% \times V_{ref}$, the high-side MOSFET will be enabled again.

Feature Description (continued)

7.3.12 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 145°C typically, the internal thermal-hiccup timer begins to count. The device reinitiates the power-up sequence after the built-in thermal-shutdown hiccup time (32768 cycles) is over.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold, the TPS54202 can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when inductor peak current is above 0 A. In CCM, the device operates at a fixed frequency.

7.4.2 Eco-mode™ Operation

The devices are designed to operate in high-efficiency pulse-skipping mode under light load conditions. Pulse skipping initiates when the switch current falls to 0 A. During pulse skipping, the low-side FET turns off when the switch current falls to 0 A. The switching node (the SW pin) waveform takes on the characteristics of discontinuous conduction mode (DCM) operation and the apparent switching frequency decreases. As the output current decreases, the perceived time between switching pulses increases.

8 Application and Implementation

NOTE

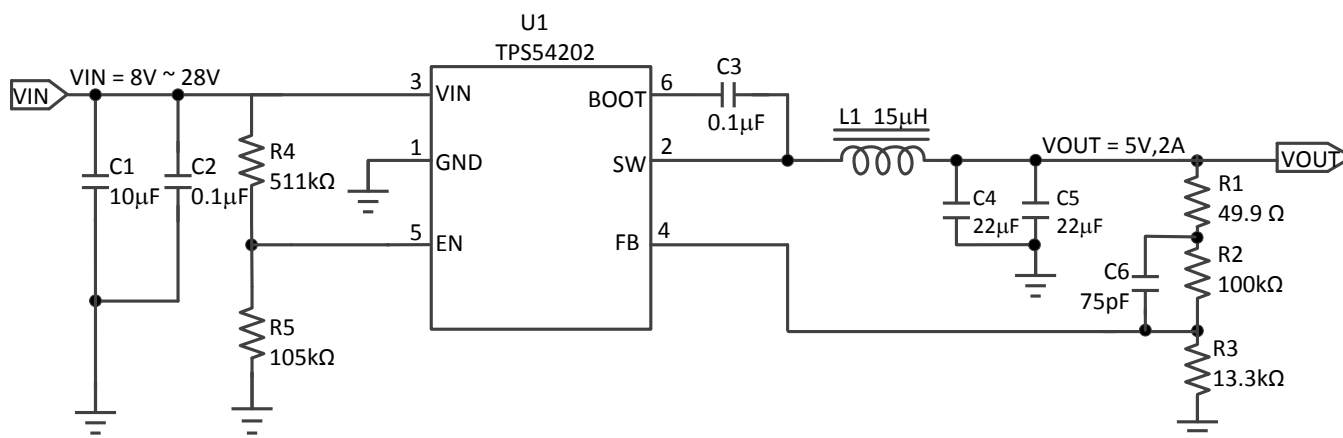
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54202 device is typically used as a step down converter, which convert an input voltage from 8 V to 28 V to fixed output voltage 5 V.

8.2 Typical Application

8.2.1 TPS54202 8-V to 28-V Input, 5-V Output Converter



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Figure 11. 5-V, 2-A Reference Design

8.2.2 Design Requirements

For this design example, use the parameters in [Table 1](#).

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range	V to 28 V
Output voltage	5 V
Output current	2 A
Transient response, 1.5 A load step	$\Delta V_{OUT} = \pm 5\%$
Input ripple voltage	400 mV
Output voltage ripple	30 mVpp
Switching frequency	500 kHz

8.2.3 Detailed Design Procedure

8.2.3.1 Input Capacitor Selection

The device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor (C2) from VIN to GND is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Use Equation 2 to calculate the input ripple voltage (ΔV_{IN}).

$$\Delta V_{\text{IN}} = \frac{I_{\text{OUT(MAX)}} \times 0.25}{C_{\text{BULK}} \times f_{\text{SW}}} + (I_{\text{OUT(MAX)}} \times \text{ESR}_{\text{MAX}})$$

where:

- C_{BULK} is the bulk capacitor value
 - f_{SW} is the switching frequency
 - $I_{\text{OUT(MAX)}}$ is the maximum loading current
 - ESR_{MAX} is maximum series resistance of the bulk capacitor
- (2)

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use Equation 3 to calculate $I_{\text{CIN(RMS)}}$.

$$I_{\text{CIN(RMS)}} = \frac{I_{\text{OUT(MAX)}}}{2}$$
(3)

The actual input-voltage ripple is greatly affected by parasitic associated with the layout and the output impedance of the voltage source. Design Requirements show the actual input voltage ripple for this circuit which is larger than the calculated value. This measured value is still below the specified input limit of 400 mV. The maximum voltage across the input capacitors is $V_{\text{IN (MAX)}} + \Delta V_{\text{IN}}/2$. The selected bypass capacitor is rated for 35 V and the ripple current capacity is greater than 2 A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

8.2.3.2 Bootstrap Capacitor Selection

A 0.1 μF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.3.3 Output Voltage Set Point

The output voltage of the TPS54202 device is externally adjustable using a resistor divider network. In the application circuit of , this divider network is comprised of R2 and R3. Use Equation 4 and Equation 5 to calculate the relationship of the output voltage to the resistor divider.

$$R3 = \frac{R2 \times V_{\text{ref}}}{V_{\text{OUT}} - V_{\text{ref}}}$$
(4)

$$V_{\text{OUT}} = V_{\text{ref}} \times \left[\frac{R2}{R3} + 1 \right]$$
(5)

Select a value of R2 to be approximately 100 k Ω . Slightly increasing or decreasing R3 can result in closer output voltage matching when using standard value resistors. In this design, $R2 = 100 \text{ k}\Omega$ and $R3 = 13.3 \text{ k}\Omega$ which results in a 5-V output voltage. The 49.9- Ω resistor, R1, is provided as a convenient location to break the control loop for stability testing.

8.2.3.4 Output Filter Components

Two components must be selected for the output filter, the output inductor (L_O) and C_O .

8.2.3.4.1 Inductor Selection

Use Equation 6 to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (6)$$

Where:

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

In general, the value of K_{IND} is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors, such as ceramics, a value as high as $K_{IND} = 0.3$ can be used. When using higher ESR output capacitors, $K_{IND} = 0.2$ yields better results.

For this design example, use $K_{IND} = 0.3$. The minimum inductor value is calculated as 13.7 μ H. For this design, a close standard value of 15 μ H was selected for L_{MIN} .

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use Equation 7 to calculate the RMS inductor current ($I_{L(RMS)}$).

$$I_{L(MAX)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_O \times f_{SW} \times 0.8} \right)^2} \quad (7)$$

Use Equation 8 to calculate the peak inductor current ($I_{L(PK)}$).

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{1.6 \times V_{IN(MAX)} \times L_O \times f_{SW}} \quad (8)$$

Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple.

8.2.3.4.2 Output Capacitor Selection

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Use Equation 9 to calculate the minimum required output capacitance.

$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

where:

- ΔI_{OUT} is the change in output current
 - f_{SW} is the switching frequency of the regulator
 - ΔV_{OUT} is the allowable change in the output voltage
- (9)

For this example, the transient load response is specified as a 5% change in the output voltage, V_{OUT} , for a load step of 1.5 A. For this example, $\Delta I_{OUT} = 1.5$ A and $\Delta V_{OUT} = 0.05 \times 5 = 0.25$ V. Using these values results in a minimum capacitance of 24 μ F. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

[Equation 10](#) calculates the minimum output capacitance required to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, [Equation 10](#) yields 4.56 μ F.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{ripple}}}$$

where:

- f_{SW} is the switching frequency
 - $V_{(OUTripple)}$ is the maximum allowable output voltage ripple
 - $I_{(ripple)}$ is the inductor ripple current
- (10)

Use [Equation 11](#) to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. [Equation 11](#) indicates the ESR should be less than 54.8 m Ω . In this case, the ESR of the ceramic capacitor is much smaller than 54.8 m Ω .

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}}$$
(11)

The output capacitor can affect the crossover frequency f_o . Considering to the loop stability and effect of the internal parasitic parameters, choose the crossover frequency less than 40 kHz without considering the feed forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor C6 is shown in [Equation 12](#), assuming C_{OUT} has small ESR.

$$f_o = \frac{3.95}{V_{OUT} \times C_{OUT}}$$
(12)

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, two 22- μ F 25-V, X7R ceramic capacitors are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use [Equation 13](#) to calculate the RMS ripple current that the output capacitor must support. For this application, [Equation 13](#) yields 79 mA for each capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_O \times f_{SW} \times N_C} \right)$$
(13)

8.2.3.4.3 Feed-Forward Capacitor

The TPS54202 device is internally compensated and the internal compensation network is composed of two capacitors and one resistor shown on the block diagram. Depending on the V_{OUT} , if the output capacitor C_{OUT} is dominated by low ESR (ceramic types) capacitors, it could result in low phase margin. To improve the phase boost an external feedforward capacitor C6 can be added in parallel with R2. C6 is chosen such that phase margin is boosted at the crossover frequency.

Equation 14 for C6 was tested:

$$C6 = \frac{1}{2\pi f_o} \times \frac{1}{R2} \quad (14)$$

For this design, $C6 = 75$ pF. C6 is not needed when C_{OUT} has high ESR, and C6 calculated from Equation 14 should be reduced with medium ESR. Table 2 can be used as a starting point.

Table 2. Recommended Component Values

V_{OUT} (V)	L (μH) ⁽¹⁾	C_{OUT} (μF)	R2 (kΩ)	R3 (kΩ)	C6 (pF)
1.8	5.6	66	100	49.9	47
2.5	8.2	44	100	31.6	33
3.3	10	44	100	22.1	56
5	15	44	100	13.3	75
12	22	44	100	5.23	100

(1) Based on $V_{IN} = 28$ V

8.2.4 Application Curves

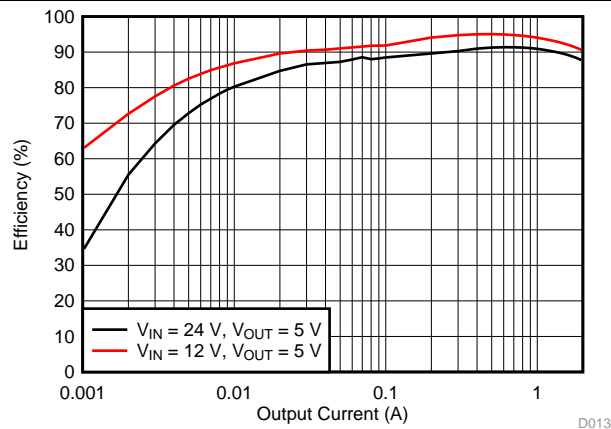


Figure 12. Efficiency

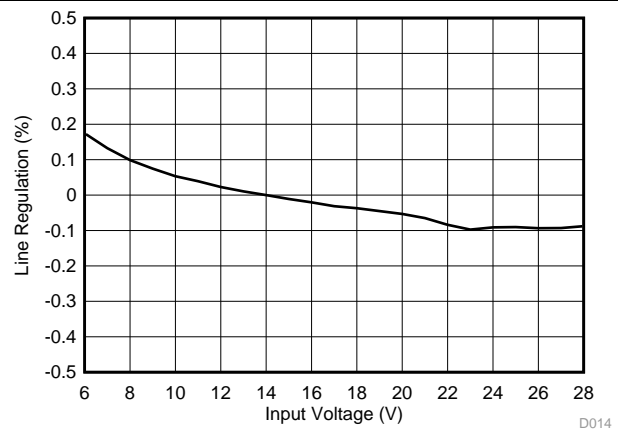


Figure 13. Line Regulation

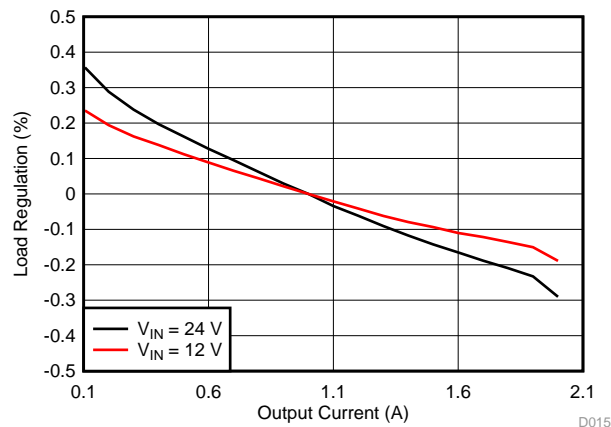


Figure 14. Load Regulation

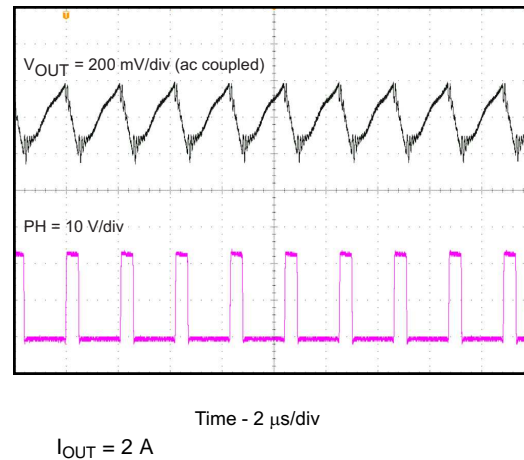


Figure 15. Input Voltage Ripple

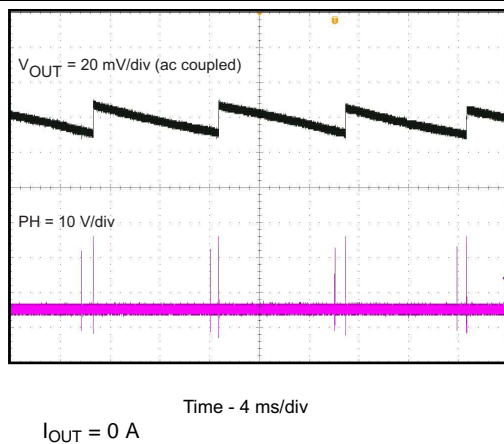


Figure 16. Output Voltage Ripple

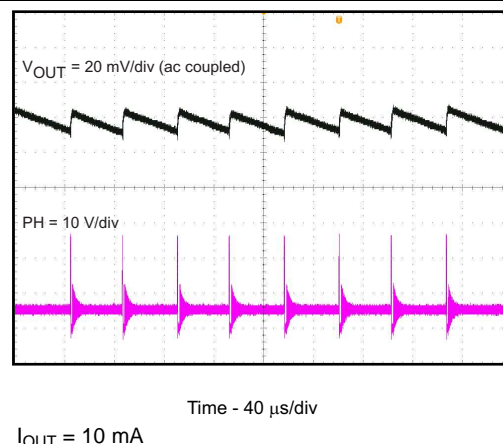
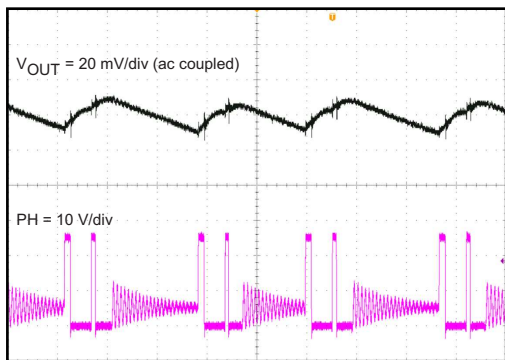
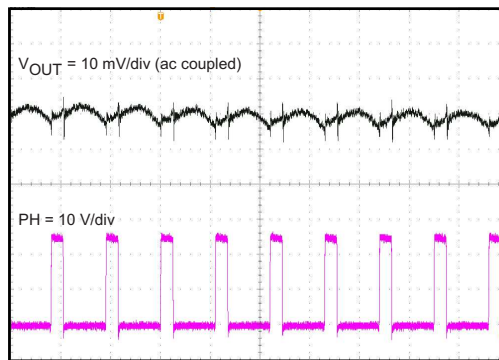


Figure 17. Output Voltage Ripple



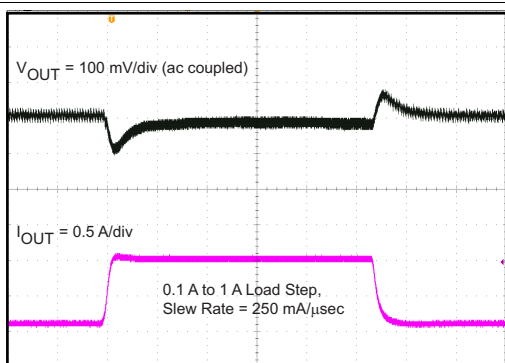
Time - 4 μ s/div
 $I_{OUT} = 100$ mA

Figure 18. Output Voltage Ripple



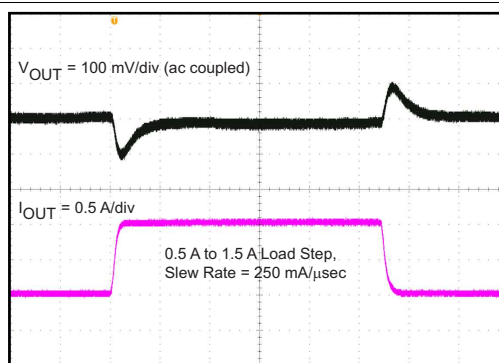
Time - 2 μ s/div
 $I_{OUT} = 2$ A

Figure 19. Output Voltage Ripple



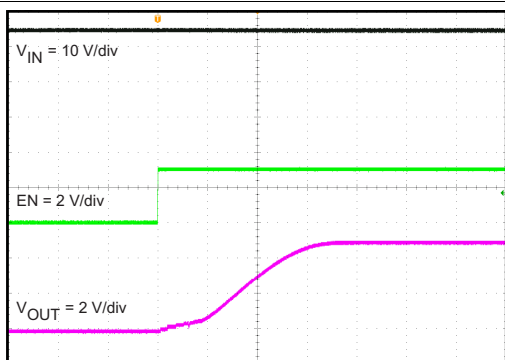
Time - 200 μ s/div
0.1 to 1 A

Figure 20. Transient Response



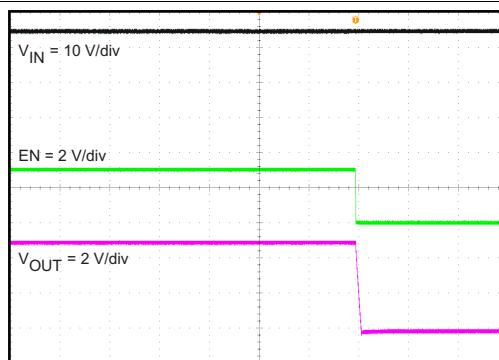
Time - 200 μ s/div
0.5 to 1.5 A

Figure 21. Transient Response



Time - 2 ms/div

Figure 22. Start-Up Relative to EN



Time - 2 ms/div

Figure 23. Shutdown Relative to EN

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 μ F is a typical choice.

10 Layout

10.1 Layout Guidelines

- VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- A separate VOUT path should be connected to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the VFB node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

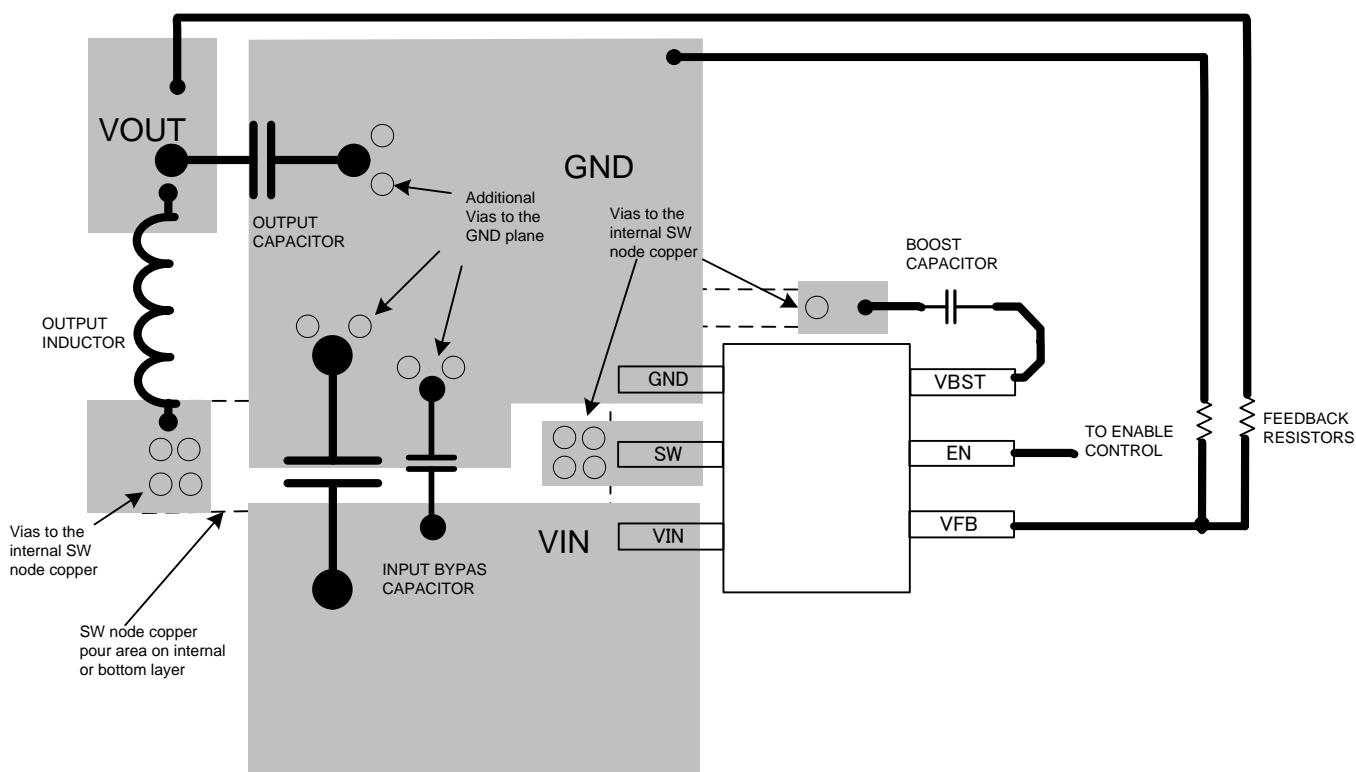


Figure 24. Board Layout

11 器件和文档支持

11.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54202DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	4202	Samples
TPS54202DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	4202	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

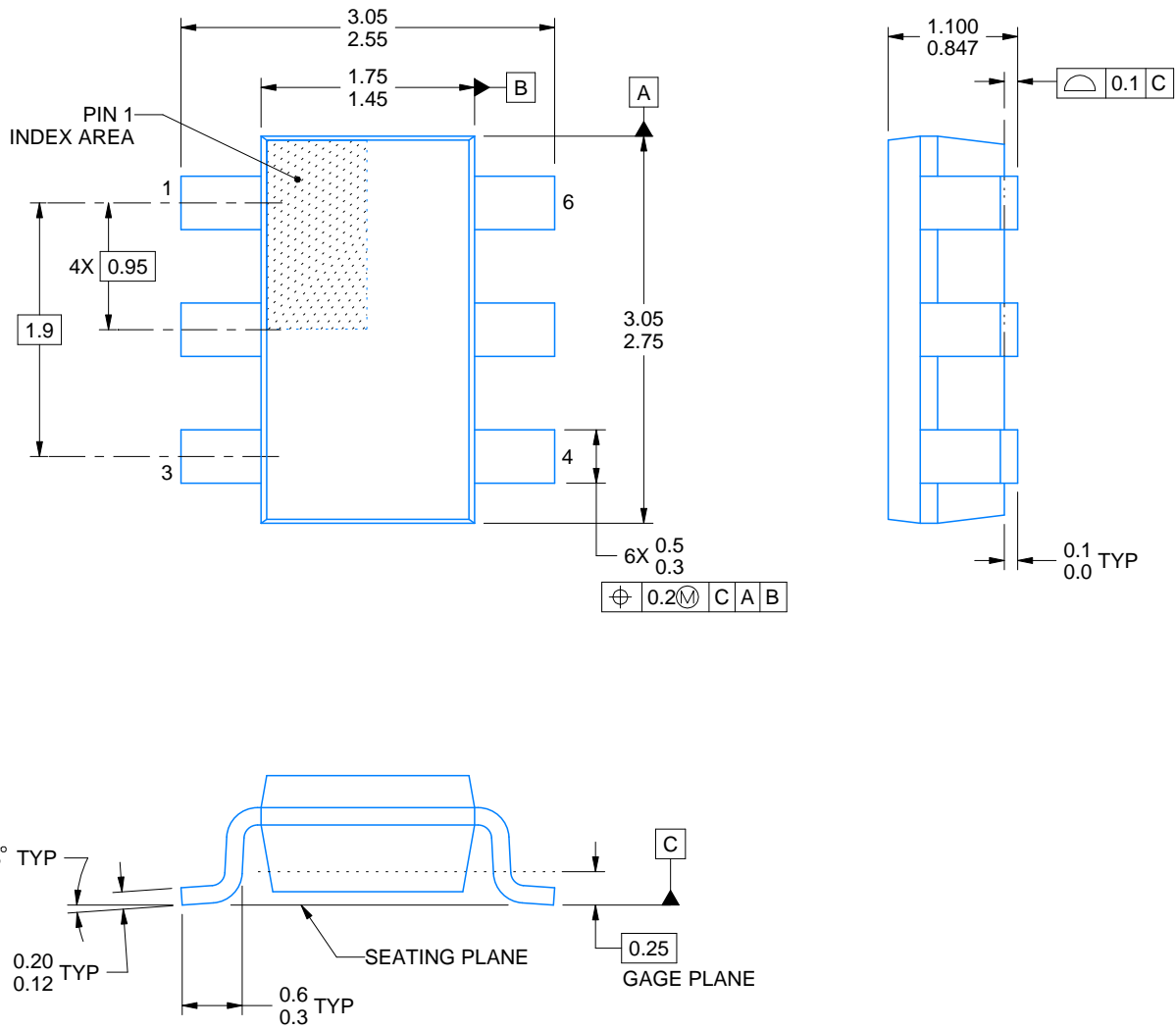
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54202DDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS54202DDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS54202DDCT	SOT-23-THIN	DDC	6	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS54202DDCT	SOT-23-THIN	DDC	6	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

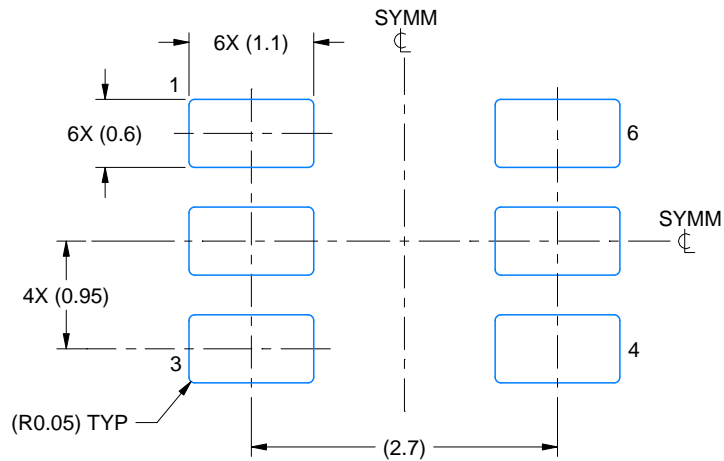
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54202DDCR	SOT-23-THIN	DDC	6	3000	184.0	184.0	19.0
TPS54202DDCR	SOT-23-THIN	DDC	6	3000	184.0	184.0	19.0
TPS54202DDCT	SOT-23-THIN	DDC	6	250	184.0	184.0	19.0
TPS54202DDCT	SOT-23-THIN	DDC	6	250	184.0	184.0	19.0



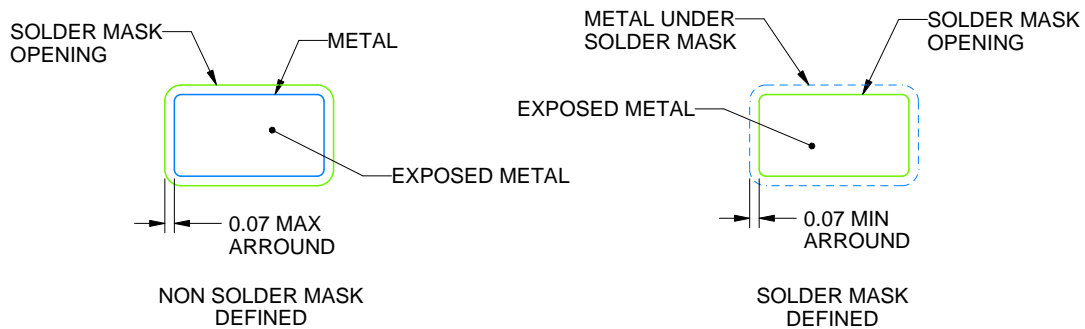
4214841/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X

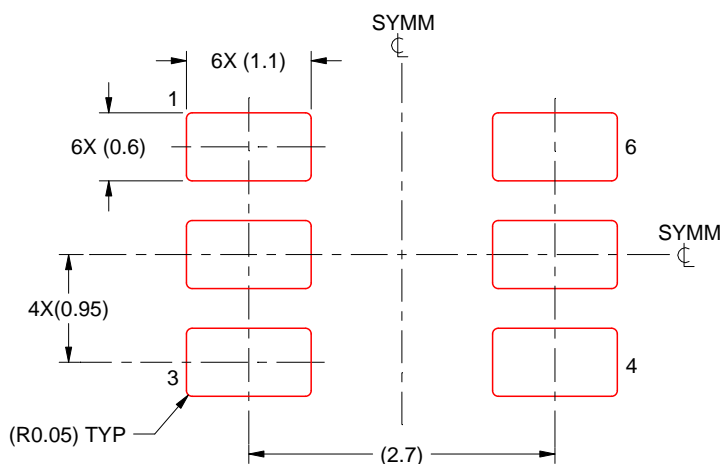


SOLDERMASK DETAILS

4214841/B 11/2020

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:15X

4214841/B 11/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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