TPS53659 Dual-Channel (4-Phase + 1-Phase) or (3-Phase + 2-Phase) D-CAP+™ Step-Down Multiphase Controller with NVM and PMBus™ for VR13 Server Memory

1 Device Overview

1.1 Features

- Full VR13 Server Feature Set Including Digital Input Power Monitor
- Programmable Loop Compensations
- Configurable with Non-Volatile Memory (NVM) for Low External Component Counts
- Individual Phase Current Calibrations and Reports
- Dynamic Phase Shedding with Programmable Current Threshold for Optimizing Efficiency at Light and Heavy Loads
- Fast Phase-Adding for Undershoot Reduction (USR)
- Backward VR12.0 and VR12.5 Compatible
- 8-Bit DAC with Selectable 5 mV or 10 mV Resolution and Output Ranges from 0.25 V to 1.52 V or 0.5 V to 2.8125 V for Dual Channels
- Driverless Configuration for Efficient High-Frequency Switching
- Fully Compatible with TI NextFET™ Power Stage for High-Density Solutions
- Accurate, Adjustable Voltage Positioning
- Frequency Selections with Closed-loop Frequency Control: 300 kHz to 1 MHz
- Patented AutoBalance™ Phase Balancing
- Selectable, 16-level Per-Phase Current Limit
- PMBus™ System Interface for Telemetry of Voltage, Current, Power, Temperature, and Fault Conditions
- Dynamic Output Voltage Transitions with Programmable Slew Rates via SVID or PMBus Interface
- Conversion Voltage Range: 4.5 V to 17 V
- Low Quiescent Current
- 5 mm × 5 mm, 40-Pin, WQFN PowerPad™ Package

1.2 Applications

- VR13 Memory Power of Server and Telecom Applications
- ASIC Needs Dual Power Rails
- High-Performance Processor Power

1.3 Description

The TPS53659 is a fully VR13 SVID compliant step-down controller with dual channels, built-in non-volatile memory (NVM), and PMBus™ interface, and is fully compatible with TI NexFET™ power stage. Advanced control features such as D-CAP+™ architecture with undershoot reduction (USR) provide fast transient response, low output capacitance, and good current sharing. The device also provides novel phase interleaving strategy and dynamic phase shedding for efficiency improvement at different loads. Adjustable control of V_{CORE} slew rate and voltage positioning round out the Intel® features. In addition, the device supports the PMBus communication interface for reporting the telemetry of voltage, current, power, temperature, and fault conditions to the systems. All programmable parameters can be configured by the PMBus interface and can be stored in NVM as the new default values to minimize the external component count.

The TPS53659 device if offered in a thermally enhanced 40-pin WQFN packaged and is rated to operate from –40°C to 125°C.

Table 1-1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TPS53659	WQFN (40)	5 mm × 5 mm

(1) For more information, see, *Mechanical, Packaging, and Orderable Information*.

Table of Contents

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2016	*	Initial release.

3 Device and Documentation Support

3.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

3.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

3.3 Trademarks

NextFET, AutoBalance, PowerPad, PMBus, NexFET, D-CAP+, E2E are trademarks of Texas Instruments.
Intel is a registered trademark of Intel.
PMBus is a trademark of SMIF, Inc..

3.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

3.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

4 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53659RSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS 53659	Samples
TPS53659RSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS 53659	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

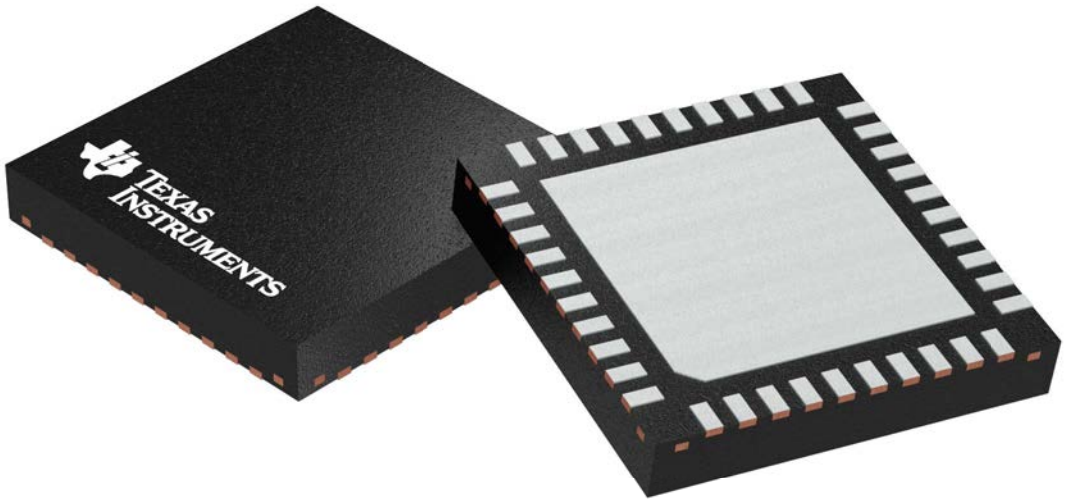
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



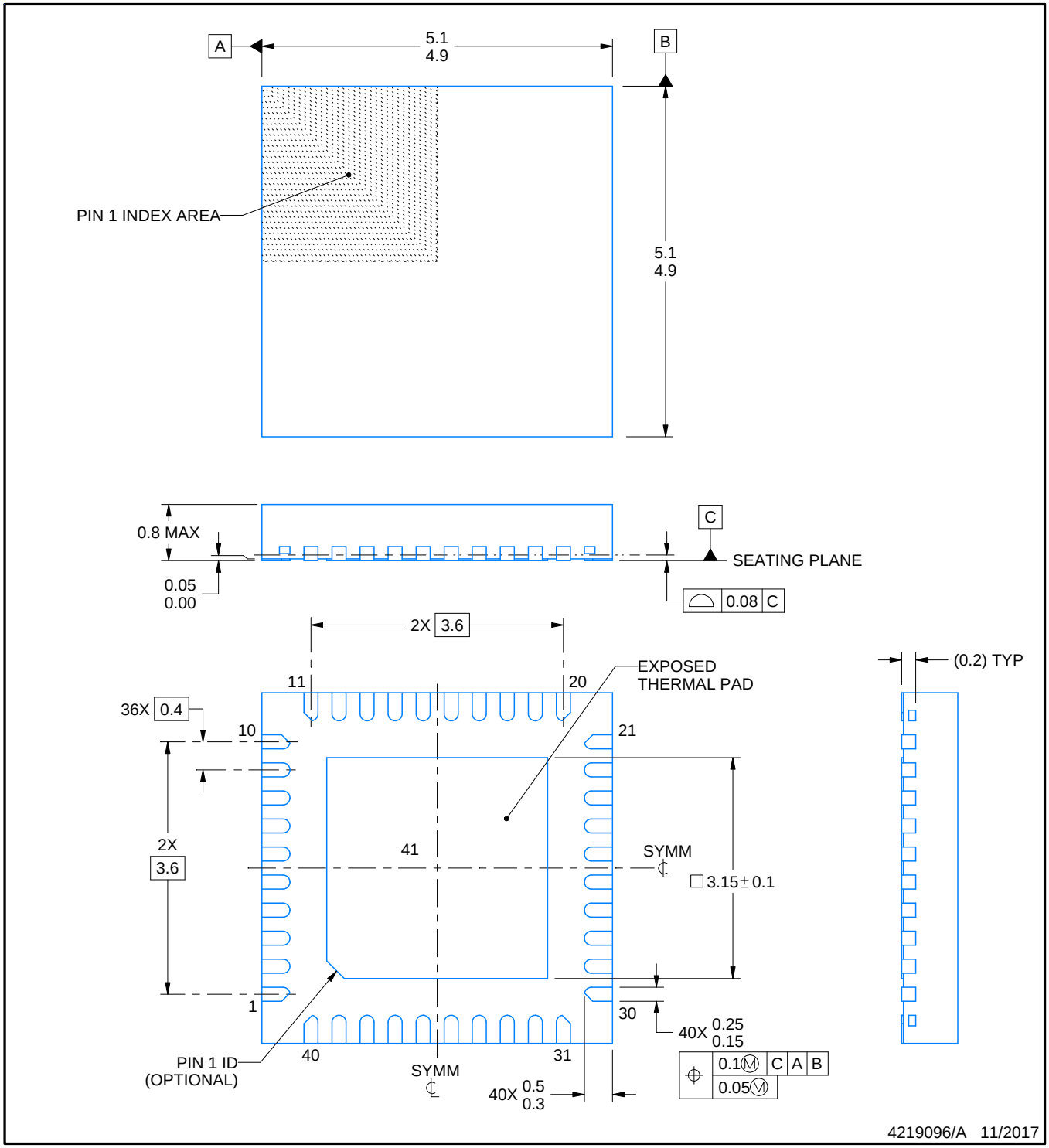
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RSB0040E

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

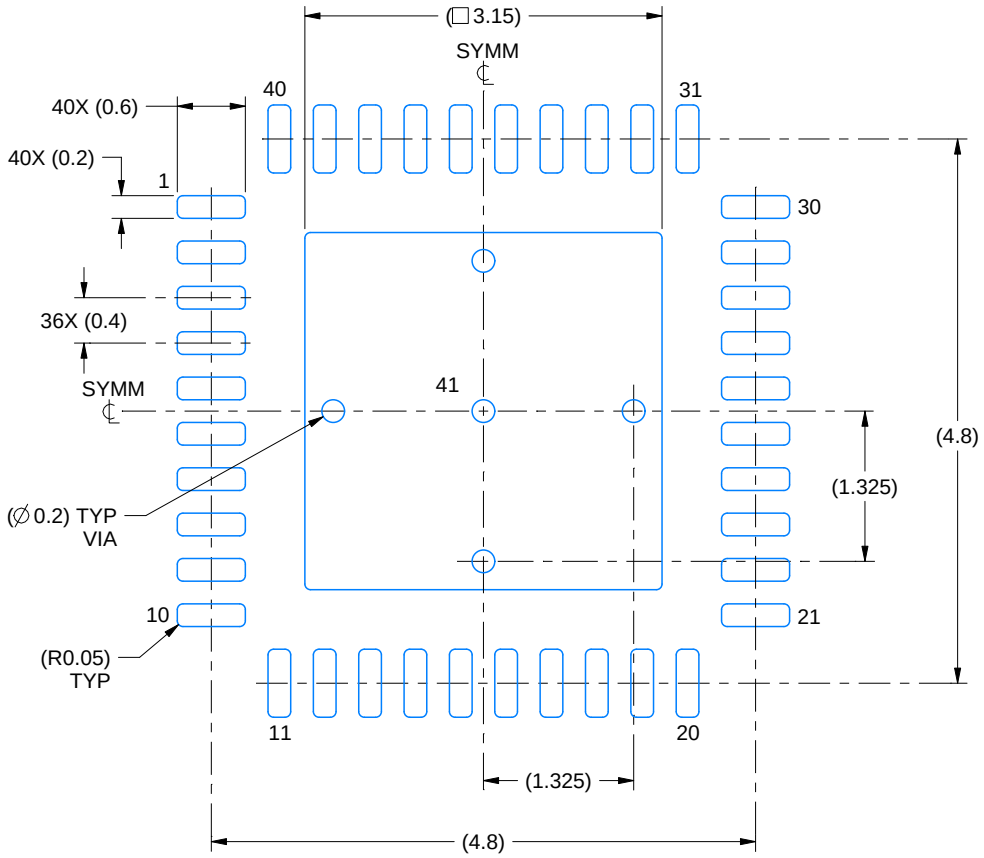
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

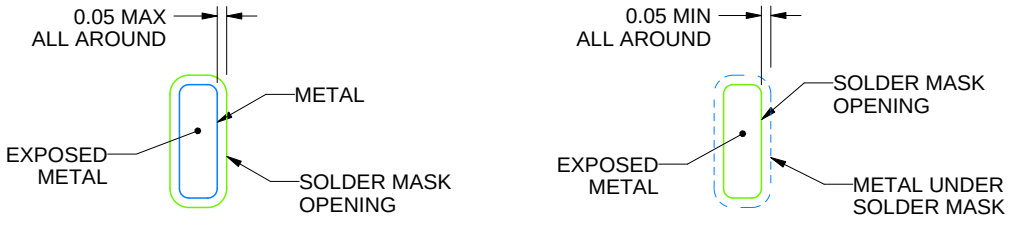
RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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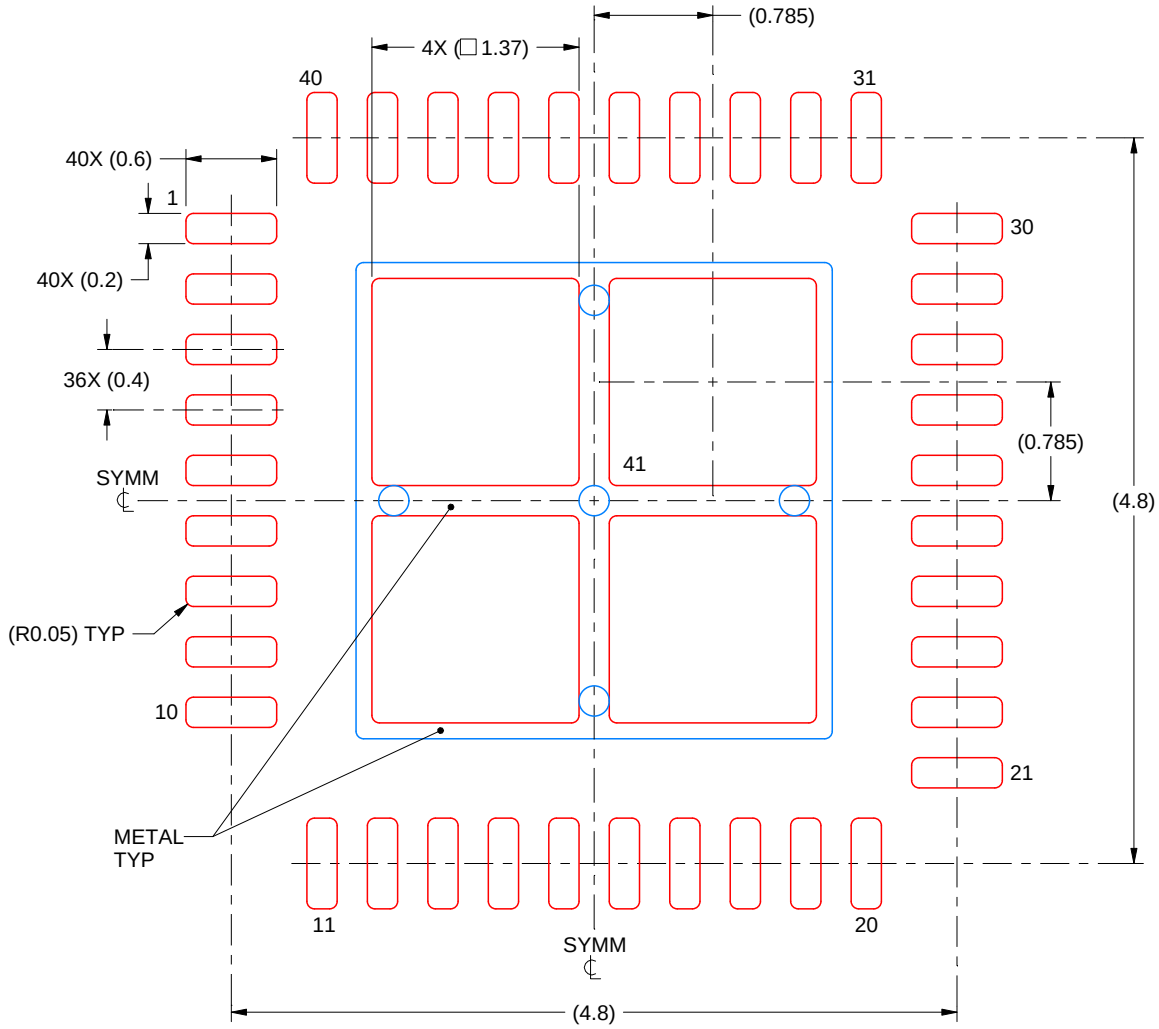
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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