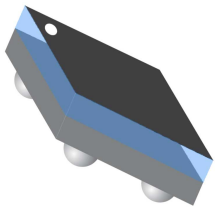
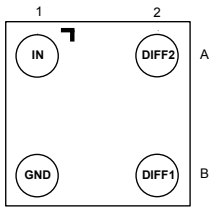
BAL-WILC10-01D3

Datasheet

50 Ω / conjugate match to WILC1000 transformer balun



Chip scale package on glass
4 bumps - 0.95 x 0.95 mm



Product status link
BAL-WILC10-01D3

Features

- 2.45 GHz Balun with integrated matching network
- Matching optimized for ATMEL WILC1000
- Low insertion loss
- Low amplitude imbalance
- Coated Flip-Chip on glass
- Small footprint < 0.90 mm²
- Benefits
  - Very low profile
  - High RF performance
  - PCB space saving versus discrete solution
  - BOM count reduction
  - Efficient manufacturability

Applications

- 2.45 GHz impedance matched balun
- Optimized for the ATMEL SmartConnect WILC1000 Wireless Link Controller
- Connectivity

Description

This device is an ultra-miniature matched balun.

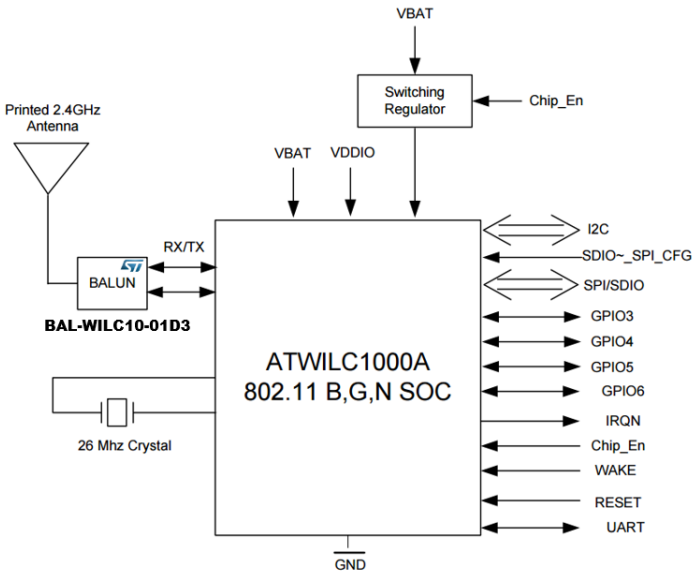
Matching impedance has been optimized for the ATMEL SmartConnect WILC1000 Wireless Link Controller.

It is using STMicroelectronics IPD technology on non-conductive glass substrate which optimizes RF performance.

1 Characteristics

1.1 Circuit block diagram

Figure 1. Block diagram



1.2 Absolute ratings

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter	Value	Unit
P_{IN}	Input power RF_{IN}	20	dBm
V_{ESD}	ESD ratings MIL STD 883C (HBM: C = 100pF, R = 1.5kΩ, air discharge)	2000	V
	ESD ratings machine model (MM: C = 200pF, R = 25 Ω, L = 500 nH)	500	
	ESD ratings charged device model (CDM, JESD22-C101D)	500	
T_{OP}	Operating temperature	-40 to +105	°C

1.3 Electrical characteristics

Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z_{OUT}	Nominal differential output impedance	Conjugate match to WILC1000			Ω
Z_{IN}	Nominal input impedance		50		Ω
f	Frequency range (bandwidth)	2400		2500	MHz
I_L	Insertion loss in bandwidth		0.65	0.8	dB
R_{L_SE}	Single ended return loss in bandwidth		-16	-15	
R_{L_DIFF}	Differential return loss in bandwidth		-17	-15	
H_2	Second harmonic rejection (differential mode)			-3.8	
H_3	Third harmonic rejection (differential mode)			-23	
Φ_{imb}	Phase imbalance	-2	1.3	2	°
A_{imb}	Amplitude imbalance	-0.9	0.8	0.9	dB

1.4 Characteristics curves

Figure 2. Transmission (dB)

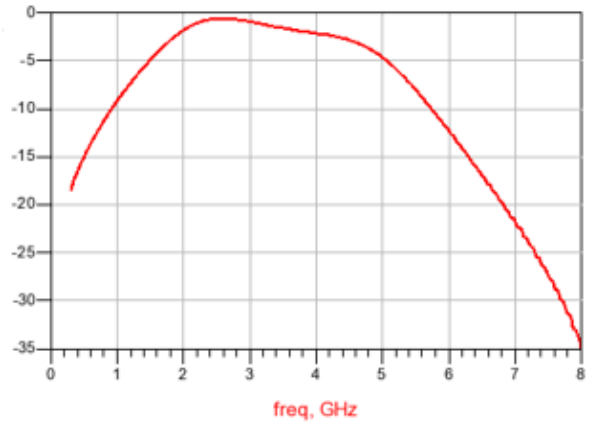


Figure 3. Insertion loss (dB)

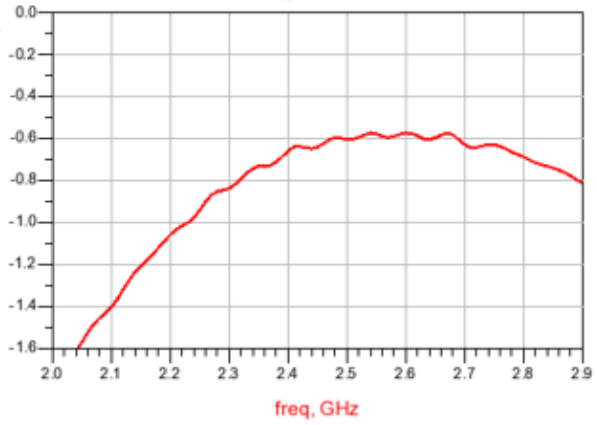


Figure 4. Amplitude imbalance (dB)

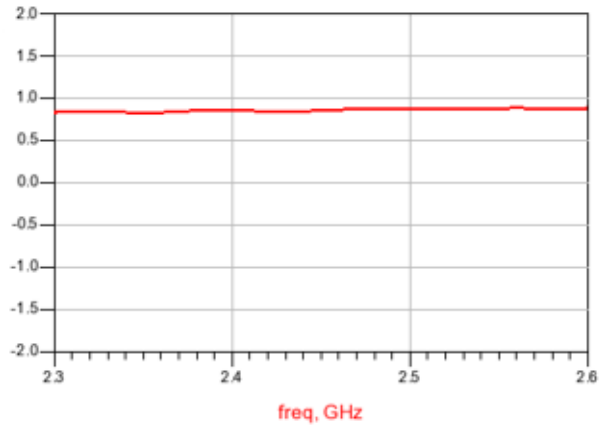


Figure 5. Return loss single ended (dB)

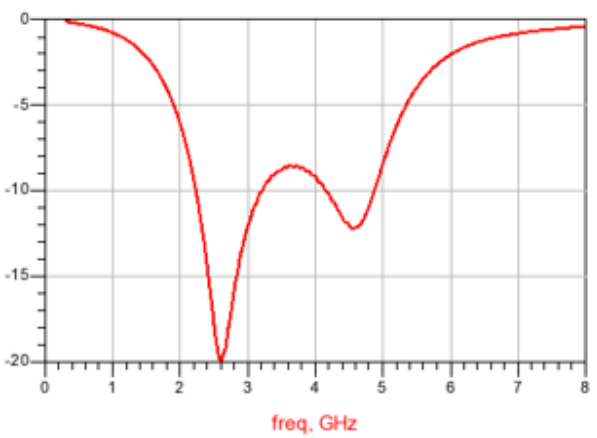


Figure 6. Return loss differential (dB)

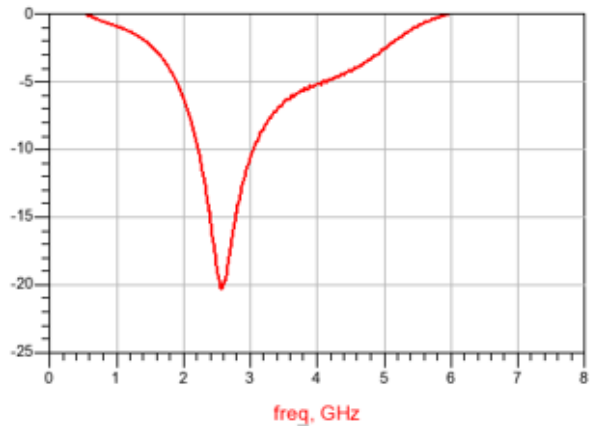
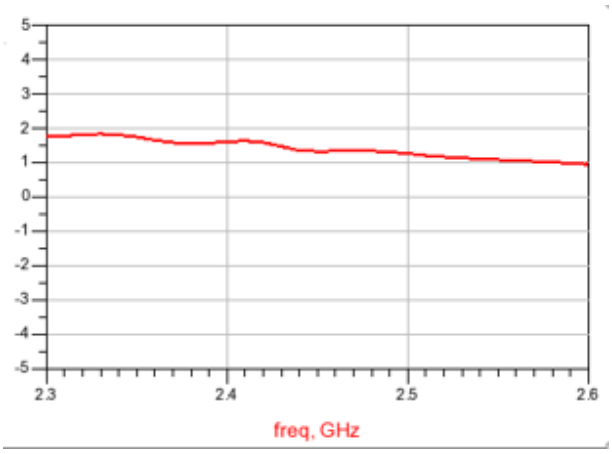


Figure 7. Phase imbalance (°)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 WLCSP 8 bumps package information

Figure 8. Flip-Chip 4 bumps CSPG 0.4 package outline

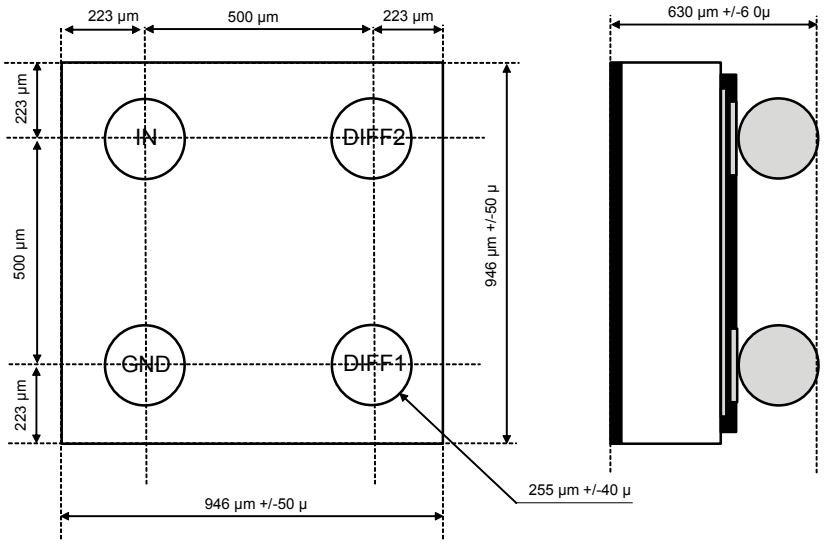
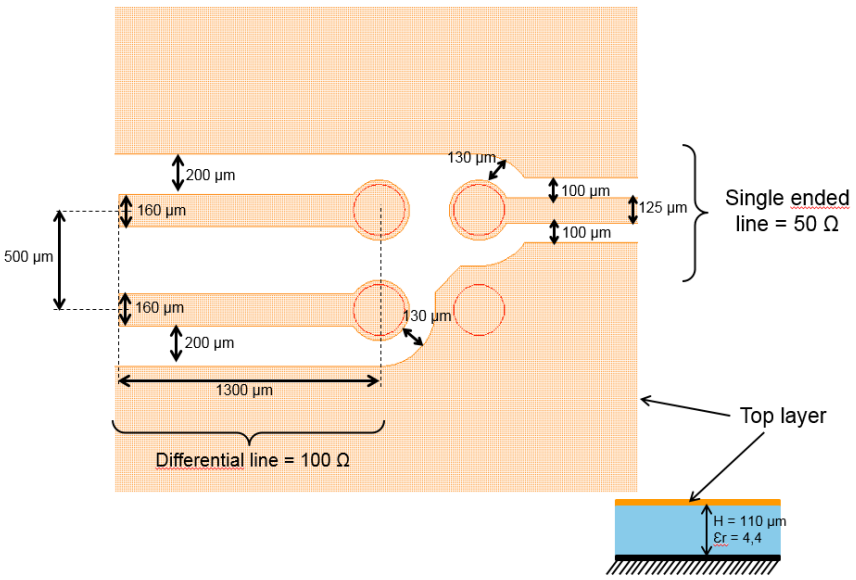
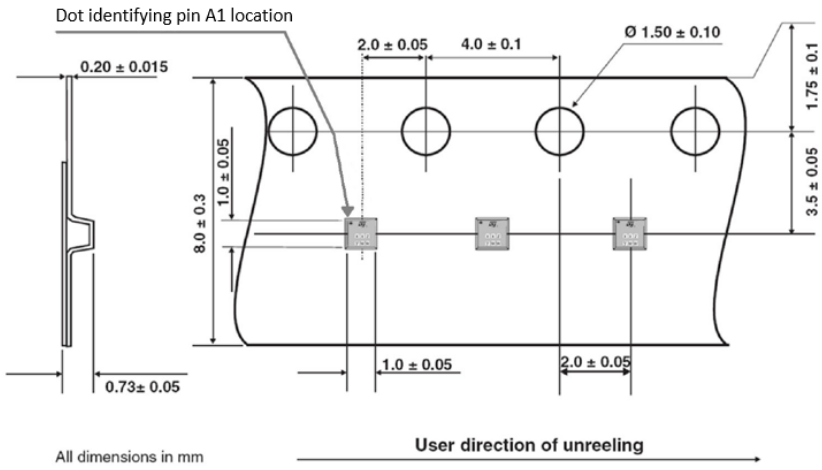


Figure 9. PCB layout recommendation



2.2 Flip-chip 4 bumps CSPG packing information

Figure 10. Flip-chip tape and reel outline



Note: More information is available in the application note AN2348: "Flip Chip: Package description and recommendations for use"

Figure 11. Marking

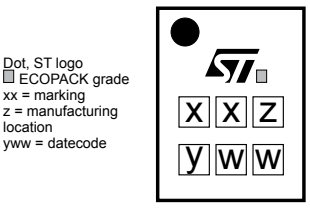


Figure 12. Footprint - non solder mask defined

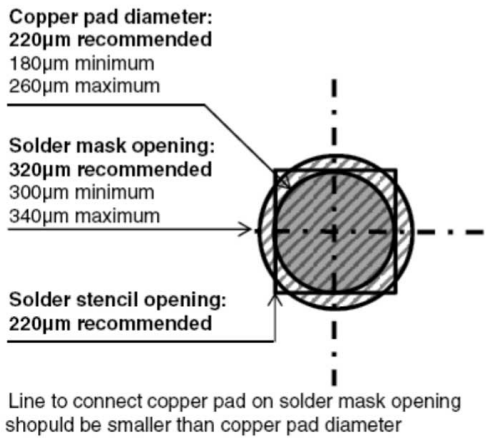
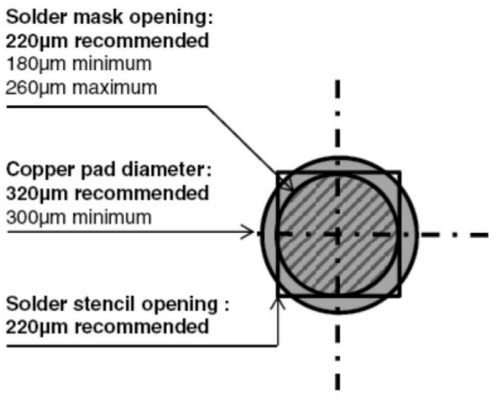


Figure 13. Footprint - solder mask defined



3 Ordering information

Table 3. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
BAL-WILC10-01D3	TI	WLCSP	1.084 mg	5000	Tape and reel (7”)

Revision history

Table 4. **Document revision history**

Date	Revision	Changes
10-Mar-2017	1	Initial release.
03-Dec-2020	2	Updated Table 3. Added Applications section.