

具有 2 位灵活电压识别 (VID) 控制的单相位、D-CAP™ 和 D-CAP2™ 控制器

查询样品: [TPS51518](#)

特性

- 差分电压反馈
- 针对精确调节的 DC 补偿
- 宽输入电压范围: 3V 至 28V
- 灵活的、2 位 VID 支持介于 0.5V 至 2V 的输出电压范围
- 具有可选控制架构的自适应接通时间调制
 - D-CAP™ 350kHz 模式, 用于快速瞬态响应
 - D-CAP2™ 350kHz 模式, 用于超低/低等效串联电阻 (ESR) 输出电容器
- 4700ppm/°C, 低侧 R_{DS} (接通) 电流感应
- 可编程软启动时间和输出电压转换时间
- 内置输出放电
- 电源良好输出
- 集成升压开关
- 内置 过压保护/欠压保护/过流保护
- 热关断 (非锁存)
- 3mm x 3mm、20 引脚、方形扁平无引脚 (QFN) (RUK) 封装

应用范围

- 笔记本电脑
- GFX 电源
- 用于英特尔 (Intel) Chief River 平台的系统代理

说明

TPS51518 是一款单一相位、D-CAP™/D-CAP2™ 同步降压控制器, 此控制器具有 2 位 VID 输入从而能够选择多达 4 个独立的外部可编程输出电压电平, 在这些电压电平上需要实现对电压电平、步长设置和电压转换率上的完全外部可编程性。它被用于需要多重电压水平的 GFX 应用。

TPS51518 支持对遥感有要求的应用中的所有固态电解电容器 (POS) / 专用聚合物铝电解电容器 (SPCAP) 和/或者所有陶瓷多层电容 (MLCC) 输出电容器选项。借助外部可编程积分电容器可实现紧密 DC 负载调节。

TPS51518 提供完全保护套件, 其中包括 OVP、过流限制 (OCL)、5V 电压闭锁 (UVLO) 和 热关断。它支持高达 28 V 的转换电压, 并且输出电压可在 0.5 V 至 2 V 的范围内进行调节。

TPS51518 采用 3mm x 3mm, QFN、0.4mm 引脚中心距封装且额定温度范围为 -10°C 至 105°C。



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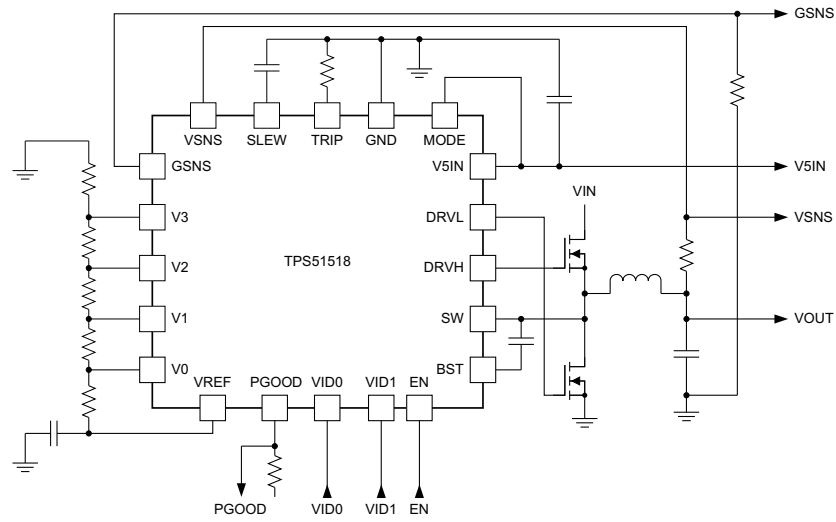
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UDG-11217



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾⁽²⁾

T _A	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY
–10°C to 105°C	PLASTIC QUAD FLAT PACK (QFN)	TPS51518RUKR	20	Tape and reel	3000
		TPS51518RUKT	20	Mini reel	250

- (1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

			MIN	MAX	UNIT
Input voltage range ⁽²⁾	BST		−0.3	36.0	V
	BST ⁽³⁾		−0.3	6.0	
	SW		−5	30	
	EN, TRIP, MODE, VID1, VID0		−0.3	5.5	
	5VIN		−0.3	5.3	
	SLEW, VSNS		−0.3	3.6	
	GSNS		−0.35	0.35	
	GND		−0.3	0.3	
Output voltage range ⁽²⁾	DRVH		−5	36	V
	DRVH ⁽³⁾		−0.3	6.0	
	DRVL		−0.3	6.0	
		transient < 20 ns	−2.0	6.0	
	PGOOD		−0.3	6.0	
	VREF, V0, V1, V2, V3		−0.3	3.6	
Junction temperature, T _J			−40	125	°C
Storage temperature, T _{STG}			−55	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.
- (3) Voltage values are with respect to the SW terminal.

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RECOMMENDED OPERATING CONDITIONS⁽¹⁾⁽²⁾

		VALUE		
		MIN	MAX	UNIT
Supply voltage	V5IN	4.50	5.25	V
Input voltage range	BST	−0.1	33.5	V
	BST ⁽¹⁾	−0.1	5.5	
	SW	−3	28	
	SW ⁽²⁾	−4.5	28.0	
	EN, TRIP, MODE, VID1, VID0	−0.1	5.5	
	SLEW, VSNS	−0.1	3.5	
	GSNS	−0.3	0.3	
	GND	−0.1	0.1	
Output voltage range	DRVH	−3.0	33.5	V
	DRVH ⁽²⁾	−4.5	33.5	
	DRVH ⁽¹⁾	−0.1	5.5	
	DRVL	−0.1	5.5	
	transient < 20 ns	−1.5	5.5	
	PGOOD	−0.1	5.5	
	VREF, V0, V1, V2, V3	−0.1	3.5	
Operating free-air temperature, T _A		−10	105	°C

(1) Voltage values are with respect to the SW terminal.

(2) This voltage should be applied for less than 30% of the repetitive period.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS51518	UNITS
		RUK (20) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	94.1	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	58.1	
θ_{JB}	Junction-to-board thermal resistance	64.3	
Ψ_{JT}	Junction-to-top characterization parameter	31.8	
Ψ_{JB}	Junction-to-board characterization parameter	58.0	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	5.9	

(1) 有关传统和新的热度的更多信息，请参阅 IC 封装热量量 应用报告 [SPRA953](#)。

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{VIN} = 5\text{ V}$, $V_{MODE} = 5\text{ V}$, $V_{EN} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{V5IN}	V5IN supply current	T _A = 25°C, No load, V _{EN} = 5 V, V _{MODE} = 5 V	560			μA
I _{V5SDN}	V5IN shutdown current	T _A = 25°C, No load, V _{EN} = 0 V	1			μA
VREF OUTPUT						
V _{VREF}	Output voltage	I _{VREF} = 30 μA, w/r/t GSNS	2.000			V
V _{VREFTOL}	Output voltage tolerance	0 μA ≤ I _{VREF} < 30 μA, 0°C ≤ T _A < 85°C	-0.8%		0.8%	
		0 μA ≤ I _{VREF} < 300 μA, -10°C ≤ T _A < 105°C	-1%		1%	
I _{VREFOCL}	Current limit	V _{VREF} -GSNS = 1.7 V	0.4	1.0		mA
OUTPUT VOLTAGE						
V _{SLEWCLP}	SLEW clamp voltage	V _{REFIN} = 1 V	0.92		1.08	V
g _M	Error amplifier transconductance	V _{REFIN} = 1 V	60			μS
I _{VSNS}	VSNS input current	V _{VSNS} = 1.0 V	-1		1	μA
I _{VSNSDIS}	VSNS discharge current	V _{EN} = 0 V, V _{VSNS} = 0.5 V, V _{MODE} = 0 V	12			mA
SMPS FREQUENCY						
f _{SW}	Switching frequency	V _{IN} = 12 V, V _{VSNS} = 1.0 V, V _{MODE} = 0 V	350			kHz
t _{ON(min)}	Minimum on-time	DRVH rising to falling	40			ns
t _{OFF(min)}	Minimum off-time	DRVH falling to rising	320			
DRIVERS						
R _{DH}	High-side driver resistance	Source, I _{DRVH} = 50 mA	1.7			Ω
		Sink, I _{DRVH} = 50 mA	0.8			
R _{DL}	Low-side driver resistance	Source, I _{DRVL} = 50 mA	1.1			Ω
		Sink, I _{DRVL} = 50 mA	0.6			
INTERNAL BOOT STRAP SW						
V _{FBST}	Forward voltage	V _{V5IN-BST} , T _A = 25°C, I _F = 10 mA	0.1		0.2	V
I _{BST}	BST leakage current	T _A = 25°C, V _{BST} = 33 V, V _{SW} = 28 V	0.01		1.50	μA
LOGIC THRESHOLD AND TIMING						
V _{VIDx(LL)}	VID1/VID0 low-level voltage				0.3	V
V _{VIDx(LH)}	VID1/VID0 high-level voltage		0.9			V
V _{VIDx(HYST)}	VID1/VID0 hysteresis voltage		0.4			V
I _{VIDx(LLK)}	VID1/VID0 input leakage current		-1	0	1	μA
V _{EN(LL)}	EN low-level voltage				0.5	V
V _{EN(LH)}	EN high-level voltage		1.5			V
V _{EN(HYST)}	EN hysteresis voltage		0.25			V
I _{EN(LLK)}	EN input leakage current		-1		1	nA
SOFT START/SLEW RATE						
I _{SS}	Soft-start current	Soft-start current source	10			μA
I _{SLEW}	Slew control current		50			μA

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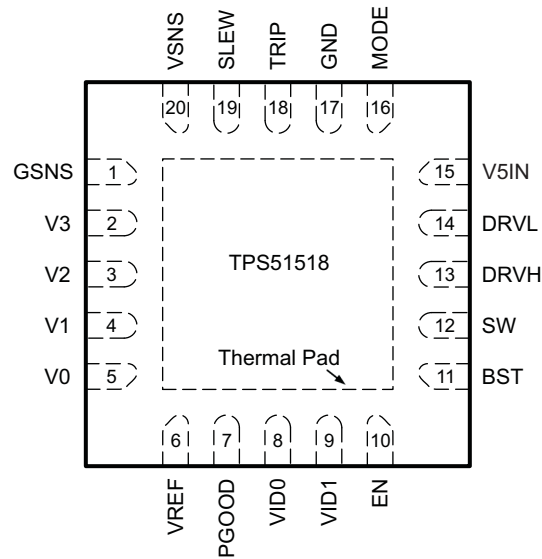
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_{VIN} = 5\text{ V}$, $V_{MODE} = 5\text{ V}$, $V_{EN} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PGOOD COMPARATOR						
V_{PGTH}	PGOOD threshold	PGOOD in from higher		108%		
		PGOOD in from lower		92%		
		PGOOD out to higher		116%		
		PGOOD out to lower		84%		
I_{PG}	PGOOD sink current	$V_{PGOOD} = 0.5\text{ V}$		6.0		mA
t_{PGDLY}	PGOOD delay time	Delay for PGOOD in		1		ms
		Delay for PGOOD out		0.2		μs
$t_{PGCMPSS}$	PGOOD start-up delay time	PGOOD comparator wake up delay		1.5		ms
I_{PGLK}	PGOOD leakage current		−1	0	1	μA
CURRENT DETECTION						
I_{TRIP}	TRIP source current	$T_A = 25^\circ\text{C}$, $V_{TRIP} = 0.4\text{ V}$	9	10	11	μA
TC_{ITRIP}	TRIP source current temperature coefficient ⁽¹⁾			4700		ppm/°C
V_{TRIP}	VTRIP voltage range		0.2		3	V
V_{OCL}	Current limit threshold	$V_{TRIP} = 3.0\text{ V}$	360	375	390	mV
		$V_{TRIP} = 1.6\text{ V}$	190	200	210	
		$V_{TRIP} = 0.2\text{ V}$	20	25	30	
V_{OCLN}	Negative current limit threshold	$V_{TRIP} = 3.0\text{ V}$	−390	−375	−360	mV
		$V_{TRIP} = 1.6\text{ V}$	−212	−200	−188	
		$V_{TRIP} = 0.2\text{ V}$	−30	−25	−20	
V_{ZC}	Zero cross detection offset			0		mV
PROTECTIONS						
V_{UVLO}	V5IN UVLO threshold voltage	Wake-up	4.3	4.4	4.6	V
		Shutdown	3.8	4.0	4.2	
V_{OVP}	OVP threshold voltage	OVP detect voltage	118%	120%	122%	
t_{OVPDLY}	OVP propagation delay	With 100-mV overdrive		300		ns
V_{UVP}	UVP threshold voltage	UVP detect voltage	66%	68%	70%	
t_{UVPDLY}	UVP delay			1		ms
$t_{UVPENDLY}$	UVP enable delay			1.4		ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold ⁽¹⁾	Shutdown temperature		140		°C
		Hysteresis		10		

(1) Ensured by design. Not production tested.

DEVICE INFORMATION



PIN DESCRIPTIONS

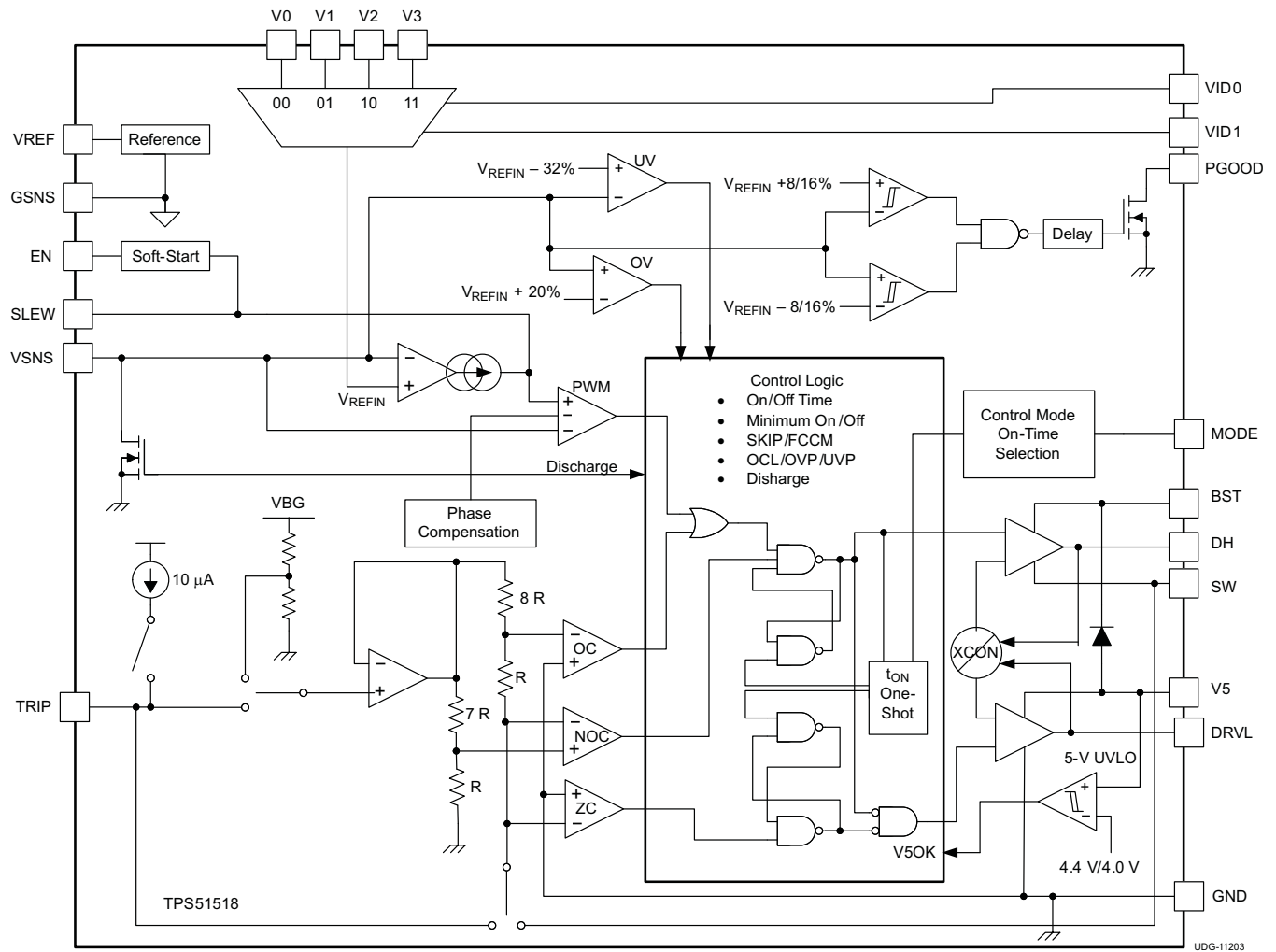
PIN		I/O	DESCRIPTION
No.	NAME		
11	BST	I	Supply input for high-side MOSFET driver (bootstrap terminal). Connect a capacitor from this pin to the SW pin. Internally connected to V5IN via the bootstrap MOSFET switch.
13	DRVH	O	High-side MOSFET gate driver output.
14	DRVL	O	Synchronous low-side MOSFET gate driver output.
10	EN	I	Enable input for the device. Support 3.3-V logic
17	GND	I	Combined AGND and PGND point. The positive on-resistance current sensing input.
1	GSNS	I	Voltage sense return tied directly to GND sense point of the load. Tie to GND with a 10-Ω resistor to close feedback if die sensing is used. Short to GND if remote sense is not used.
16	MODE	I	See Table 2 .
7	PGOOD	O	PGOOD output. Connect pull-up resistor.
19	SLEW	I	Program the startup using 10 μA and voltage transition time using 50 μA from an external capacitor via current source.
12	SW	I/O	High-side MOSFET gate driver return. The $R_{DS(on)}$ current sensing input (–).
18	TRIP	I	Connect resistor to GND to set OCL at $V_{TRIP}/8$. Output 10 μA current at room temperature, $T_C = 4700\text{ppm}/^\circ\text{C}$.
5	V0	I	Voltage set-point programming resistor input, corresponding to 00
4	V1	I	Voltage set-point programming resistor input, corresponding to 01
3	V2	I	Voltage set-point programming resistor input, corresponding to 10
2	V3	I	Voltage set-point programming resistor input, corresponding to 11
15	V5IN	I	5-V power supply input for internal circuits and MOSFET gate drivers
8	VID0	I	Logic input for set-point voltage selector. Use in conjunction with VID1 pin to select among four set-point reference voltages. Support 1-V and 3.3-V logic.
9	VID1	I	Logic input for set-point voltage selector. Use in conjunction with VID0 pin to select among four set-point reference voltages. Support 1-V and 3.3-V logic.
6	VREF	O	2 V, 300-μA voltage reference. Bypass to GND with a 1-μF ceramic capacitor.
20	VSNS	I	Voltage sense return tied directly to the load voltage sense point. Tie to V_{OUT} with a 10-Ω resistor to close feedback if die sensing is used.
Thermal Pad			Connect directly to system GND plane with multiple vias.

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FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

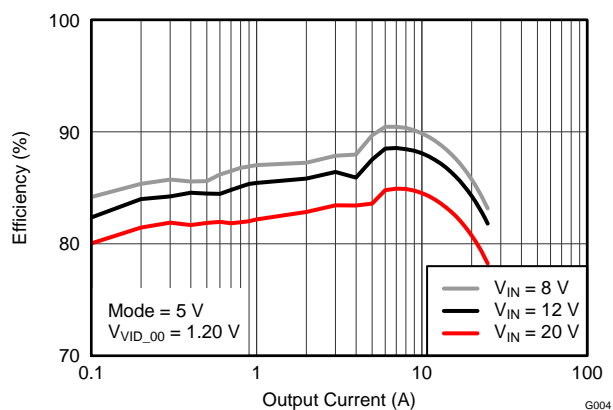


Figure 1. GFX Efficiency

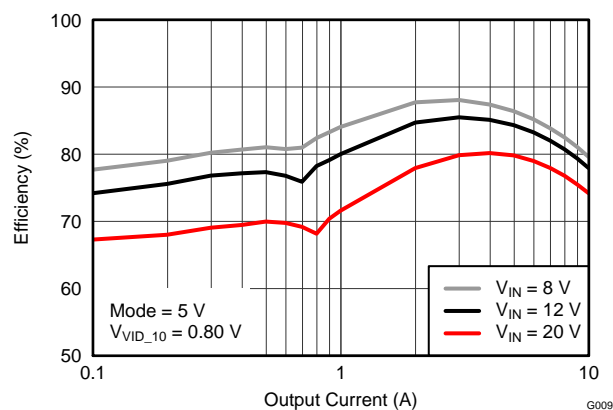


Figure 2. SA Efficiency

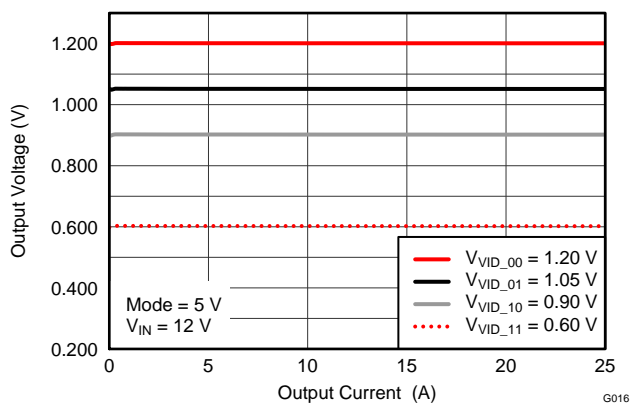


Figure 3. GFX Load Regulation

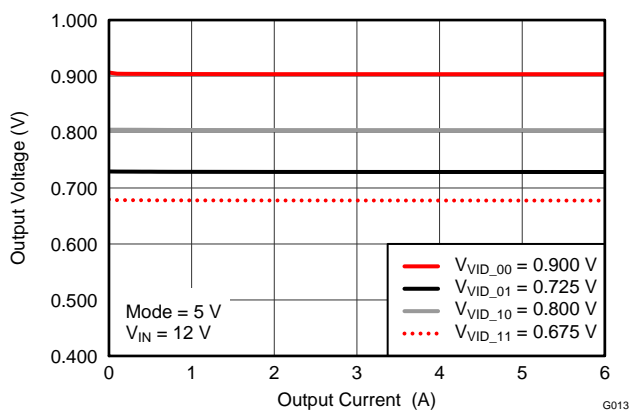


Figure 4. SA Load Regulation

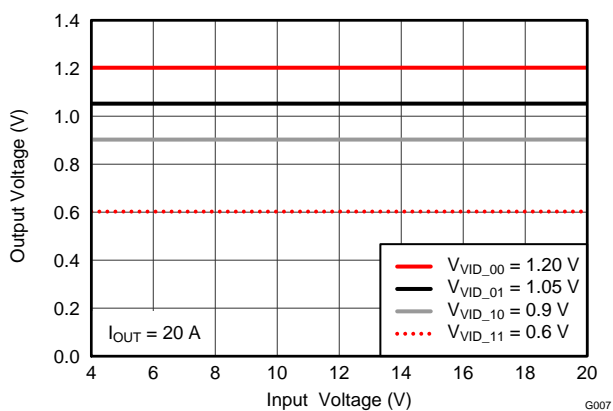


Figure 5. GFX Line Regulation

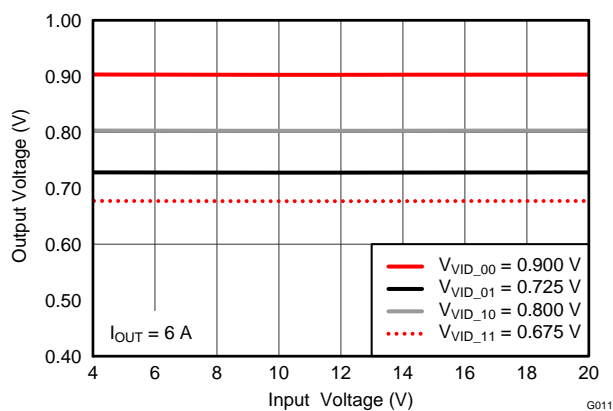


Figure 6. SA Line Regulation

TYPICAL CHARACTERISTICS (continued)

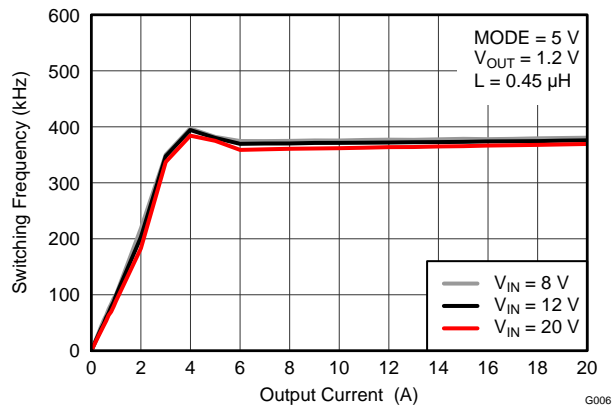


Figure 7. GFX Frequency vs. Load Current

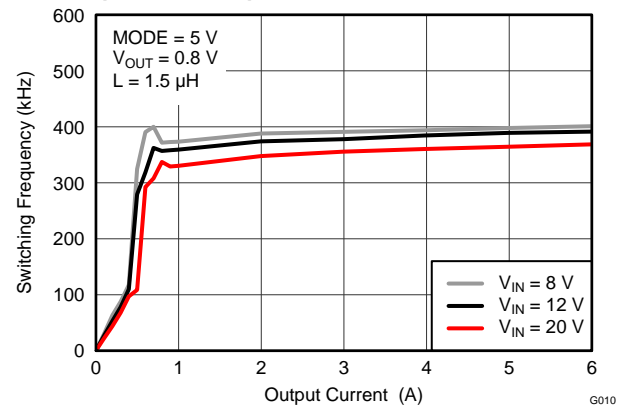


Figure 8. SA Frequency vs. Load Current

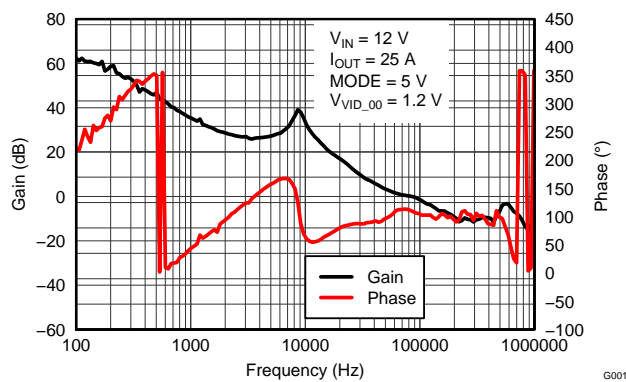


Figure 9. GFX Bode Plot

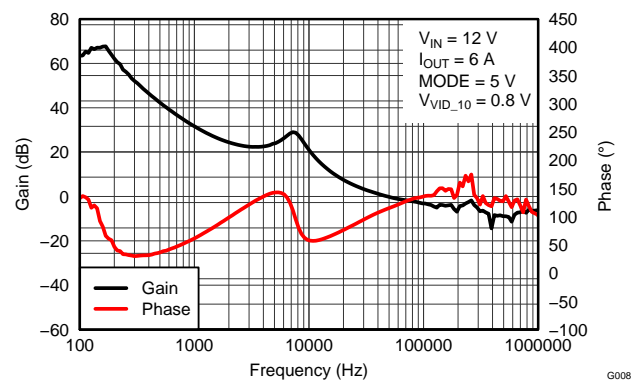


Figure 10. SA Bode Plot

TYPICAL CHARACTERISTICS

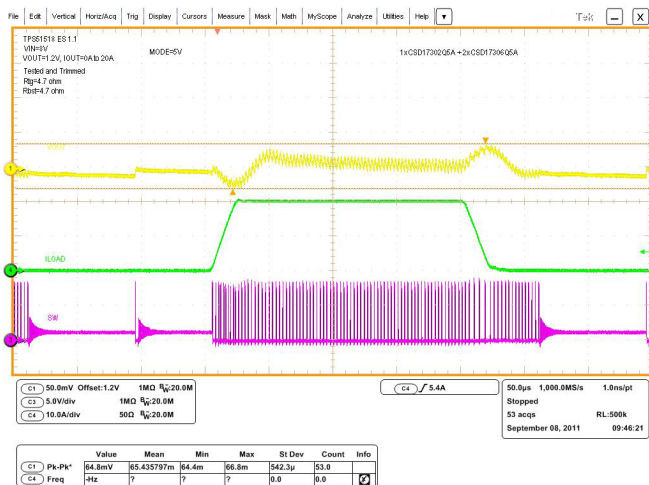


Figure 11. Load Transient

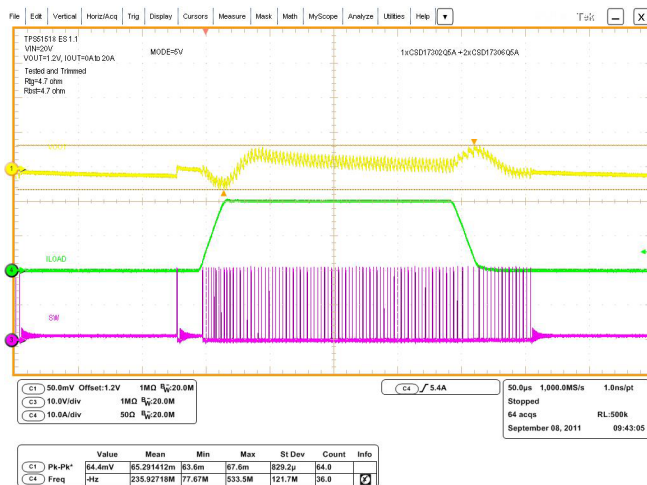


Figure 12. Load Transient



Figure 13. Startup

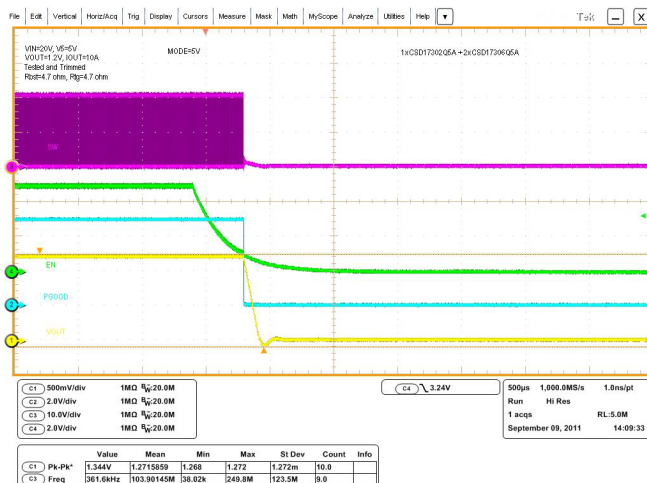


Figure 14. Shutdown

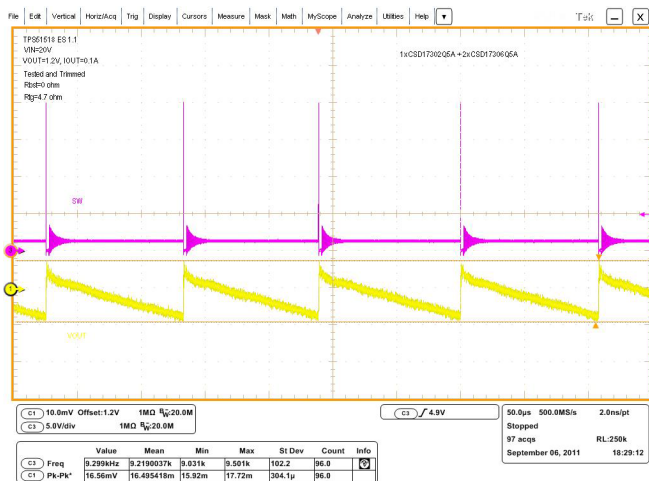


Figure 15. Steady-State Ripple, I_{LOAD} = 0.1 A

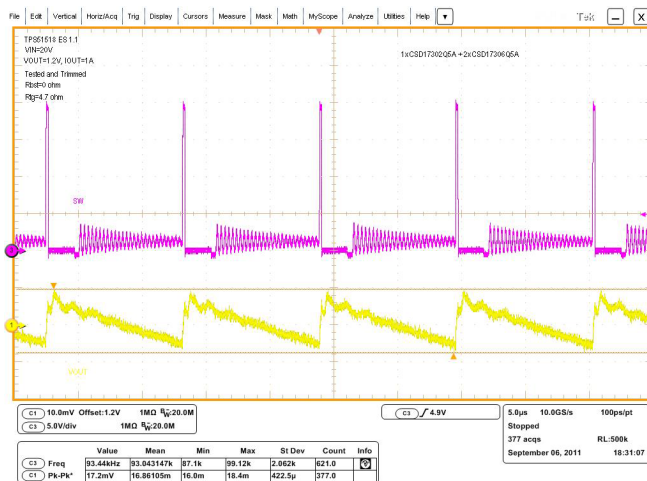


Figure 16. Steady-State Ripple, I_{LOAD} = 1 A

TYPICAL CHARACTERISTICS (continued)

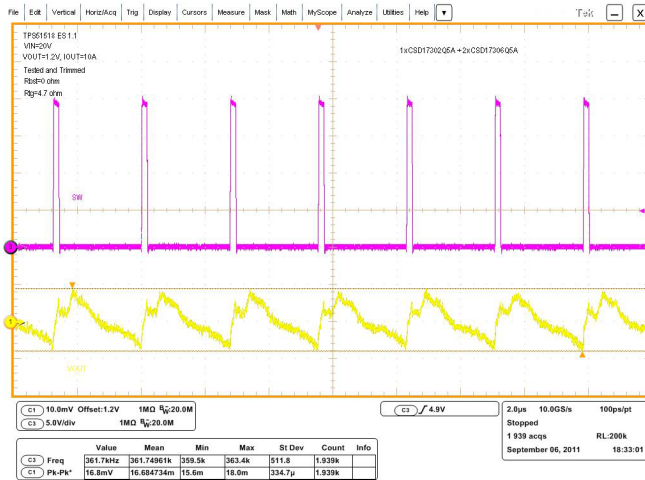


Figure 17. Steady-State Ripple, $I_{LOAD} = 10\text{ A}$

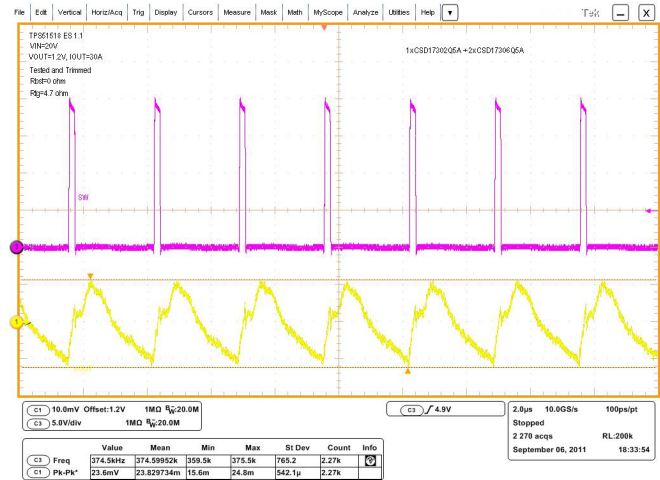


Figure 18. Steady-State Ripple, $I_{LOAD} = 30\text{ A}$

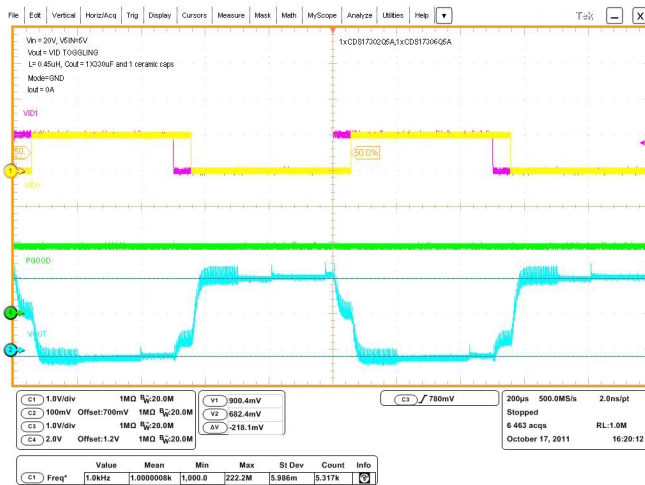


Figure 19. VID transition, $I_{LOAD} = 0\text{ A}$

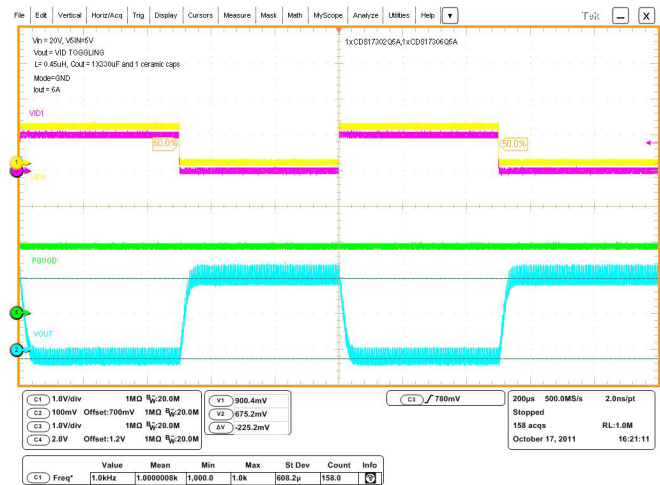


Figure 20. VID transition, $I_{LOAD} = 6\text{ A}$

Switch Mode Power Supply Control

The TPS51518 is a high performance, single-synchronous step-down controller with differential voltage feedback. It realizes accurate regulation at the specific load point over wide load range.

The TPS51518 supports two control architectures, D-CAP™ mode and D-CAP2™ mode. Both control modes do not require complex external compensation networks and are suitable for designs with small external components counts. The D-CAP™ mode provides fast transient response with appropriate amount of equivalent series resistance (ESR) on the output capacitors. The D-CAP2™ mode is dedicated for a configuration with very low ESR output capacitors such as multi-layer ceramic capacitors (MLCC). For the both modes, an adaptive on-time control scheme is used to achieve pseudo-constant frequency. The TPS51518 adjusts the on-time (t_{ON}) to be inversely proportional to the input voltage (V_{IN}) and proportional to the SMPS output voltage (V_{OUT}). The switching frequency remains nearly constant over the variation of input voltage at the steady-state condition. Control modes are selected by the MODE pin described in [Table 2](#).

VREF, V0, V1, V2, V3 and Output Voltage

The device provides a 2.0-V, accurate voltage reference from the VREF pin. This output has a 300- μ A current sourcing capability to drive V0, V1, V2 and V3 input voltages through a voltage divider circuit as shown in [Figure 21](#). If higher overall system accuracy is required, the sum of total resistance ($R1+R2+R3+R4+R5$) from VREF to GND should be designed to be more than 67 k Ω . A MLCC capacitor with a value of 0.1- μ F or larger should be attached close to the VREF pin.

The device also provides 2-bit VID flexible output voltage control. Up to four voltage levels can be programmed externally by a voltage divider circuit. V0 corresponds to VID 00, V1 corresponds to VID 01, V2 corresponds to VID 10 and V3 corresponds to VID 11. It is not necessary to match the voltage set point (V_{SET1} , V_{SET2} , V_{SET3} or V_{SET4}) to any particular V0, V1, V2 or V3 input. Assignment of the input voltage is entirely dependent on the user requirement, which makes the device very easy and flexible to use.

The device can also be configured to provide 1-bit VID flexible output voltage operation. Up to two voltage levels can be programmed externally by a voltage divider circuit. Normally, if 1-bit VID operation is desired, the VID0 pin is generally used (the VID1 pin should be grounded if not used).

In the applications where fewer than four input voltage levels are needed, the remaining input voltage pins cannot be left floating. Connection from the unused pins to GND is required for proper operation.

Table 1. VID Settings

	VID1	VID0	
V0	0	0	V_{SET1} , V_{SET2} , V_{SET3} , V_{SET4}
V1	0	1	V_{SET1} , V_{SET2} , V_{SET3} , V_{SET4}
V2	1	0	V_{SET1} , V_{SET2} , V_{SET3} , V_{SET4}
V3	1	1	V_{SET1} , V_{SET2} , V_{SET3} , V_{SET4}

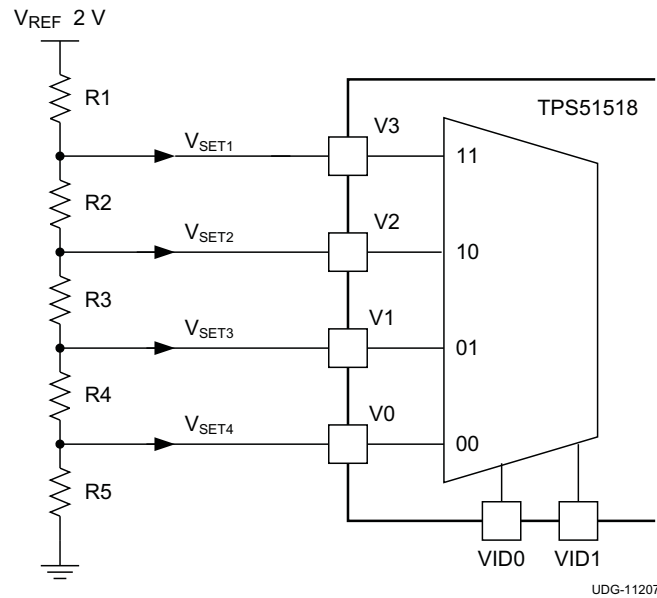


Figure 21. Setting the Output Voltage

Soft-Start and Power Good

Prior to asserting EN high, the power stage conversion voltage and V5IN voltage should be ready. When EN is asserted high, TPS51518 provides soft start to suppress in-rush current during start-up. The soft start action is achieved by an internal SLEW current of 10 μ A (typ) sourcing into a small external MLCC capacitor connected from SLEW pin to GND.

Use [Equation 1](#) to determine the soft-start timing.

$$t_{SS} = C_{SLEW} \times \frac{V_{OUT}}{I_{SLEW}}$$

where

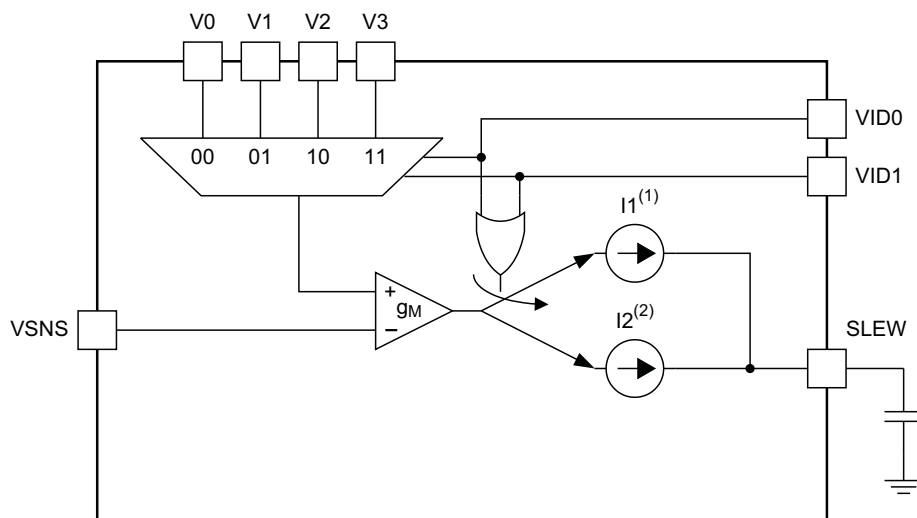
- C_{SLEW} is the soft start capacitance
- V_{OUT} is the output voltage
- I_{SLEW} is the internal 10- μ A current source

(1)

The TPS51518 has a powergood open-drain output that indicates the Vout voltage is within the target range. The target voltage window and transition delay times of the PGOOD comparator are $\pm 8\%$ (typ) and 1-ms delay for assertion from low to high, and $\pm 16\%$ (typ) and 0.2- μ s delay for de-assertion from high to low during operation.

SLEW and VID Function

In addition to providing soft start function, SLEW is also used to program the VID transition time. TPS51518 supports 2-bit VID and 1-bit VID operations. VID0 and VID1 works with 1.05-V logic level signals with capability of supporting up to 3.3-V logic high.



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(1) I1: Enable during VID transition, 50 μ A.

(2) I2: Soft start, 10 μ A.

Figure 22. VID Configuration

During VID transition:

- SLEW current is increased to 50 μ A. Based on the VID transition time of the system, the amount of the SLEW capacitance can be calculated to meet such requirement. The minimum SLEW capacitance can be supported by the device is 2.7 nF.

$$C_{\text{SLEW}} = I_{\text{SLEW_VID}} \times \frac{dt}{dV}$$

where

- I_{SLEW} is 50 μ A, dv is the voltage change during VID transition
- dt is the required transition time (2)
- FCCM (forced continuous conduction mode) operation is used regardless of the load level. In the meantime, the overcurrent level is temporally increased to 125% times the normal OCL level to prevent false OC trip during fast SLEW up transition. Power good, UVP and OVP functions are all blanked as well. All normal functions are resumed 16 internal clock cycles (64 μ s) after VID transition is completed.
- Additional SLEW CLAMP is implemented. If severe output short occurs (either to GND or to some other high voltage rails in the system), SLEW is engaged into SLEW CLAMP, approximately 50 mV above or below the output voltage reference point. After 32 internal clockcycles, the CLAMP is engaged, UVP and OVP functions are activated to disable the controller at fault.

MODE Pin Configuration

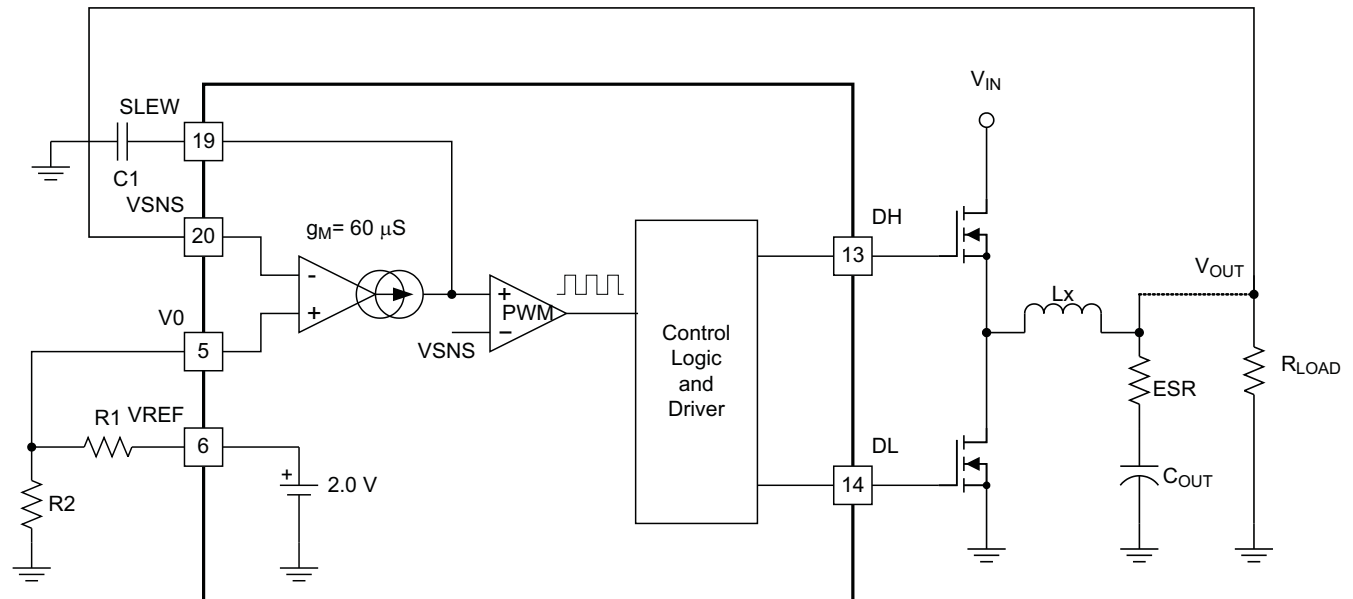
The TPS51518 reads the MODE pin voltage when the EN signal is raised high and stores the status in a register. [Table 2](#) shows the MODE connection, corresponding control topology.

Table 2. Mode States

MODE PIN CONNECTION	CONTROL TOPOLOGY	CURRENT SENSE	f _{SW} (KHz)
GND	D-CAP	R _{DS(on)}	350
5-V Supply	D-CAP2		

D-CAP™ Mode

[Figure 23](#) shows a simplified model of D-CAP™ mode architecture in the TPS51518.



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Figure 23. D-CAP™ Mode Application

The transconductance (g_M) amplifier and SLEW capacitor (C1) forms an integrator. The ripple voltage generated by ESR of the output capacitor is inverted and averaged by the integrator. The small AC component is superimposed onto otherwise DC information and forms a reference input at the PWM comparator. As long as the integrator time constant is much larger than the inverse of the loop crossover frequency, the AC component is negligible. The VSNS voltage is directly compared to the SLEW voltage at the PWM comparator. The PWM comparator creates a set signal to turn on the high side MOSFET each cycle.

The PWM comparator creates a set signal to turn on the high-side MOSFET each cycle. The D-CAP™ mode offers flexibility on output inductance and capacitance selections with ease-of-use without complex feedback loop calculation and external components. However, it does require sufficient amount of ESR that represents inductor current information for stable operation and good jitter performance. Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

The requirement for loop stability is simple and is described in [Equation 3](#). The 0-dB frequency, f₀, is recommended to be lower than 1/3 of the switching frequency to secure proper phase margin. The integrator time constant should be long enough compared to f₀, for example one decade low, as described in [Equation 4](#).

$$f_0 = \frac{1}{2\pi \times \text{ESR} \times C_{\text{OUT}}} \leq \frac{f_{\text{SW}}}{3}$$

where

- ESR is the effective series resistance of the output capacitor

- C_{OUT} is the capacitance of the output capacitor
- f_{SW} is the switching frequency

$$\frac{g_M}{2\pi \times C1} \leq \frac{f_0}{10}$$

where

- g_M is transconductance of the error amplifier (typically 60 μS)

Jitter is another attribute caused by signal-to-noise ratio of the feedback signal. One of the major factors that determine jitter performance in D-CAPTM mode is the down-slope angle of the VSNS ripple voltage. Figure 24 shows, in the same noise condition, that jitter is improved by making the slope angle larger.

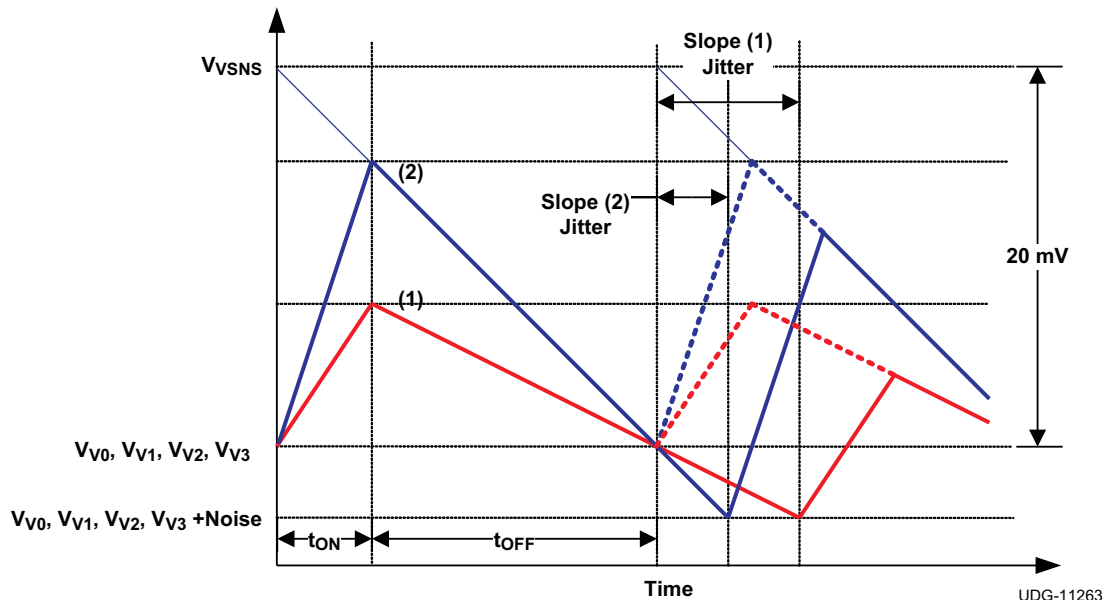


Figure 24. Ripple Voltage Slope and Jitter Performance

For a good jitter performance, use the recommended down slope of approximately 20 mV per switching period as shown in Figure 24 and Equation 5.

$$\frac{V_{OUT} \times ESR}{f_{SW} \times L_X} \geq 20mV$$

where

- V_{OUT} is the SMPS output voltage
- L_X is the inductance

D-CAP2TM Mode

Figure 25 shows a simplified model of D-CAP2TM mode architecture in the TPS51518.

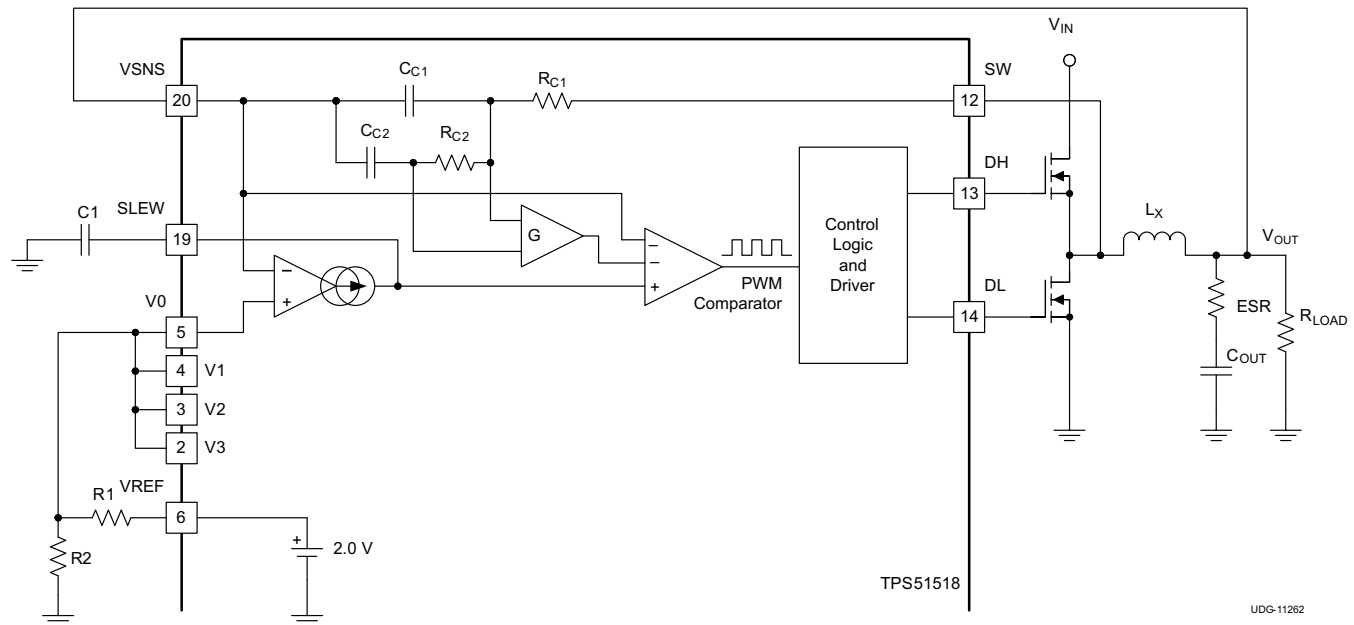


Figure 25. Simplified D-CAP2 Mode Architecture

When TPS51518 operates in D-CAP2 mode, it uses an internal phase compensation network (R_{C1} , R_{C2} , C_{C1} and C_{C2} and G) to work with very low ESR output capacitors such as multi-layer ceramic capacitors (MLCC). The role of such network is to sense and scale the ripple component of the inductor current information and then use it in conjunction with the voltage feedback to achieve loop stability of the converter.

The switching frequency used for D-CAP2 mode is 350 kHz and it is generally recommended to have a unity gain crossover (f_0) of 1/4 or 1/3 of the switching frequency, which is approximately 90 kHz to 120 kHz for the purpose of this application.

Given the range of the recommended unity gain frequency, the power stage design is flexible, as long as [Equation 6](#) is true.

$$\frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \leq \frac{1}{10} \times f_0 \quad (6)$$

When TPS51518 is configured in D-CAP2 mode, the overall loop response is dominated by the internal phase compensation network. The compensation network is designed to have two identical zeros at 5.2 kHz in the frequency domain, which serves the purpose of splitting the L-C double pole into one low frequency pole (same as the L-C double pole frequency) and one high-frequency pole (greater than the unity gain crossover frequency).

Light-Load Operation

In auto-skip mode, the TPS51518 SMPS control logic automatically reduces its switching frequency to improve light-load efficiency. To achieve this intelligence, a zero cross detection comparator is used to prevent negative inductor current by turning off the low-side MOSFET. [Equation 7](#) shows the boundary load condition of this skip mode and continuous conduction operation.

$$I_{LOAD(LL)} = \frac{(V_{IN} - V_{OUT})}{2 \times L_X} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (7)$$

Out-of-Bound Operation

When the output voltage rises to 8% above the target value, the out-of-bound operation starts. During the out-of-bound condition, the controller operates in forced PWM-only mode. Turning on the low-side MOSFET beyond the zero inductor current quickly discharges the output capacitor. During this operation, the cycle-by-cycle negative overcurrent limit is also valid. Once the output voltage returns to within regulation range, the controller resumes to auto-skip mode.

Current Sensing

In order to provide both cost effective solution and good accuracy, TPS51518 supports MOSFET $R_{DS(on)}$ sensing. For $R_{DS(on)}$ sensing scheme, TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP} . In this scheme, TRIP terminal sources $10\mu A$ of I_{TRIP} current (at $T_A = 25^\circ C$) and the trip level is set to 1/8 of the voltage across the R_{TRIP} . The inductor current is monitored by the voltage between the GND pin and the SW pin so that the SW pin is connected to the drain terminal of the low-side MOSFET. I_{TRIP} has a $4700\text{ppm}/^\circ C$ temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the sense resistor or the source terminal of the low-side MOSFET.

Overcurrent Protection

TPS51518 has cycle-by-cycle overcurrent limiting protection. The inductor current is monitored during the off-state and the controller maintains the off-state when the inductor current is larger than the overcurrent trip level. The overcurrent trip level, V_{OCTRIP} , is determined by Equation 8.

$$V_{OCTRIP} = R_{TRIP} \times \left(\frac{I_{TRIP}}{8} \right) \quad (8)$$

Because the comparison is made during the off-state, V_{OCTRIP} sets the valley level of the inductor current. The load current OCL level, I_{OCL} , can be calculated by considering the inductor ripple current.

Overcurrent limiting using $R_{DS(on)}$ sensing is shown in Equation 9.

$$I_{OCL} = \left(\frac{V_{OCTRIP}}{R_{DS(on)}} \right) + \frac{I_{IND(ripple)}}{2} = \left(\frac{V_{OCTRIP}}{R_{DS(on)}} \right) + \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L_X} \times \frac{V_{OUT}}{f_{SW} \times V_{IN}}$$

where

- $I_{IND(ripple)}$ is inductor ripple current (9)

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down.

Overvoltage and Undervoltage Protection

The TPS51518 sets the overvoltage protection (OVP) when VSNS voltage reaches a level 20% (typ) higher than the target voltage. When an OV event is detected, the controller changes the output target voltage to 0 V. This usually turns off DRVH and forces DRVL to be on. When the inductor current begins to flow through the low-side MOSFET and reaches the negative OCL, DRVL is turned off and DRVH is turned on, for a minimum on-time.

After the minimum on-time expires, DRVH is turned off and DRVL is turned on again. This action minimizes the output node undershoot due to LC resonance. When the VSNS reaches 0 V, the driver output is latched as DRVH off, DRVL on.

The undervoltage protection (UVP) latch is set when the VSNS voltage remains lower than 68% (typ) of the REFIN voltage for 1 ms or longer. In this fault condition, the controller latches DRVH low and DRVL low and discharges the V_{OUT} . UVP detection function is enabled after 1.2 ms of SMPS operation to ensure startup.

To release the OVP and UVP latches, toggle EN or adjust the V5IN voltage down and up beyond the undervoltage lockout threshold.

V5IN Undervoltage Lockout Protection

TPS51518 has a 5-V supply undervoltage lockout protection (UVLO) threshold. When the V5IN voltage is lower than UVLO threshold voltage, typically 4.0 V, V_{OUT} is shut off. This is a non-latch protection.

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Thermal Shutdown

TPS51518 includes an internal temperature monitor. If the temperature exceeds the threshold value, 140°C (typ), V_{OUT} is shut off. The state of V_{OUT} is open at thermal shutdown. This is a non-latch protection and the operation is restarted with soft-start sequence when the device temperature is reduced by 10°C (typ).

Layout Considerations

Certain issues must be considered before designing a layout using the TPS51518.

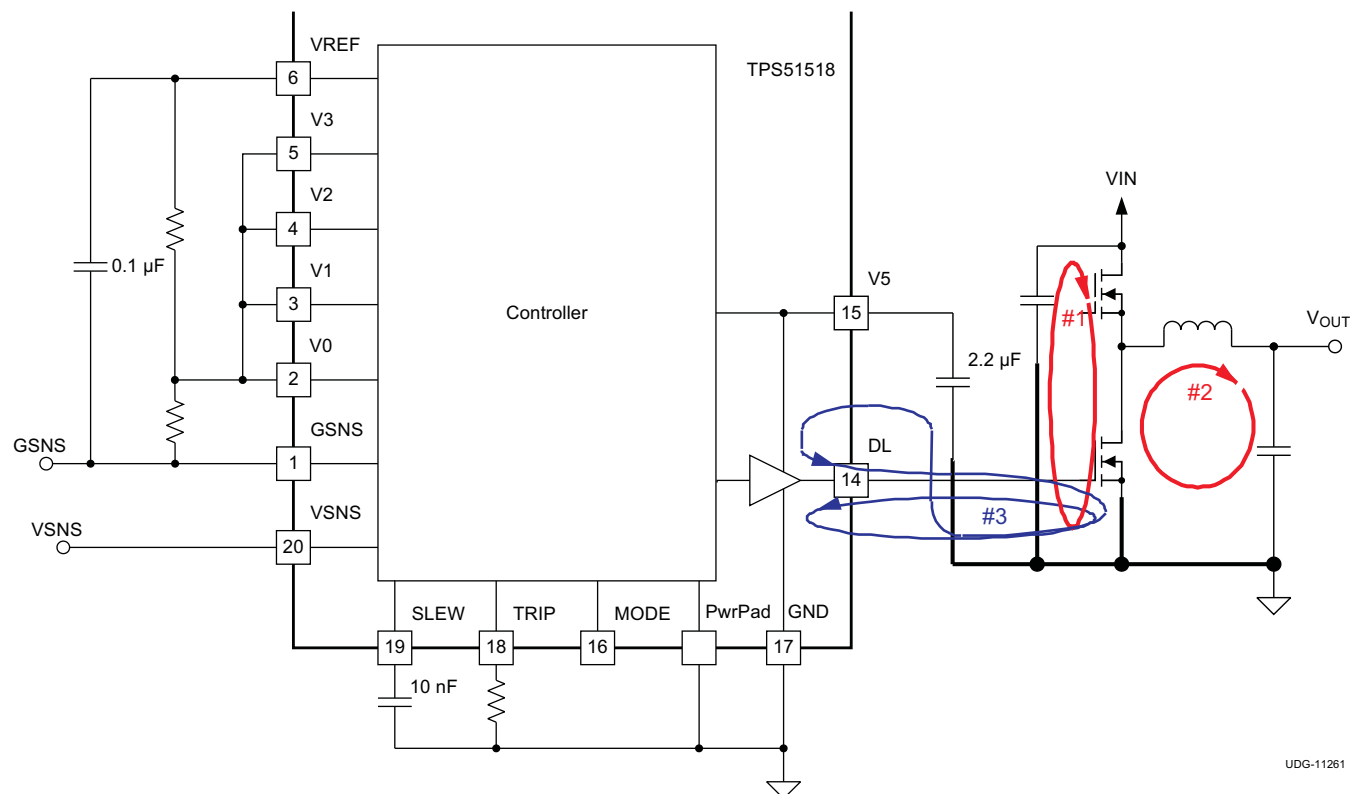


Figure 26. DC/DC Converter Ground System

- V_{IN} capacitor(s), V_{OUT} capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VSNS, SLEW, MODE, V0, V1, V2, V3, VREF and TRIP should be placed away from high-voltage switching nodes such as SW, DH, DL or BST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
 - Loop #1. The most important loop to minimize the area of is the path from the V_{IN} capacitor(s) through the high and low-side MOSFETs, and back to the capacitor(s) through ground. Connect the negative node of the V_{IN} capacitor(s) and the source of the low-side MOSFET at ground as close as possible. (Refer to loop #1 of Figure 26)
 - Loop #2. The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of V_{OUT} capacitor(s) at ground as close as possible. (Refer to loop #2 of Figure 26)
 - Loop #3. The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from V5 capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current

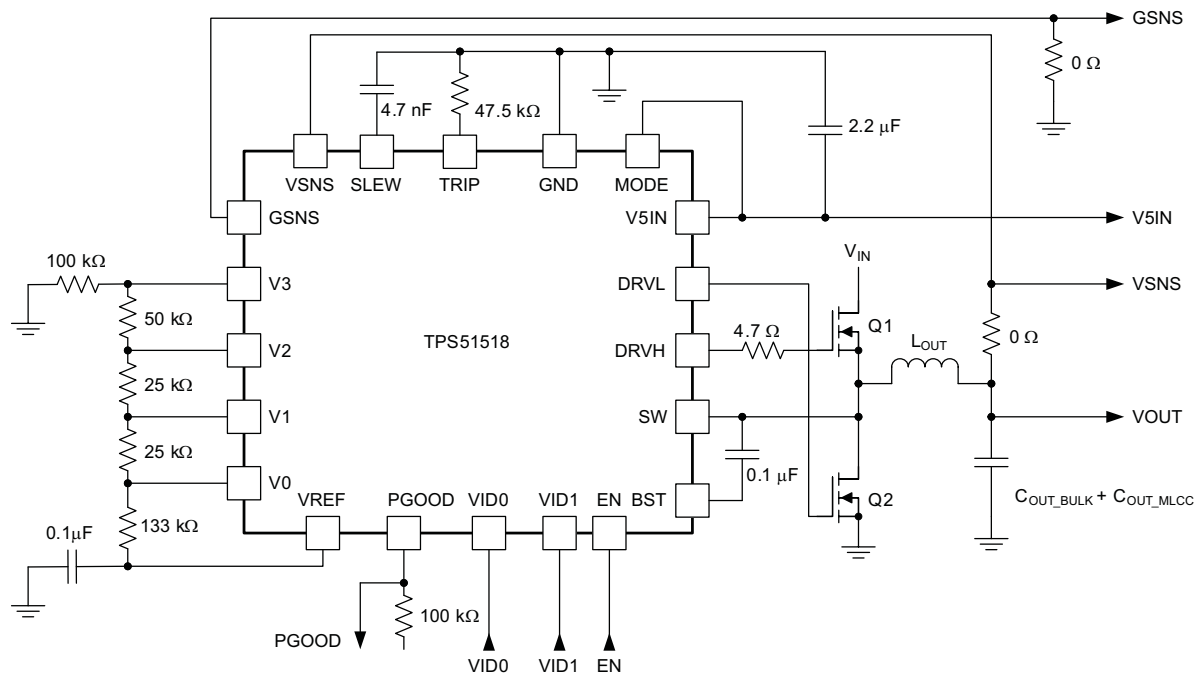
flows from gate of the low-side MOSFET through the gate driver and PGND, and back to source of the low-side MOSFET through ground. Connect negative node of V5 capacitor, source of the low-side MOSFET and PGND at ground as close as possible. (Refer to loop #3 of [Figure 26](#))

- VSNS can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side. For additional noise filtering, insert a 10- Ω , 1-nF, R-C filter between the sense point and the VSNS pin. Connect GSNS to ground return point at the load device or the general ground plane/layer. VSNS and GSNS can be used for the purpose of remote sensing across the load device, however, care must be taken to minimize the routing trace to prevent excess noise injection to the sense lines.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as SW node, which connects to the source of the switching MOSFET, the drain of the rectifying MOSFET and the high-voltage side of the inductor, should be as short and wide as possible.
- In order to effectively remove heat from the package, prepare the thermal land and solder to the package thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps to dissipate heat. Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation.

DESIGN EXAMPLES

This section describes three different applications for the TPS51518 controller. Design 1 is a 2-Bit VID $I_{CC(max)} = 25$ A, D-CAP2™, 350-kHz application. Design 2 is a 2-Bit VID $I_{CC(max)} = 2.5$ A, D-CAP2™, 350-kHz application. Design 3 is a 2-Bit VID $I_{CC(max)}$ D-CAP2™, 350-kHz for Intel Chief River System Agent application (SV processor).

Design 1: 2-Bit VID $I_{CC(max)} = 25$ A, D-CAP2™, 350-kHz Application



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Figure 27. Application Circuit for Design 1

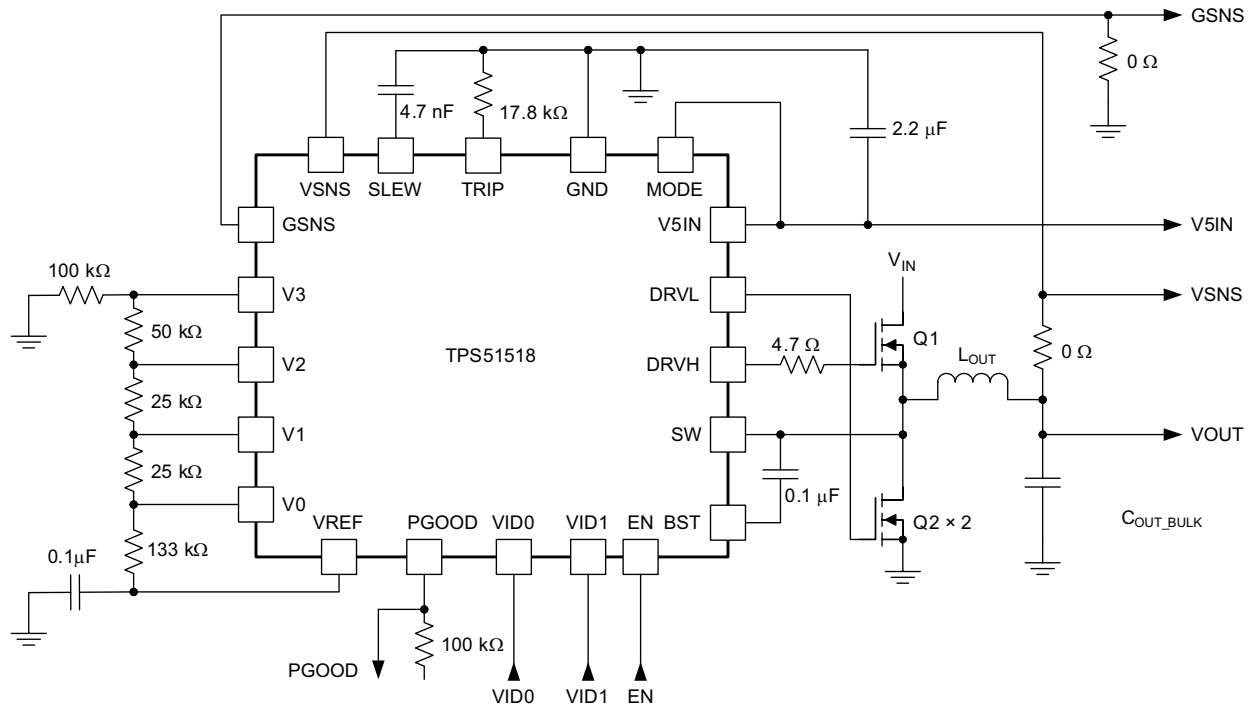
Table 3. VID Table for Design 1

VID1	VID0	OUTPUT VOLTAGE (V)
0	0	1.2
0	1	1.05
1	0	0.9
1	1	0.6

Table 4. List of Materials for Design 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C _{IN} (not shown)	4	10 μ F, 25 V	Taiyo Yuden	TMK325BJ106MM
C _{OUT_BULK}	3	330 μ F, 2.5 V, 9 m Ω	Sanyo	2TPE330M9
C _{OUT_MLCC}	10	22 μ F, 6.3 V	Murata	GRM21BB30J226ME38
L _{OUT}	1	0.45 μ H, 17 A, 1.1 m Ω	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 7.3 m Ω	Texas Instruments	CSD17302Q5A
Q2	2	30 V, 3.3 m Ω	Texas Instruments	CSD17306Q5A

Design 2: 2-Bit VID $I_{CC(max)} = 25\text{ A}$, D-CAP™, 350-kHz, Application Circuit



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Figure 28. Application Circuit for Design 2

Table 5. VID Table for Design 2

VID1	VID0	OUTPUT VOLTAGE (V)
0	0	1.2
0	1	1.05
1	0	0.9
1	1	0.6

Table 6. List of Materials for Design 2

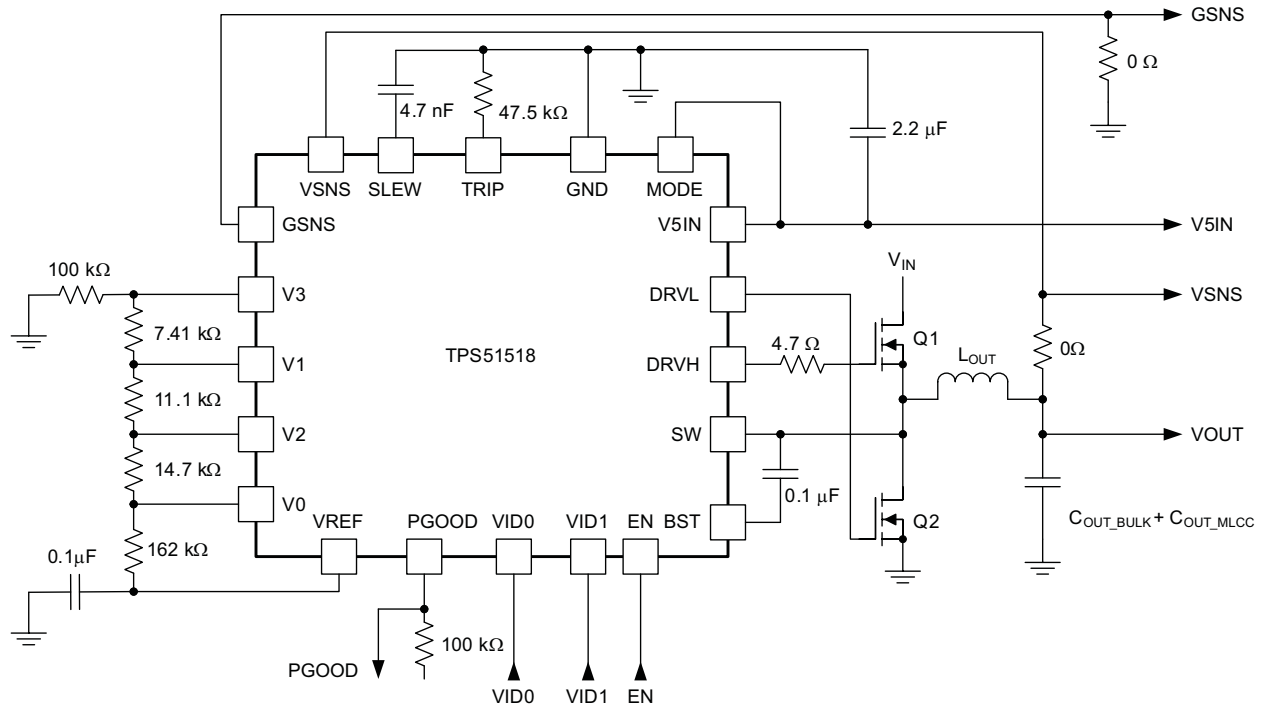
REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C _{IN} (not shown)	4	10 μF, 25 V	Taiyo Yuden	TMK325BJ106MM
C _{OUT_BULK}	3	330 μF, 2.5 V, 9 mΩ	Sanyo	2TPE330M9
L _{OUT}	1	0.45 μH, 17 A, 1.1 mΩ	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 7.3 mΩ	Texas Instruments	CSD17302Q5A
Q2	2	30 V, 3.3 mΩ	Texas Instruments	CSD17306Q5A

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Design 3: 2-Bit VID, $I_{CC(max)} = 6$ A, D-CAP2™ 350-kHz for Intel Chief River System Agent Application (SV Processor)



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Figure 29. Application Circuit for Design 3

Table 7. VID Table for Design 3

VID1	VID0	OUTPUT VOLTAGE (V)
0	0	0.9
0	1	0.8
1	0	0.725
1	1	0.675

Table 8. List of Materials for Design 3

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C _{IN} (not shown)	2	10 μF, 25 V	Taiyo Yuden	TMK325BJ106MM
C _{OUT_BULK}	1	220 μF, 2.5 V, 9 mΩ	Sanyo	2TPE330M9
C _{OUT_MLCC}	1	22 μF, 6.3 V	Murata	GRM21BB30J226ME38
L _{OUT}	1	1.5 μH, 10 A, 9.7 mΩ	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 7.3 mΩ	Texas Instruments	CSD17302Q5A
Q2	1	30 V, 3.3 mΩ	Texas Instruments	CSD17306Q5A

DESIGN PROCEDURE

The simplified design procedure is done for a system agent rail for IMVP7 Intel platform application using the TPS51518 controller.

Step One: Determine the specifications.

The system agent rail requirements provide the following key parameters:

- $V_{00} = 0.90 \text{ V}$
- $V_{01} = 0.725 \text{ V}$
- $V_{10} = 0.80 \text{ V}$
- $V_{11} = 0.675 \text{ V}$
- $I_{CC(max)} = 6 \text{ A}$
- $I_{DYN(max)} = 2 \text{ A}$

Step Two: Determine system parameters.

The input voltage range and operating frequency are of primary interest.

In this example:

- $9 \text{ V} \leq V_{IN} \leq 20 \text{ V}$
- $f_{SW} = 350 \text{ kHz}$

Step Three: Determine inductor value and choose Inductor.

Smaller values of inductor have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 25% to 50% of the maximum current. In this example, use 25%:

$$I_{P-P} = 6 \text{ A} \times 0.25 = 1.5 \text{ A}$$

At $f_{SW} = 350 \text{ kHz}$ with a 20-V input and a 0.80-V output:

$$L = \frac{V \times dT}{I_{P-P}} = \frac{(V_{IN} - V_{OUT}) \times \left(\frac{V_{10}}{f_{SW} \times V_{IN}} \right)}{I_{P-P}} = \frac{(20 \text{ V} - 0.8 \text{ V}) \times \left(\frac{0.8 \text{ V}}{350 \text{ kHz} \times 20 \text{ V}} \right)}{1.5 \text{ A}} \quad (10)$$

For this application, a 1.5-μH, 9.7-mΩ inductor from TDK with part number SPM6530T-1R5M100 is used.

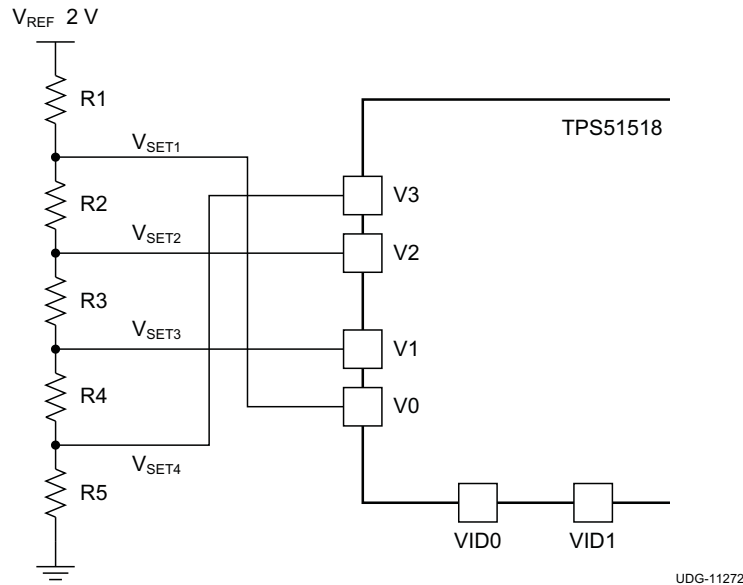
Step Four: Set the output voltages.

Set the output voltage levels. for V0, V1, V2 and V3 pins).

- VID 00, V0 = $V_{SET1} = 0.9 \text{ V}$
- VID 10, V2 = $V_{SET2} = 0.8 \text{ V}$
- VID 01, V1 = $V_{SET3} = 0.725 \text{ V}$
- VID 11, V3 = $V_{SET4} = 0.675 \text{ V}$

Follow the TPS51518 Design Tool_1.0.xls (in the **VID_Config** section) to determine the resistor values:

- $V_{REF} = 2 \text{ V}$
- $R1 = 162 \text{ k}\Omega$
- $R2 = 14.7 \text{ k}\Omega$
- $R3 = 11.1 \text{ k}\Omega$
- $R4 = 7.41 \text{ k}\Omega$
- $R5 = 100 \text{ k}\Omega$


Figure 30. Setting the Output Voltage
Step Five: Calculate SLEW capacitance.

SLEW can be used to program the soft-start time and voltage transition timing. During soft-start operation, the current source used to program the SLEW rate is 10 μA (nominal). During VID transition, the current source is switched to a higher current of 50 μA .

In this design example, the requirement is to complete VID_00 to VID_11 transition within 20 μs , calculate the SLEW capacitance based on Equation 11.

$$C_{\text{SLEW}} = I \times \frac{dt}{dV} = 50 \mu\text{A} \times \frac{20 \mu\text{s}}{0.9\text{V} - 0.675\text{V}} = 4.7\text{nF} \quad (11)$$

For $V_{\text{OUT}} = 0.9\text{V}$, the soft start timing based on C_{SLEW} is 423 μs .

The slower slew rate is desired to minimize large inductor current perturbation during startup and voltage transition, thus reducing the possibility of acoustic noise.

Step Six

TPS51518 uses a low-side on-resistance ($R_{\text{DS(on)}}$) sensing scheme. The TRIP pin sources 10 μA of current and the trip level is set to 1/8 of the voltage across the TRIP resistor (R_{TRIP}). The overcurrent trip level is determined by $R_{\text{TRIP}} \times (I_{\text{TRIP}}/8)$. Because the comparison is done during the off state, the trip voltage sets the valley current. The load current can be calculated by considering the inductor ripple current.

$$R_{\text{TRIP}} = \frac{8 \times \left(I_{\text{OCL}} - \left(\frac{(V_{\text{IN}} - V_{\text{OUT}})}{(2 \times Lx)} \right) \times \frac{(V_{\text{OUT}})}{(f_{\text{SW}} \times V_{\text{IN}})} \right) \times R_{\text{DS(on)}}}{I_{\text{TRIP}}}$$

where

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- f_{SW} is the switching frequency (350 kHz)
- $R_{\text{DS(on)}}$ is the low-side FET on resistance
- I_{TRIP} is the trip current, 10 μA (nominal)
- Lx is the output inductance

(12)

Step Seven: Determine the output capacitance.

D-CAP™ Mode

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine the ESR value to meet small signal stability and recommended ripple voltage. A quick reference is shown in [Equation 13](#) and [Equation 14](#).

$$f_0 = \frac{1}{2\pi \times \text{ESR} \times C_{\text{OUT}}} \leq \frac{f_{\text{SW}}}{3} \quad (13)$$

$$\frac{g_M \times \text{ESR}}{2 \times \pi \times C_1} \leq \frac{f_0}{10}$$

where

- g_M is the 60 μS
- C_1 is the SLEW capacitance

(14)

$$\frac{V_{\text{OUT}} \times \text{ESR}}{f_{\text{SW}} \times L_x} \geq 20\text{mV} \quad (15)$$

D-CAP2™ Mode

The switching frequency for D-CAP2™ mode is 350 kHz and it is generally recommend to have a unity gain crossover (f_0) of 1/4 or 1/3 of the switching frequency, which is approximately 90 kHz to 120kHz for the purpose of this application.

$$f_0 = \frac{f_{\text{SW}}}{3} = 90\text{kHz} \quad \text{or} \quad f_0 = \frac{f_{\text{SW}}}{4} = 120\text{kHz} \quad (16)$$

Given the range of the recommended unity gain frequency, the power stage design is flexible, as long as the LC double pole frequency is less than 10% of f_0 .

$$f_{\text{LC}} = \frac{1}{2\pi\sqrt{L_{\text{OUT}} \times C_{\text{OUT}}}} \leq \frac{1}{10} \times f_0 = 9\text{kHz} \Leftrightarrow 12\text{kHz} \quad (17)$$

As long as the LC double pole frequency is designed to be less than 1/10 of f_0 , the internal compensation network provides sufficient phase boost at the unity gain crossover frequency in order for the converter to be stable with enough margin ($> 60^\circ$).

When the ESR frequency of the output bulk capacitor is in the vicinity of the unity gain crossover frequency of the loop, additional phase boost is achieved. This applies to POSCAP and/or SPCAP output capacitors.

When the ESR frequency of the output capacitor is beyond the unity gain crossover frequency of the loop, no additional phase boost is achieved. This applies to low/ultra low ESR output capacitors, such as MLCCs.

[Equation 18](#) and [Equation 19](#) can be used to estimate the amount of capacitance needed for a given dynamic load step/release. Note that there are other factors that may impact the amount of output capacitance for a specific design, such as ripple and stability. [Equation 18](#) and [Equation 19](#) are used only to estimate the transient requirement, the result should be used in conjunction with other factors of the design to determine the necessary output capacitance for the application.

$$C_{\text{OUT(min_under)}} = \frac{L \times (\Delta I_{\text{LOAD(max)}})^2 \times \left(\frac{V_{\text{OUT}} \times t_{\text{SW}}}{V_{\text{IN(min)}}} + t_{\text{MIN(off)}} \right)}{2 \times \Delta V_{\text{LOAD(insert)}} \times \left(\left(\frac{V_{\text{IN(min)}} - V_{\text{OUT}}}{V_{\text{IN(min)}}} \right) \times t_{\text{SW}} - t_{\text{MIN(off)}} \right) \times V_{\text{OUT}}} \quad (18)$$

$$C_{\text{OUT(min_over)}} = \frac{L_{\text{OUT}} \times (\Delta I_{\text{LOAD(max)}})^2}{2 \times \Delta V_{\text{LOAD(release)}} \times V_{\text{OUT}}} \quad (19)$$

[Equation 18](#) and [Equation 19](#) calculate the minimum C_{OUT} for meeting the transient requirement, which is 72.9 μF assuming $\pm 3\%$ voltage allowance for load step and release.

TPS51518

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Step Eight: Select decoupling and peripheral components.

For the TPS51518, peripheral capacitors use the following minimum values of ceramic capacitance. X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always appropriate.

- V5IN decoupling $\geq 2.2 \mu\text{F}$, $\geq 10 \text{ V}$
- VREF decoupling $0.22 \mu\text{F}$ to $1 \mu\text{F}$, $\geq 4 \text{ V}$
- Bootstrap capacitors $\geq 0.1 \mu\text{F}$, $\geq 10 \text{ V}$
- Pull-up resistors on PGOOD, $100 \text{ k}\Omega$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51518RUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-10 to 105	51518	Samples
TPS51518RUKT	ACTIVE	WQFN	RUK	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-10 to 105	51518	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

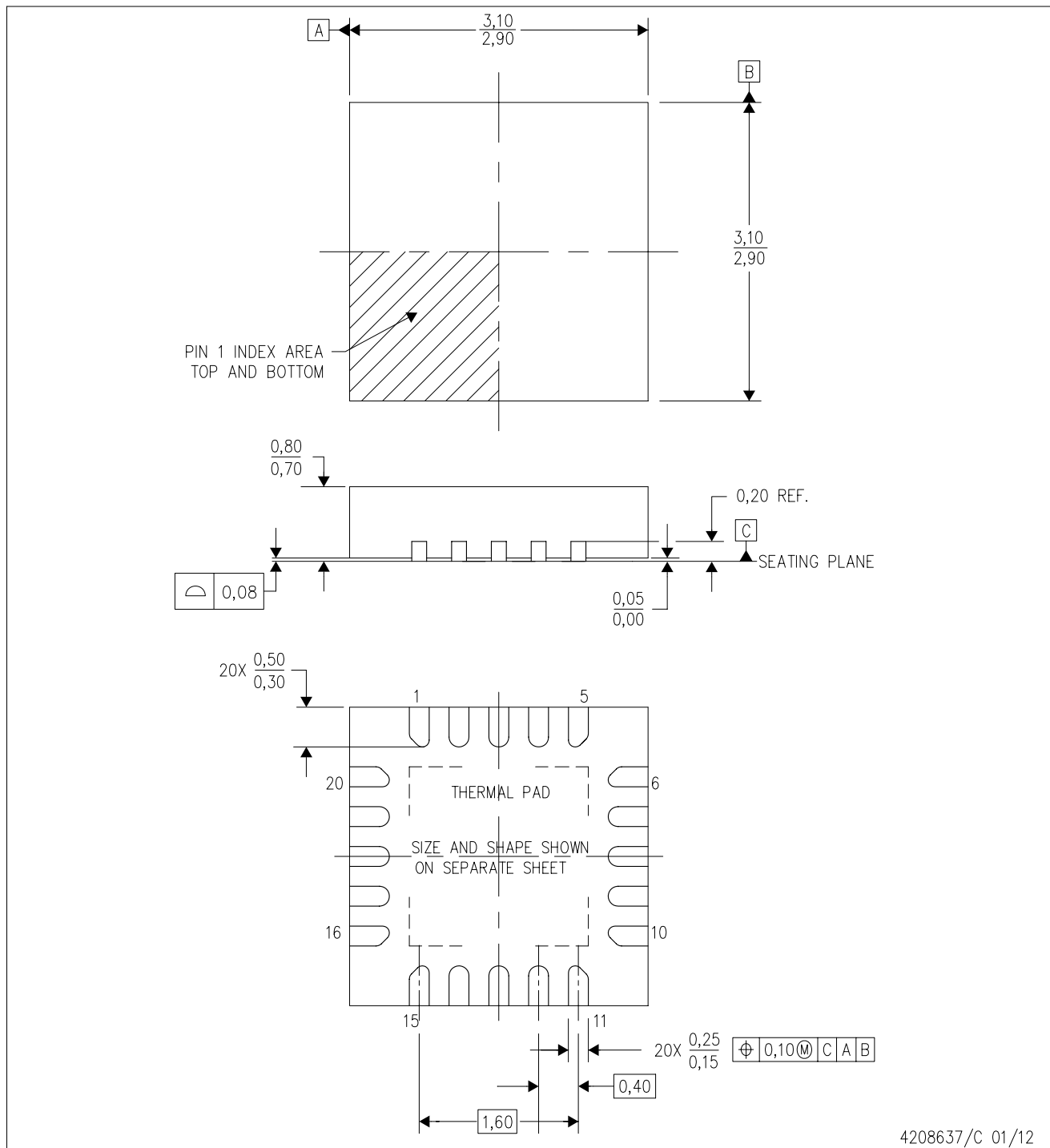
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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RUK (S-PWQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

RUK (S-PWQFN-N20)

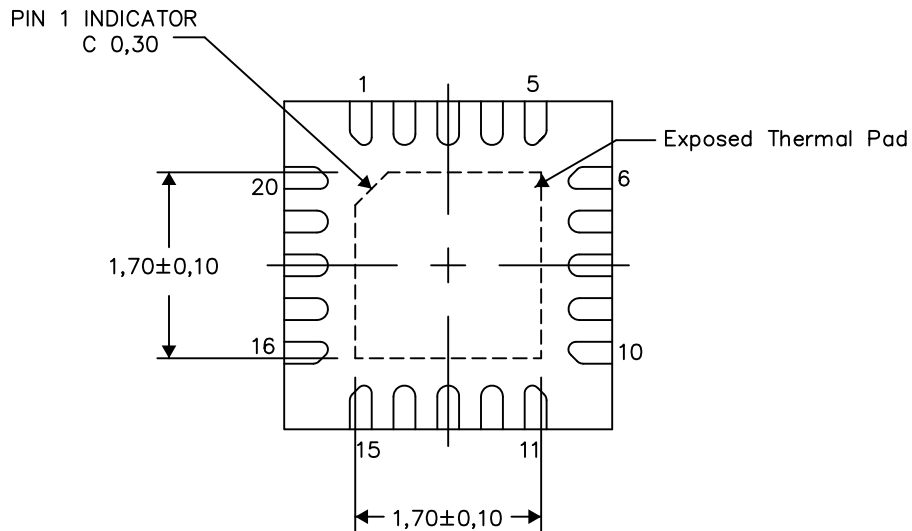
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

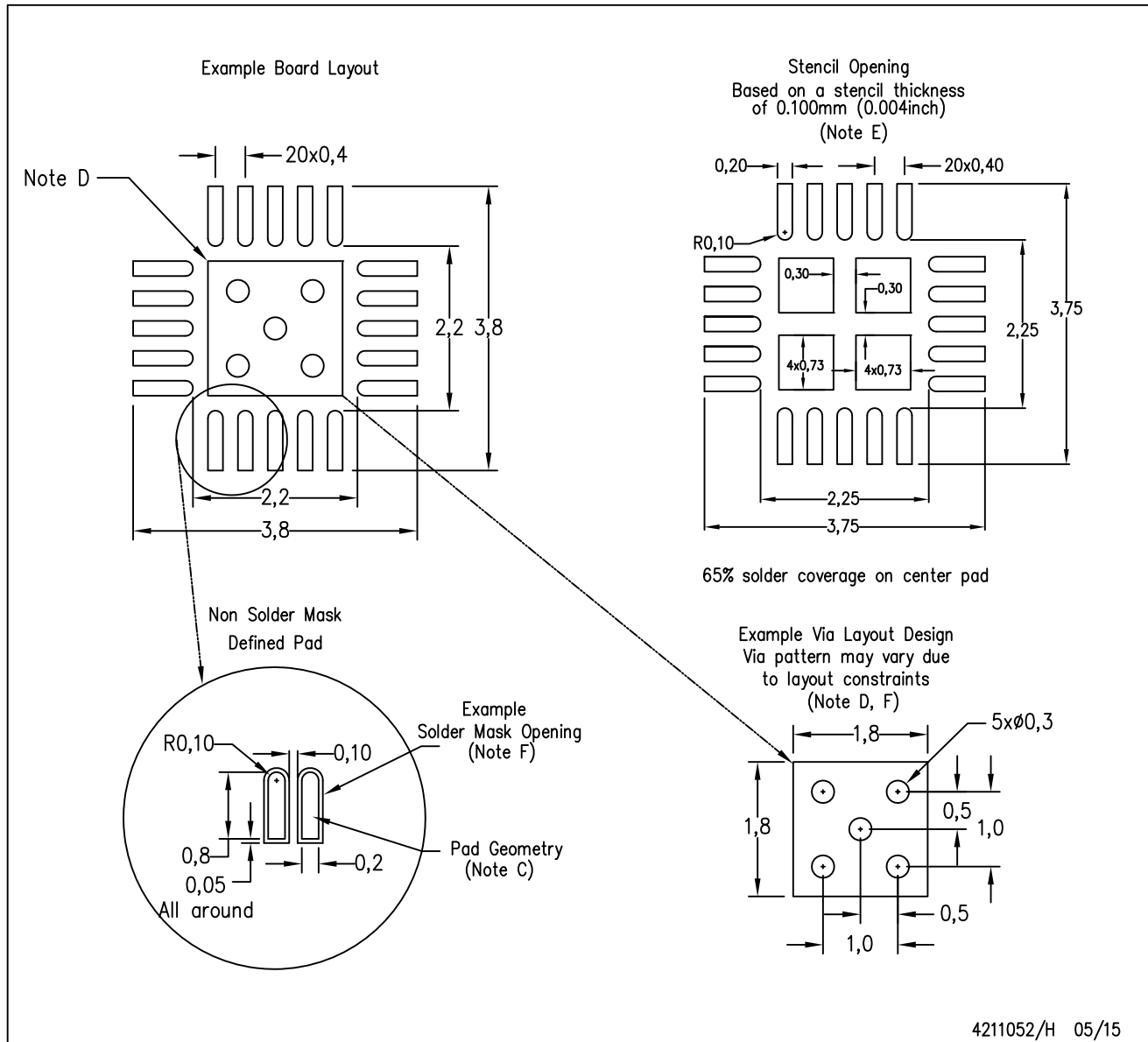
Exposed Thermal Pad Dimensions

4209762/1 05/15

NOTE: All linear dimensions are in millimeters

RUK (S-PWQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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