μA741 通用运算放大器

1 特性

- 短路保护
- 失调电压清零功能
- 宽泛的共模和差分电压范围
- 无需频率补偿
- 无锁存

2 应用

- DVD 录像机和播放器
- 专业音频混合器

3 说明

μA741 器件是一款具有失调电压清零功能的通用运算放大器。

此放大器具有高共模输入电压范围且无锁存，因此是电压跟随器 应用的理想选择。该器件
具有短路保护功能，并且内部频率补偿可在无需外部组件的情况下确保稳定性。失调电压清零输入之间可以连接一个低值电位器，从而将失调电压清零，如图 12 所示。

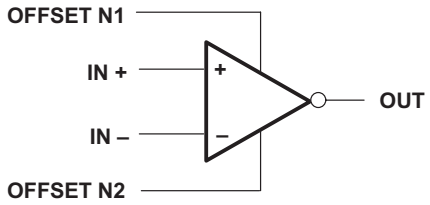
μA741C 器件的额定工作温度范围是 0°C 至 70°C。

器件信息(1)

部件号	封装	封装尺寸（标称值）
μA741CD	SOIC (8)	4.90mm × 3.91mm
μA741CP	PDIP (8)	9.81mm × 6.35mm
μA741CPS	SO (8)	6.20mm × 5.30mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

Changes from Revision F (May 2017) to Revision G **Page**

- Changed supply voltage unit from "°C" to "V" in *Absolute Maximum Ratings* table ... 5

Changes from Revision E (January 2015) to Revision F **Page**

- 根据最新文档和翻译标准更新了数据表文本 ... 1
- 已删除 *说明* 部分中有关 µA741M 器件（过时的封装）的文本 ... 1
- 已添加 向*器件信息* 表添加了 µA741CD、µA741CP 和 µA741CPS 器件 ... 1
- 已删除 从*器件信息* 表删除了 µA741x 器件 ... 1
- Updated pinout diagrams and *Pin Functions* tables in the *Pin Configurations and Functions* section ... 4
- Deleted µA741M pinout drawings information from *Pin Configurations and Functions* section ... 4
- Deleted Electrical Characteristics: µA741M table from *Specifications* section ... 5
- Added operating junction temperature (T_J) and values to *Absolute Maximum Ratings* table ... 5
- Deleted text regarding µA741M from *Absolute Maximum Ratings* table ... 5
- Deleted text regarding µA741M device from *Recommended Operating Conditions* table ... 5
- Deleted *Dissipation Ratings* table ... 5
- Added *Thermal Information* table and values ... 5
- Deleted µA741M in *Switching Characteristics* table ... 7
- Correct typo in 图 1 ... 8
- 已删除 text regarding µA741M device from *Detailed Description* section ... 10
- Updated text in *Overview* section ... 10
- 已添加 2017 copyright to *Functional Block Diagram* ... 10
- 已添加 caption to 图 11 in *Device Functional Modes* section ... 11
- 已更改 pins 1 and 5 from "NC" to "Offset N1" and "Offset N2" in 图 18 ... 15

Changes from Revision D (February 2014) to Revision E **Page**

- 添加了*应用*、*器件信息* 表、*引脚功能* 表、*ESD 额定值* 表、*热性能信息* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 1
- Moved *Typical Characteristics* into *Specifications* section. 8

Changes from Revision C (January 2014) to Revision D **Page**

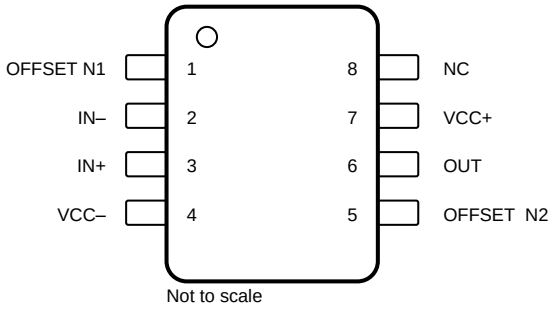
- Fixed *Typical Characteristics* graphs to remove extra lines. 8

Changes from Revision B (September 2000) to Revision C **Page**

- 将文档更新为新的 TI 数据表格式 - 无规格变化。 1
- 已删除 *订购信息* 表。 1

5 Pin Configurations and Functions

uA741C D, P, or PS Package
8-Pin SOIC, PDIP, SO
Top View



Not to scale

NC- no internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN–	2	I	Inverting input
NC	8	—	No internal connection
OFFSET N1	1	I	External input offset voltage adjustment
OFFSET N2	5	I	External input offset voltage adjustment
OUT	6	O	Output
VCC+	7	—	Positive supply
VCC–	4	—	Negative supply

6 Specifications

6.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_{CC}(2)	µA741C		–18	18	V
Differential input voltage, V_{ID}(3)	µA741C		–15	15	V
Input voltage, V_I (any input) (2)(4)	µA741C		–15	15	V
Voltage between offset null (either OFFSET N1 or OFFSET N2) and $V_{CC–}$	µA741C		–15	15	V
Duration of output short circuit(5)			Unlimited		
Continuous total power dissipation			See *Thermal Information*		
Case temperature for 60 seconds		µA741C	N/A	N/A	°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds		µA741C	N/A	N/A	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, P, or PS package	µA741C		260	°C
Operating junction temperature, T_J				150	°C
Storage temperature range, T_{stg}		µA741C	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or either power supply.

6.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$			–5	–15	
T_A	Operating free-air temperature	µA741C	0	70	°C

6.3 Thermal Information

THERMAL METRIC(1)		µA741			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.2	87.4	119.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.6	89.3	66	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	64.4	70	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.9	49.8	27.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.7	64.1	69	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.4 Electrical Characteristics: µA741C

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6	mV
			Full range			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		±15		mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200	nA
			Full range			300	
I_{IB}	Input bias current	V_O = 0	25°C		80	500	nA
			Full range			800	
V_{ICR}	Common-mode input voltage range	25°C		±12	±13		V
		Full range		±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			
		R_L = 2 kΩ	25°C	±10			
		R_L ≥ 2 kΩ	Full range	±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	25°C	20	200		V/mV
		V_O = ±10 V	Full range	15			
r_i	Input resistance	25°C		0.3	2		MΩ
r_o	Output resistance	V_O = 0; see[2]	25°C		75		Ω
C_i	Input capacitance	25°C			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	25°C	70	90		dB
			Full range	70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150	µV/V
			Full range			150	
I_{OS}	Short-circuit output current	25°C			±25	±40	mA
I_{CC}	Supply current	V_O = 0; no load	25°C		1.7	2.8	mA
			Full range			3.3	
P_D	Total power dissipation	V_O = 0; no load	25°C		50	85	mW
			Full range			100	

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C.
(2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

6.5 Electrical Characteristics: µA741Y

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0		1	5	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0		±15		mV
I_{IO}	Input offset current	V_O = 0		20	200	nA
I_{IB}	Input bias current	V_O = 0		80	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	±12	±14		V
		R_L = 2 kΩ	±10	±13		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	20	200		V/mV
r_i	Input resistance		0.3	2		MΩ
r_o	Output resistance	V_O = 0; see(1)		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V		30	150	µV/V
I_{OS}	Short-circuit output current			±25	±40	mA
I_{CC}	Supply current	V_O = 0; no load		1.7	2.8	mA
P_D	Total power dissipation	V_O = 0; no load		50	85	mW

(1) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.
(2) All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

6.6 Switching Characteristics: µA741C

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ C_L = 100 pF; see 图 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ C_L = 100 pF; see 图 1		0.5		V/µs

6.7 Switching Characteristics: µA741Y

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ C_L = 100 pF; see 图 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ C_L = 100 pF; see 图 1		0.5		V/µs

6.8 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

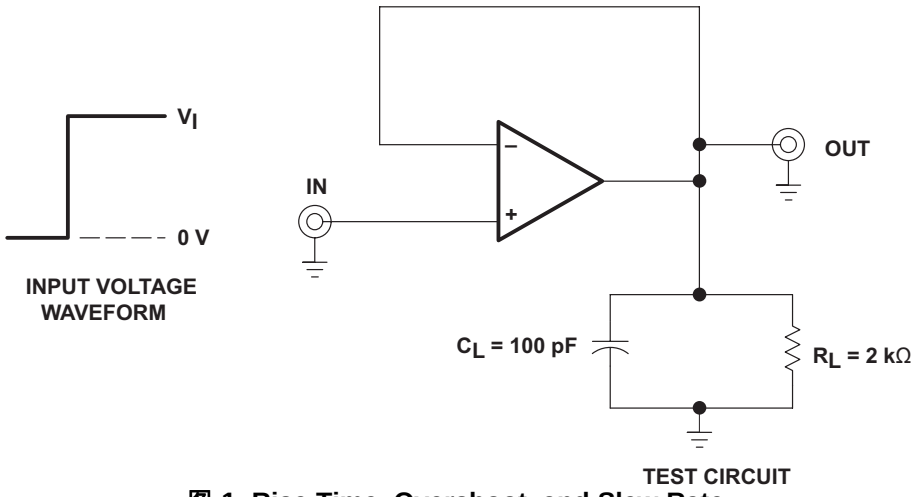


图 1. Rise Time, Overshoot, and Slew Rate

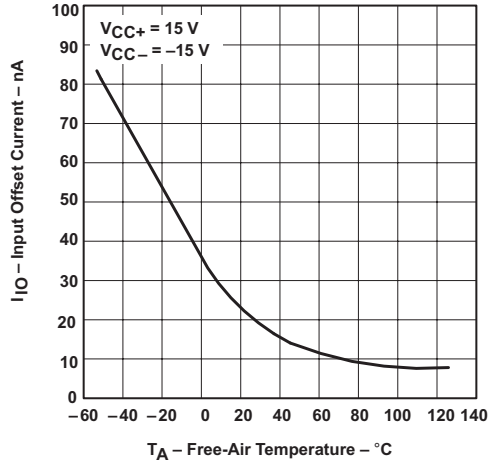


图 2. Input Offset Current vs Free-Air Temperature

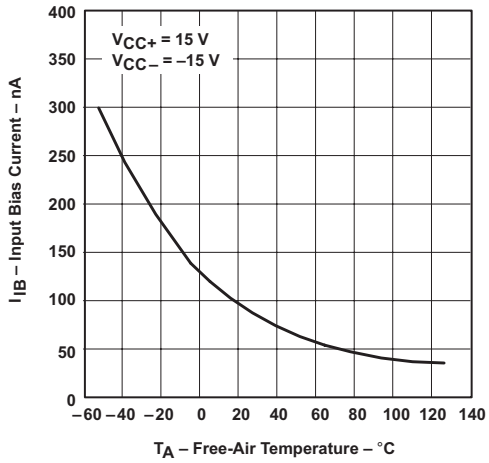


图 3. Input Bias Current vs Free-Air Temperature

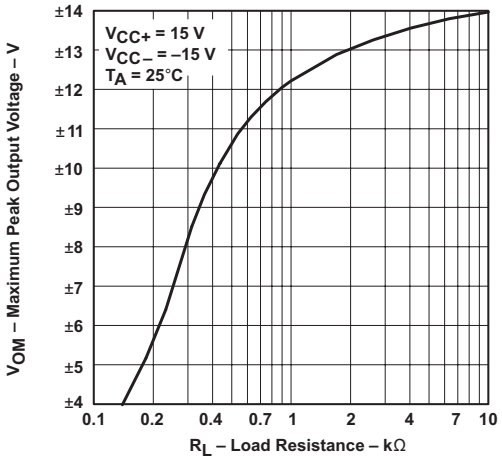


图 4. Maximum Output Voltage vs Load Resistance

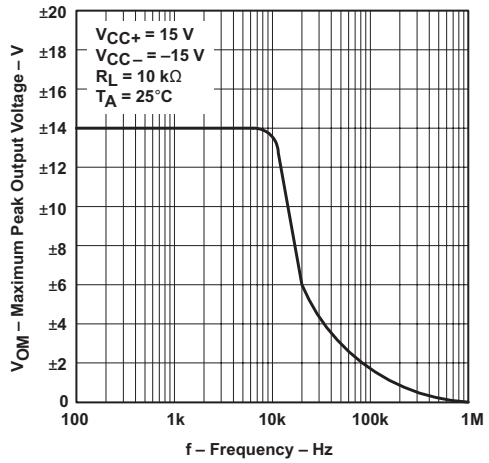


图 5. Maximum Peak Output Voltage vs Frequency

Typical Characteristics (接下页)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

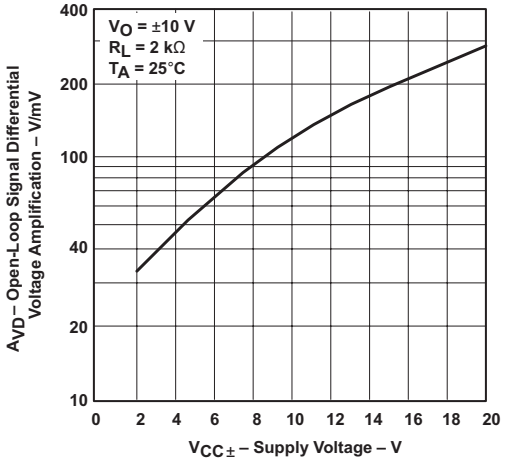


图 6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage

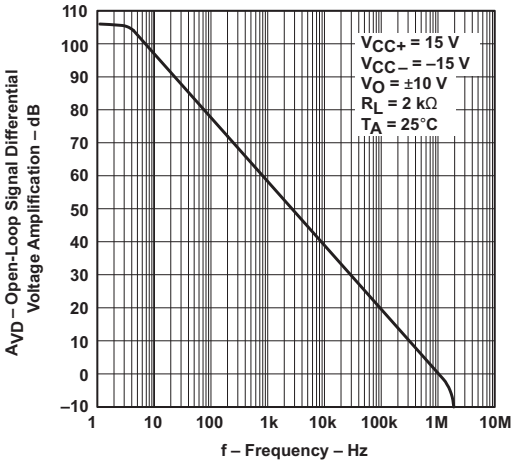


图 7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency

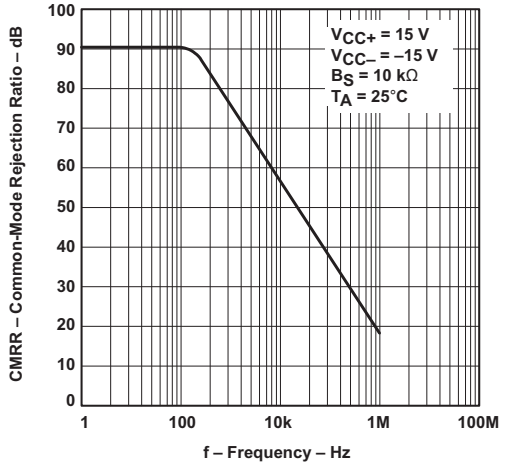


图 8. Common-Mode Rejection Ratio vs Frequency

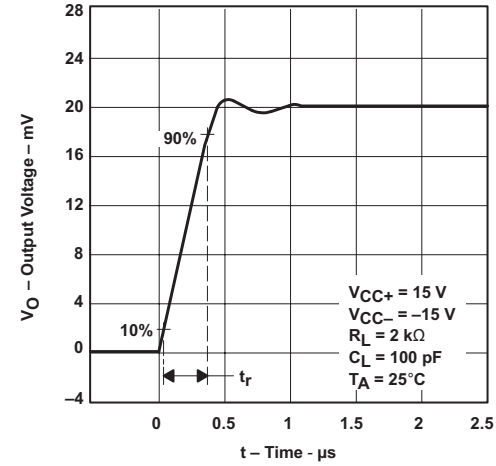


图 9. Output Voltage vs Elapsed Time

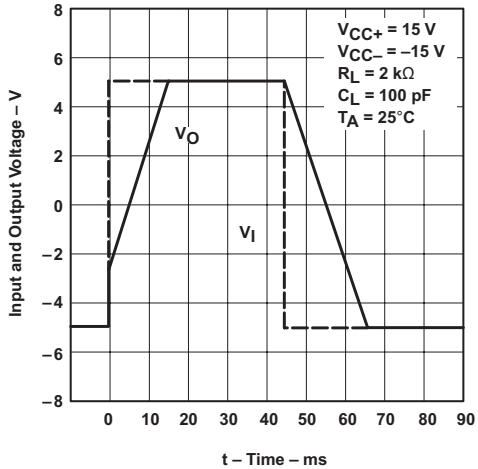


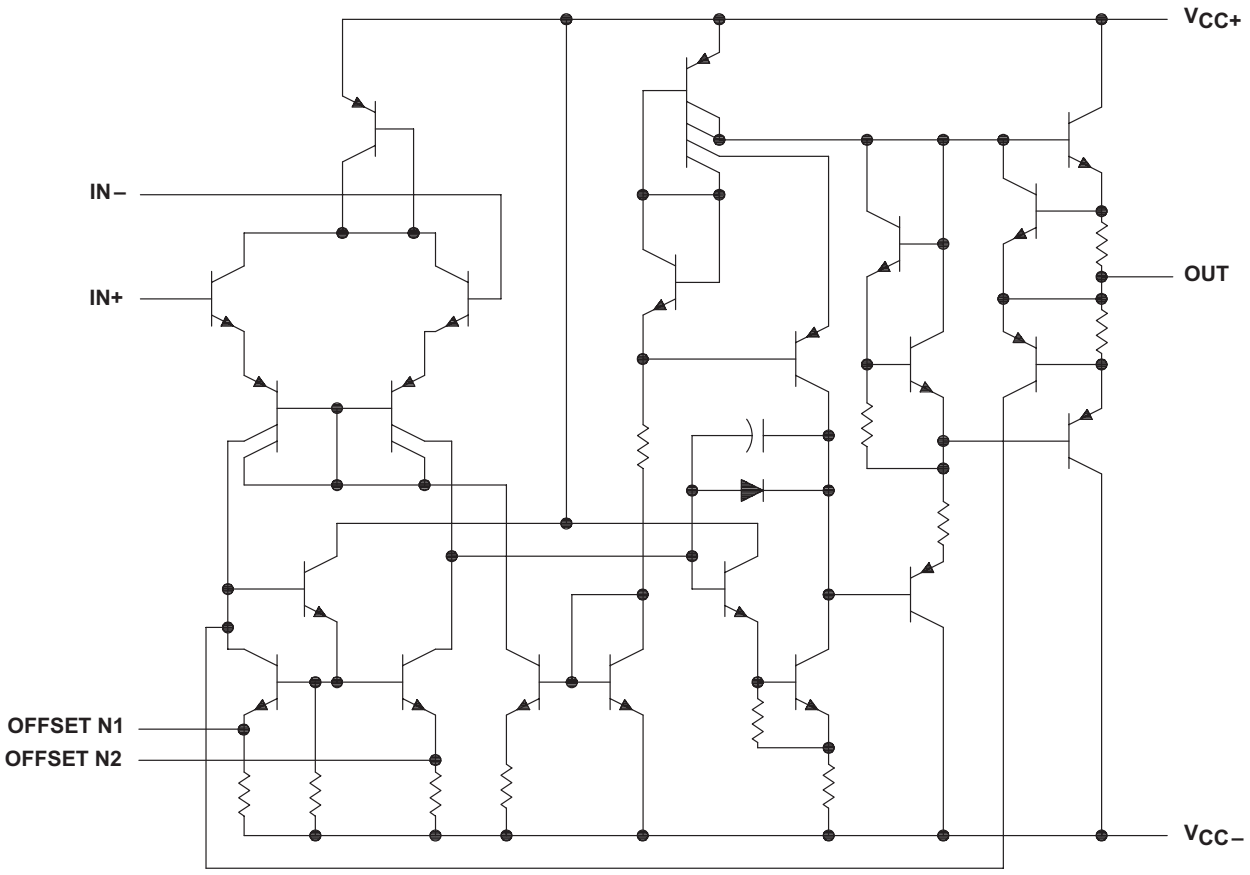
图 10. Voltage-Follower Large-Signal Pulse Response

7 Detailed Description

7.1 Overview

The μA741 has been a popular operational amplifier for over four decades. Typical open loop gain is 106 dB while driving a 2000-Ω load. Short circuit tolerance, offset voltage trimming, and unity-gain stability makes the μA741 useful for many applications.

7.2 Functional Block Diagram



Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

7.3 Feature Description

7.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches caused by external circuitry. See *Application and Implementation* for more details on design techniques.

Feature Description (接下页)

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change an output when there is a change on the input. The µA741 device has a 0.5-V/µs slew rate. Parameters that vary significantly with operating voltages or temperature are shown in *Typical Characteristics*.

7.4 Device Functional Modes

The µA741 device is powered on when the power supply is connected. The device can operate as a single-supply or dual-supply operational amplifier depending on the application.

7.5 µA741Y Chip Information

When properly assembled, this chip displays characteristics similar to the µA741C device. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.

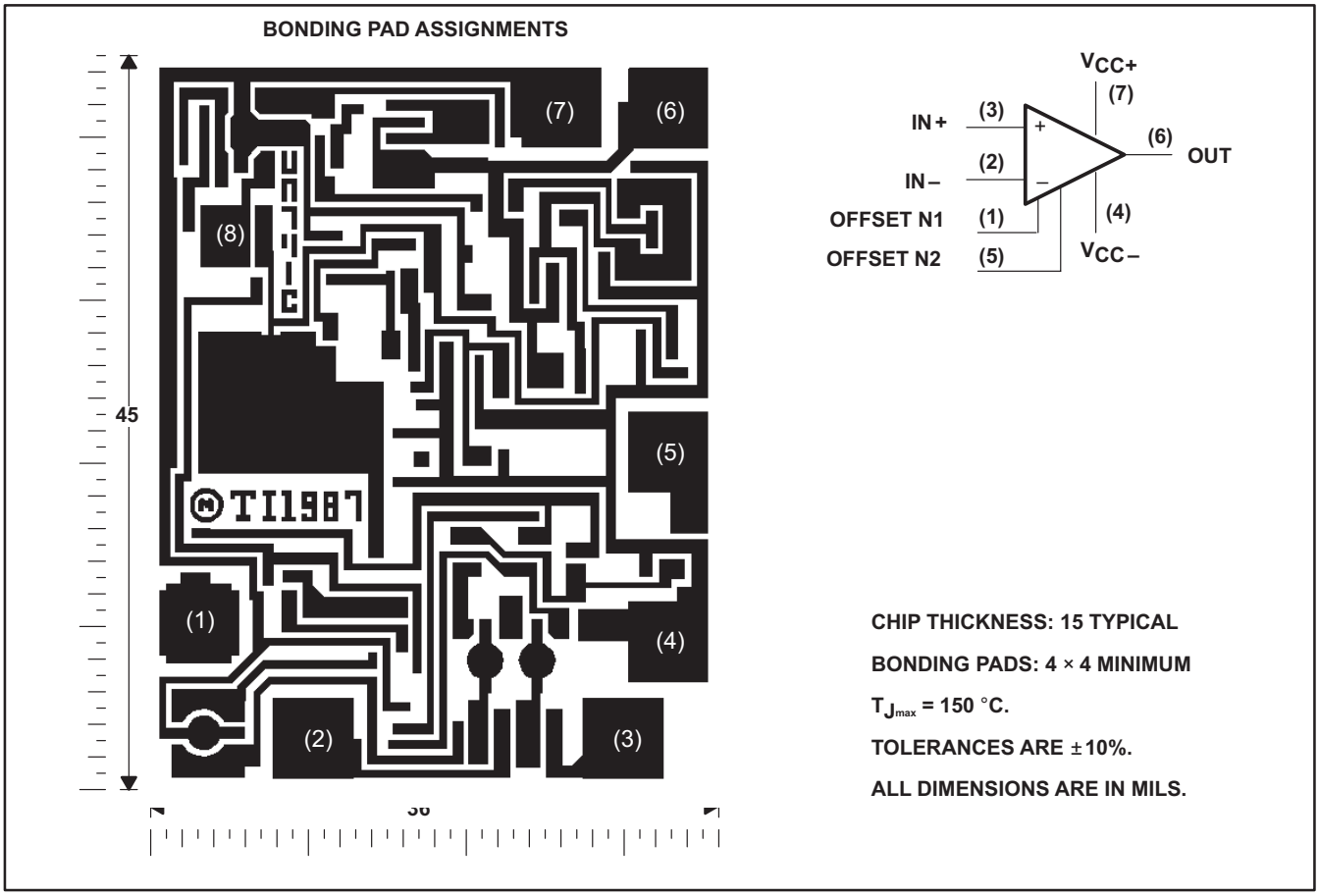


图 11. Bonding Pad Assignments

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches resulting from external circuitry. These input mismatches can be adjusted by placing resistors or a potentiometer between the inputs as shown in 图 12. A potentiometer can fine-tune the circuit during testing or for applications which require precision offset control. For more information about designing using the input-offset pins, see *Nulling Input Offset Voltage of Operational Amplifiers*.

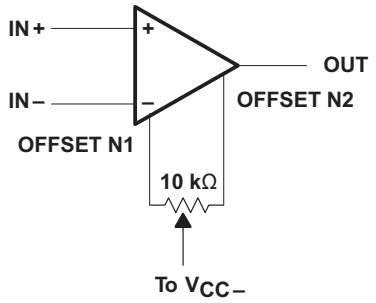


图 12. Input Offset Voltage Null Circuit

8.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal drives a relatively high current load. This circuit is also called a buffer amplifier or unity-gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so the resistance can provide as much current as necessary to the output load.

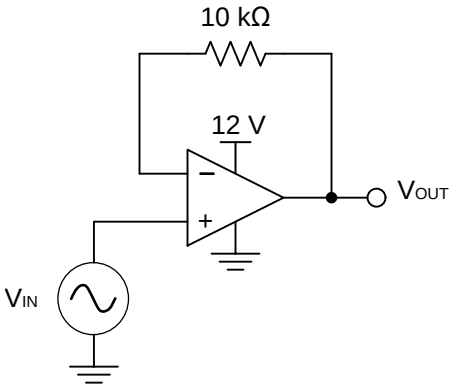


图 13. Voltage Follower Schematic

Typical Application (接下页)

8.2.1 Design Requirements

- Output range from 2 V to 11.5 V
- Input range from 2 V to 11.5 V
- Resistive feedback to negative input

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by the internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

8.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The selected amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11.5 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail rather than ground allows the amplifier to maintain linearity for inputs below 2 V.

8.2.3 Application Curves for Output Characteristics

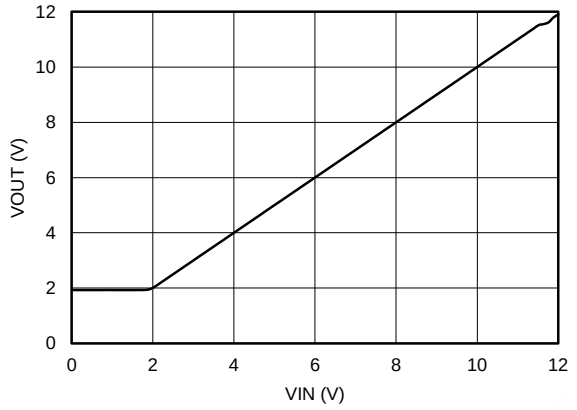


图 14. Output Voltage vs Input Voltage

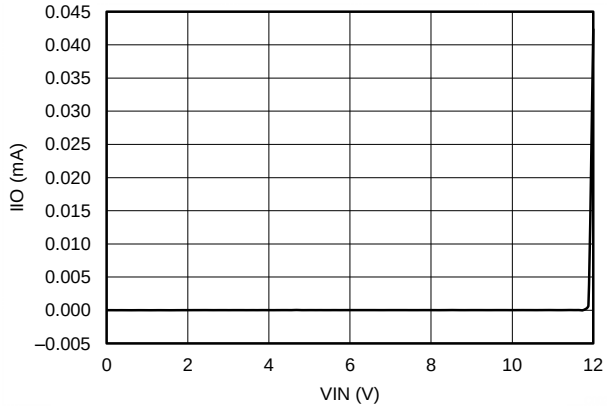


图 15. Current Drawn Input of Voltage Follower (I_{IO}) vs Input Voltage

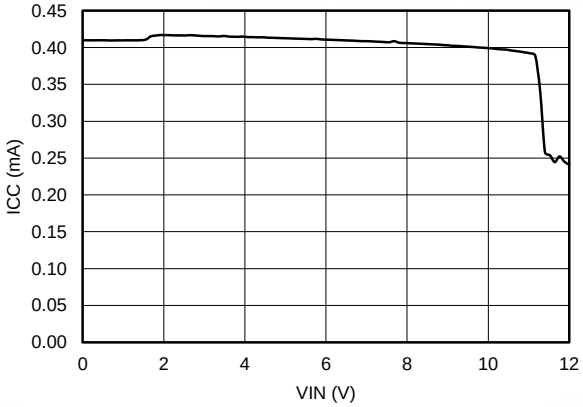


图 16. Current Drawn from Supply (I_{CC}) vs Input Voltage

9 Power Supply Recommendations

The μA741 device is specified for operation from ±5 to ±15 V; many specifications apply from 0°C to 70°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

CAUTION

Supply voltages larger than ±18 V can permanently damage the device (see *Absolute Maximum Ratings*).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

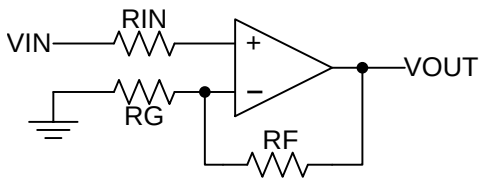


图 17. Operational Amplifier Schematic for Noninverting Configuration

Layout Example (接下页)

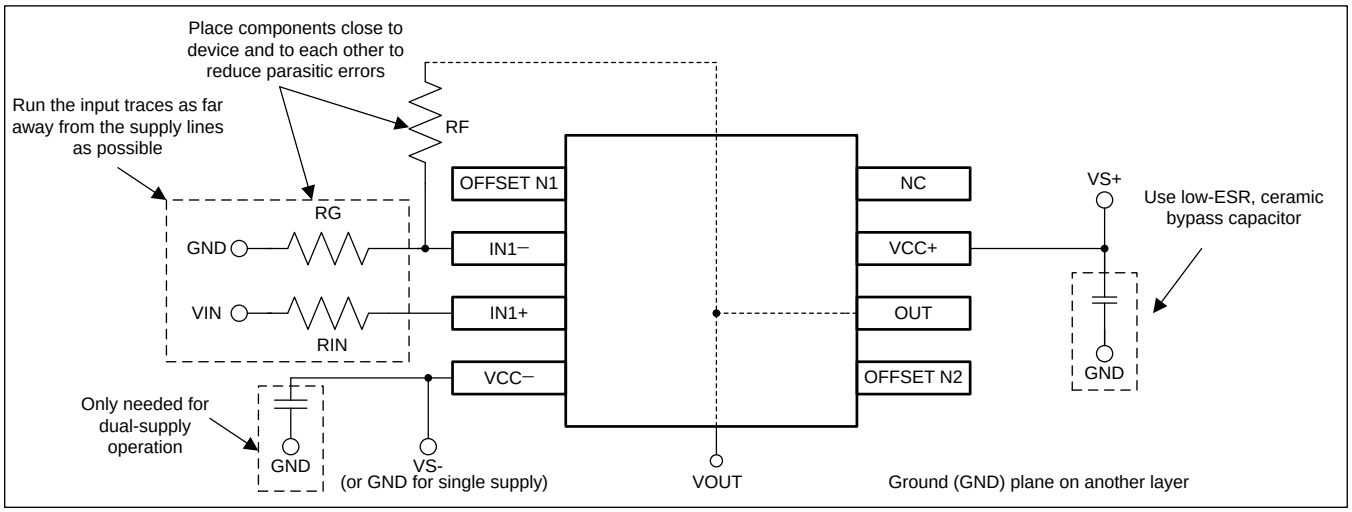


图 18. Operational Amplifier Board Layout for Noninverting Configuration

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 商标

All trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA741CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UA741CP	Samples
UA741CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UA741CP	Samples
UA741CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	U741	Samples
UA741CPSRE4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	U741	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

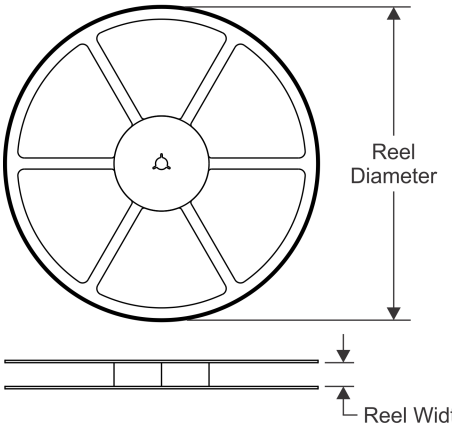
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

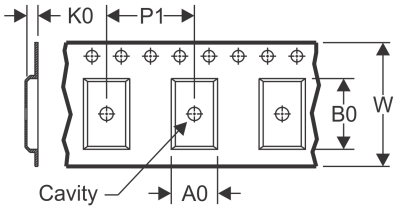
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

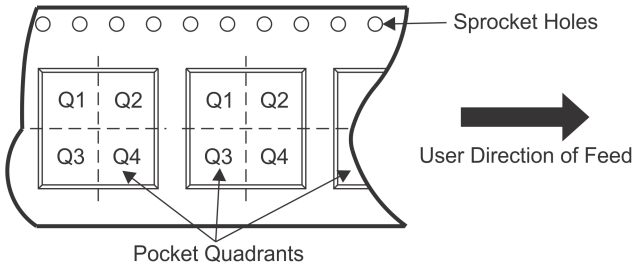


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

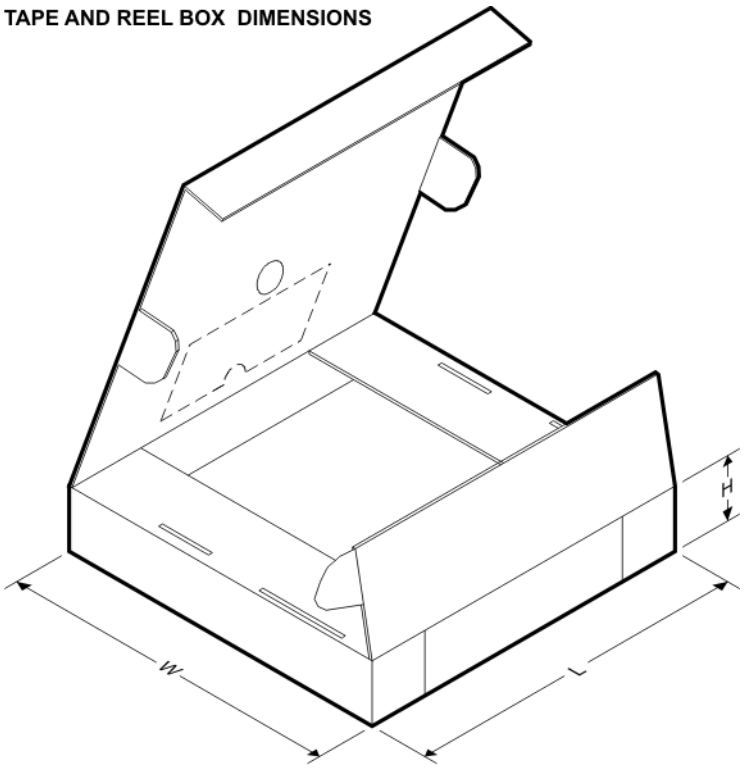
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

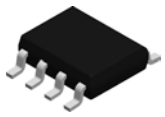
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA741CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA741CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA741CDR	SOIC	D	8	2500	340.5	338.1	20.6
UA741CPSR	SO	PS	8	2000	853.0	449.0	35.0

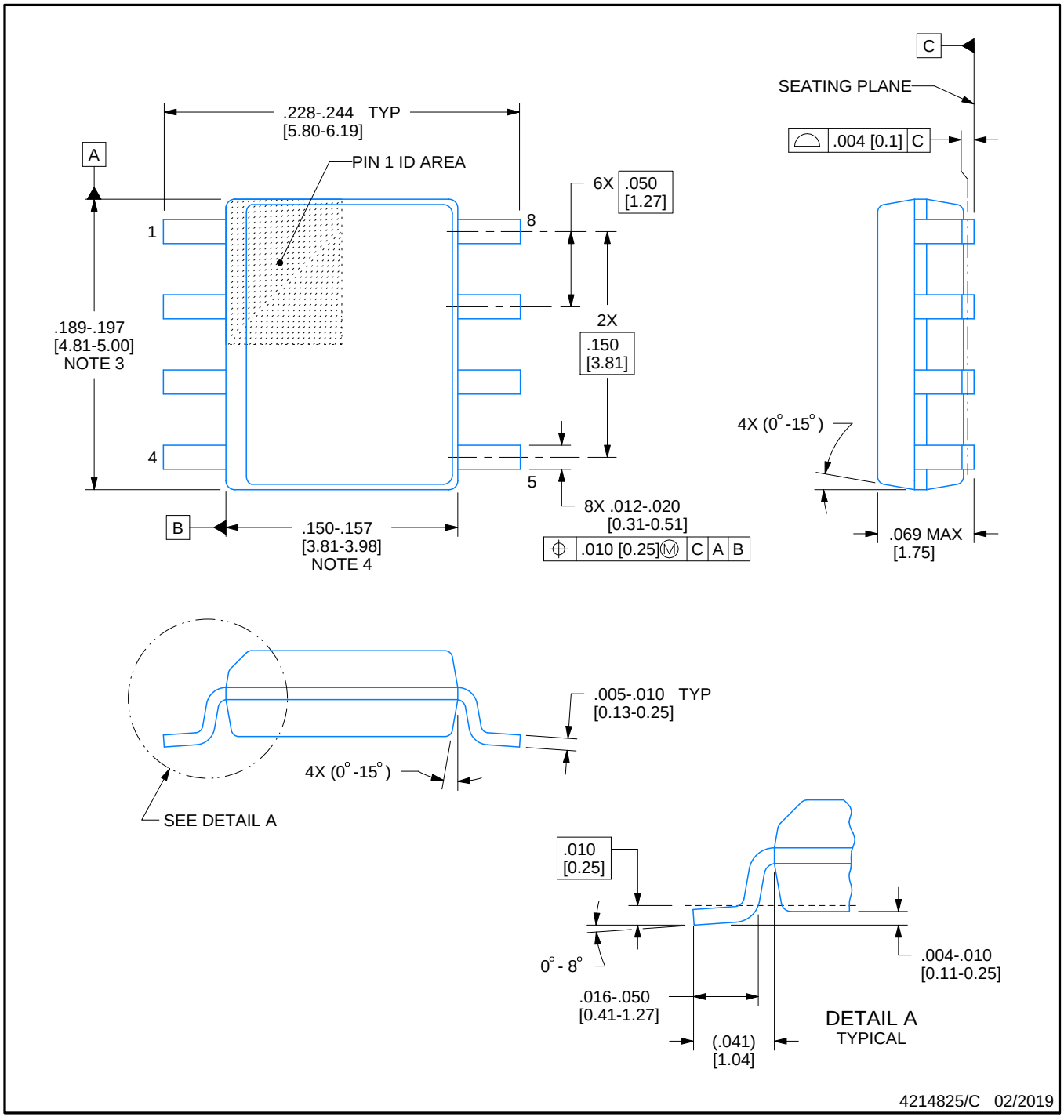


PACKAGE OUTLINE

D0008A

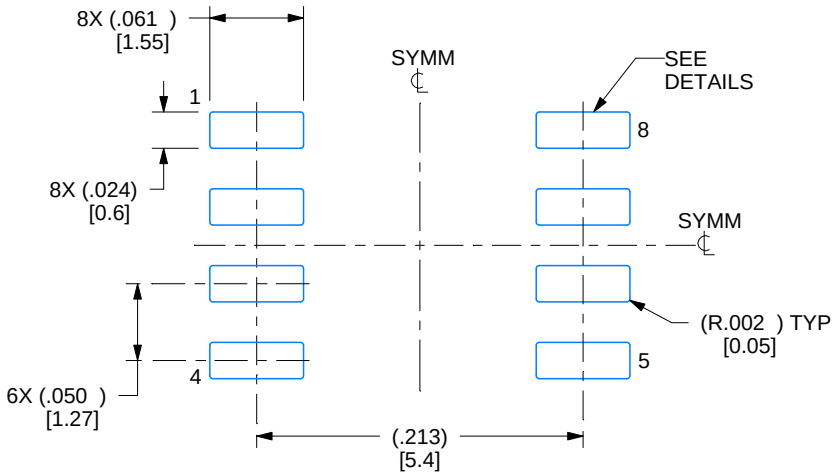
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

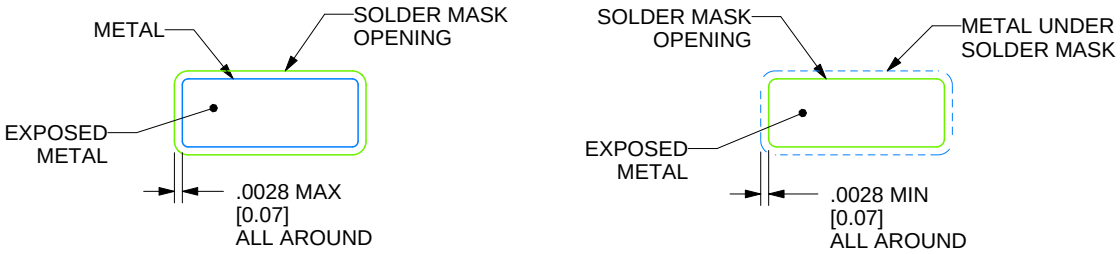


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

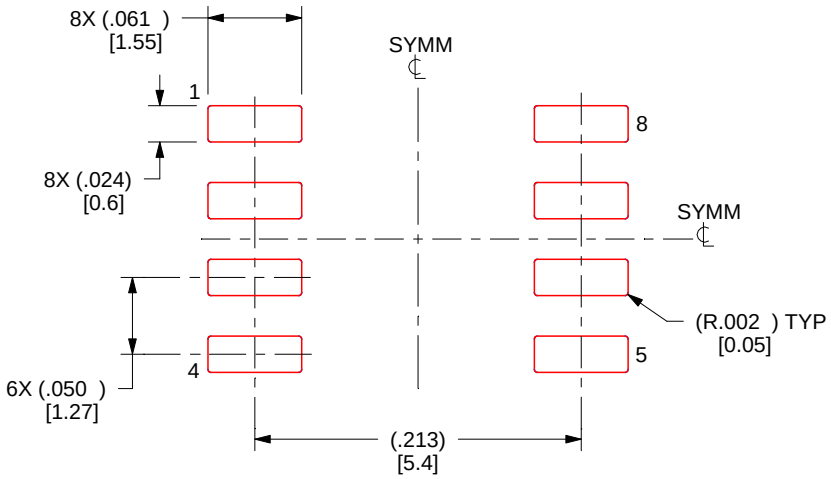
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

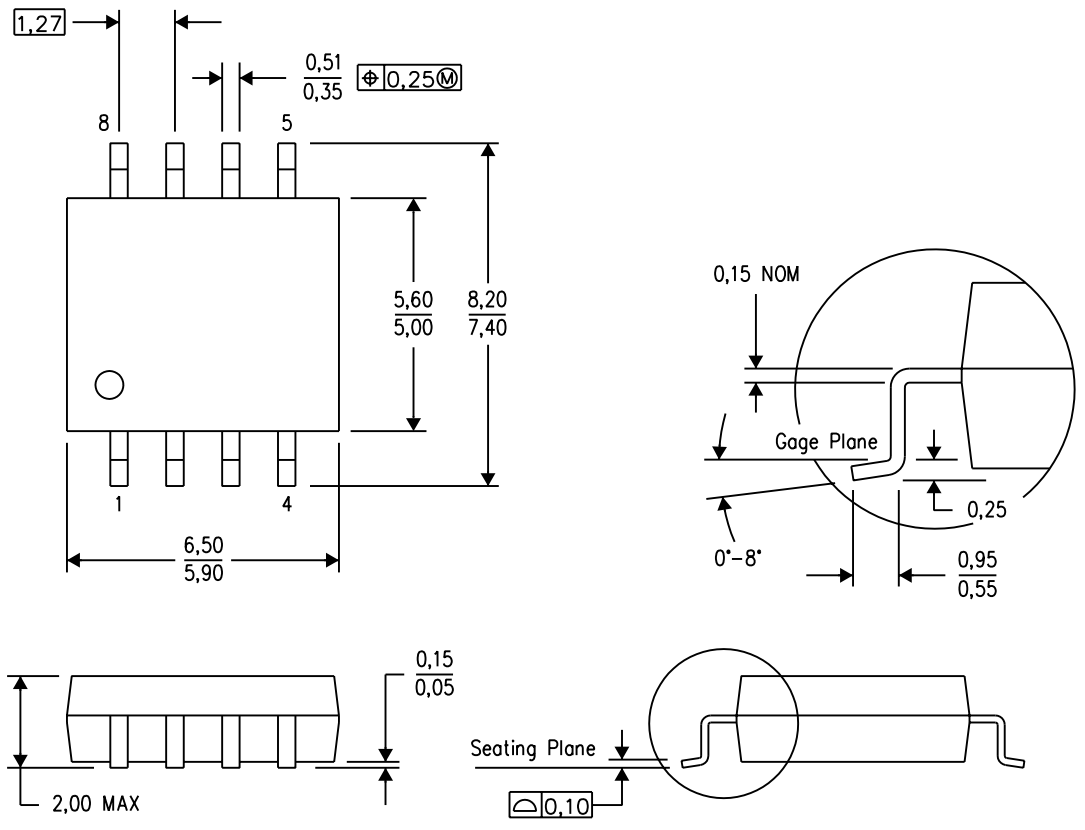
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

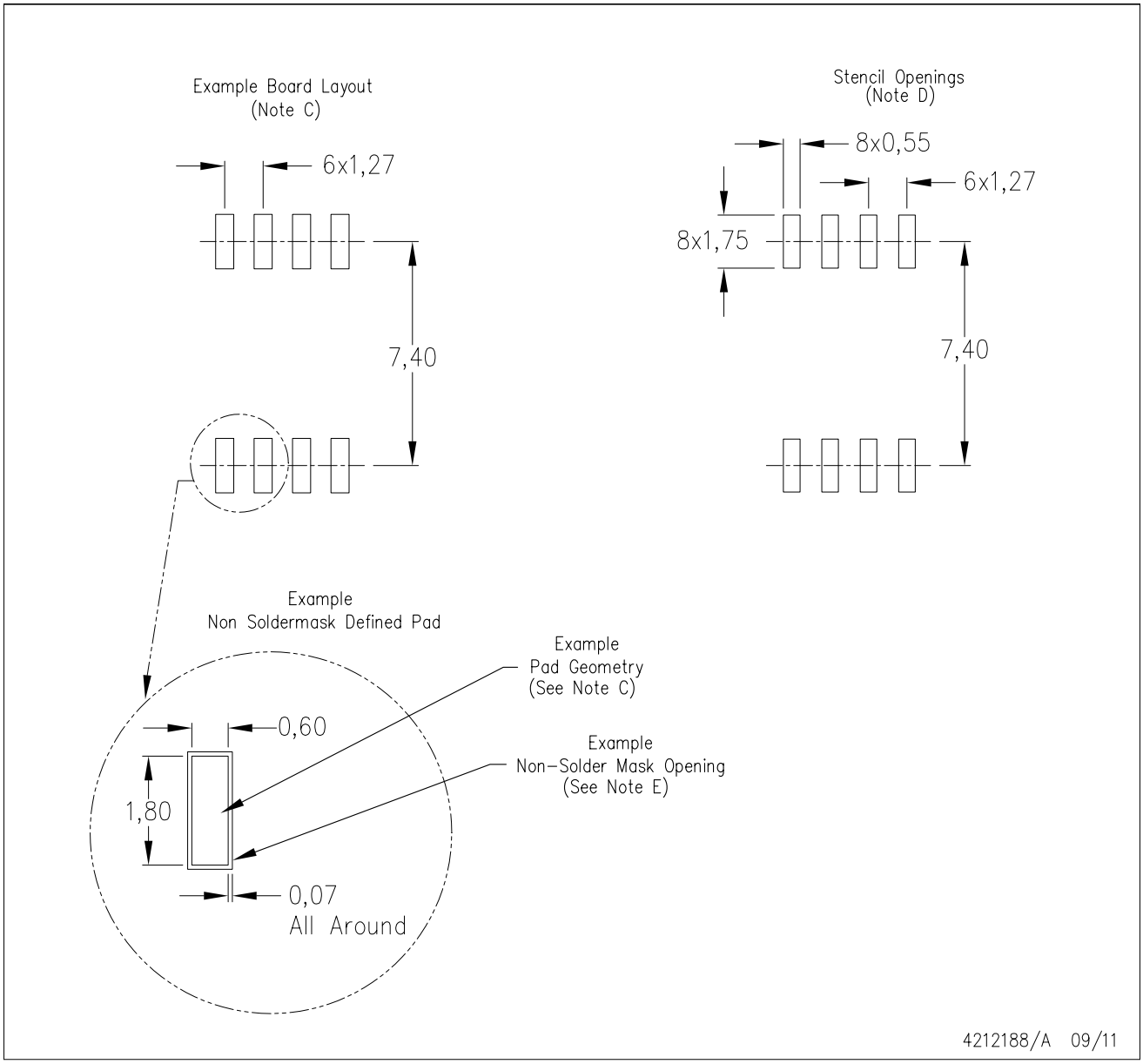
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

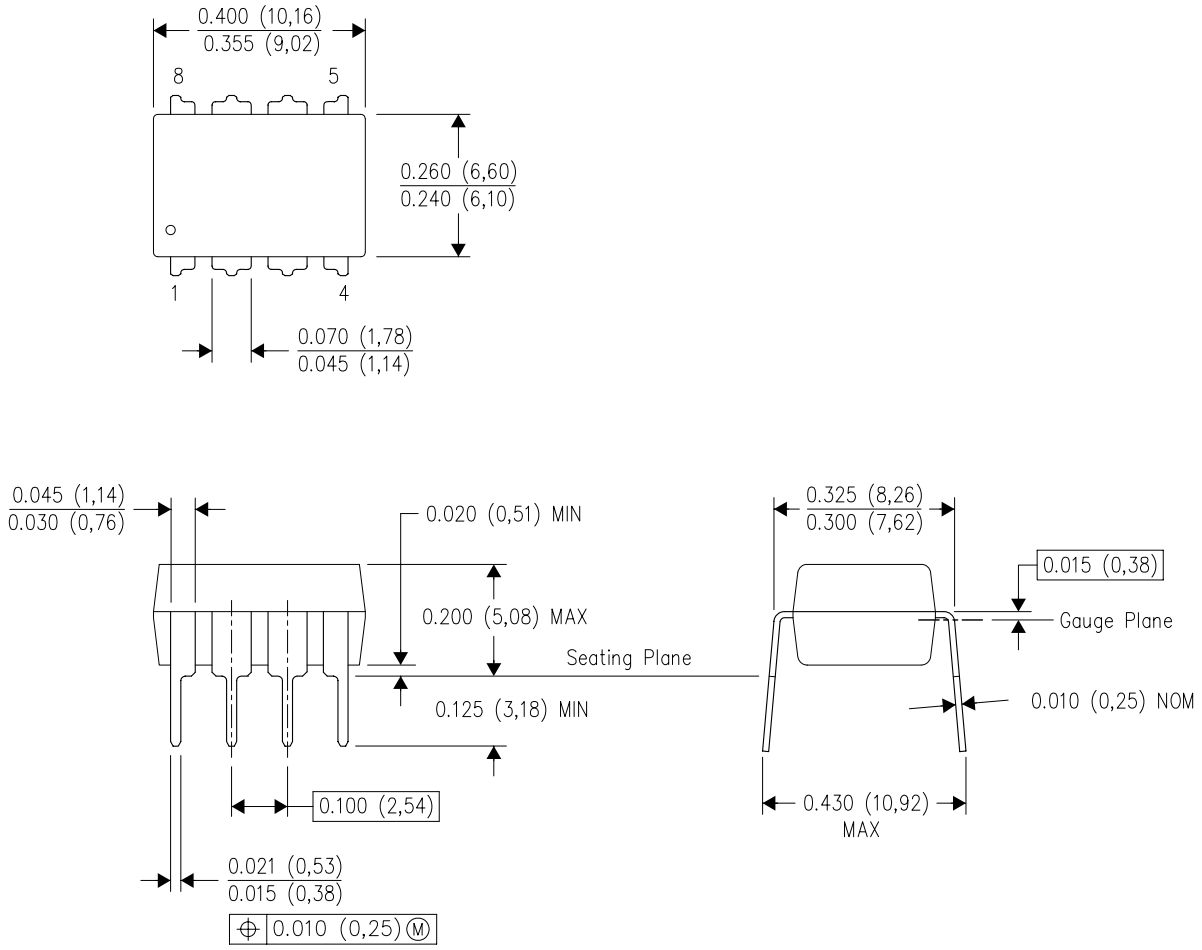
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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