AMC1200/B 全差分隔离放大器

1 特性

- 针对分流电阻进行优化的 ±250mV 输入电压范围
- 极低非线性度：5V 时最大值为 0.075%
- 低偏移误差：最大值为 1.5mV
- 低噪声：3.1mV_{RMS}（典型值）
- 低高侧电源电流：
  5V 时最大值为 8mA
- 输入带宽：最小值为 60kHz
- 固定增益：8（精度为 0.5%）
- 高共模抑制比：108dB
- 3.3V 低侧工作电压
- 经认证的电流隔离：
  - 已通过 UL1577 和 VDE V 0884-10 批准
  - 隔离电压：4250 V_{PEAK} (AMC1200B)
  - 工作电压：1200 V_{PEAK}
  - 瞬态抗扰度：10kV/μs（最小值）
- 在额定工作电压下使用寿命通常为 10 年（请参阅应用报告）
- 可在扩展工业温度范围内运行

2 应用

- 在下列应用中基于分流电阻器的电流感测：
  - 电机控制
  - 绿色环保能源
  - 变频器
  - 不间断电源

3 说明

AMC1200 和 AMC1200B 是高精度隔离放大器，通过磁场抗扰度较高的二氧化硅 (SiO_2) 隔离层隔离输出和输入电路。该隔离层经 UL1577 与 VDE V 0884-10 标准认证，可提供高达 4250 V_{PEAK} (AMC1200B) 或 4000 V_{PEAK} (AMC1200) 的电流隔离。通过与隔离电源配合使用，这些器件可防止共模高电压线路上的噪声电流进入本地接地并干扰或损害敏感电路。

AMC1200 或 AMC1200B 的输入针对直接连接至分流电阻器或其它低电压电平信号源进行了优化。该器件性能优异，支持精确电流控制，从而降低系统级功耗（尤其在电机控制应用中）并减少扭矩纹波。可自动将输出信号的共模电压调节为 3V 或 5V 低侧电源电压。

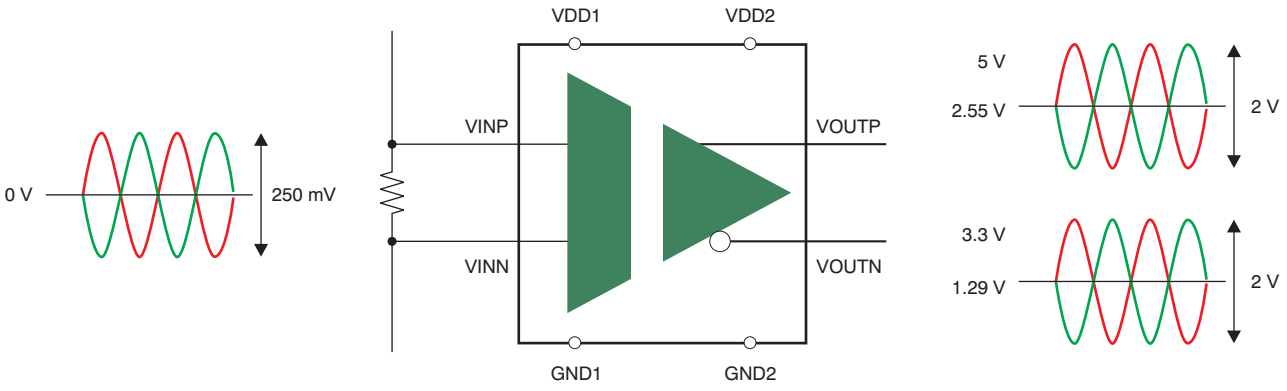
AMC1200 和 AMC1200B 在扩展工业温度范围内（–40°C 到 105°C）完全额定运行，采用宽体 8 引脚小外形尺寸集成电路 (SOIC) (DWV) 封装以及 gullwing 8 (DUB) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC1200 和 AMC1200B	SOP (8)	9.50mm × 6.57mm
	SOIC (8)	5.85mm × 7.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (September 2013) to Revision D — **Page**

- 已添加 *ESD 额定值*表，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision B (August 2012) to Revision C — **Page**

- 已删除 器件图 ... 1
- 已添加 DWV (SOIC-9) 封装至文档 ... 1
- 已更改 *部分的*最后一段 ... 1
- Added DWV pin out drawing ... 3
- Added DWV column to Thermal Information table ... 4
- Added row for DWV package to *L(I01)* and *L(I02)* parameters in Package Characteristics table ... 12

Changes from Revision A (August 2011) to Revision B — **Page**

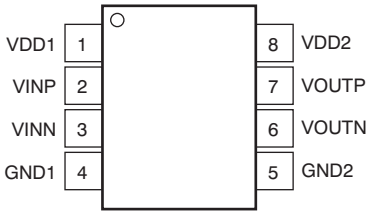
- 已更改隔离电压特性着重号 ... 1
- 已添加 AMC1200B 器件至数据表 ... 1
- Changed title for Figure 25 ... 10
- Changed CTI parameter minimum value in Electrical Characteristics from ≥ 175 to ≥ 400 ... 12

Changes from Original (April 2011) to Revision A — **Page**

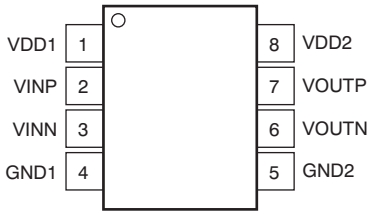
- Changed sign for maximum junction temperature from minus to plus (typo) ... 4
- Added "0.5-V step" to test condition for Rise/fall time parameter ... 5
- Changed Figure 12 ... 6
- Changed Figure 13 ... 7
- Changed surge immunity parameter from ±4000 to ±6000 ... 12

5 Pin Configuration and Functions

DUB Package
8-Pin SOP
Top View



DWV Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VDD1	Power	High-side power supply
2	VINP	Analog input	Noninverting analog input
3	VINN	Analog input	Inverting analog input
4	GND1	Power	High-side analog ground
5	GND2	Power	Low-side analog ground
6	VOUTN	Analog output	Inverting analog output
7	VOUTP	Analog output	Noninverting analog output
8	VDD2	Power	Low-side power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over the operating ambient temperature range, unless otherwise noted.(1)

	MIN	MAX	UNIT
Supply voltage, VDD1 to GND1 or VDD2 to GND2	–0.5	6	V
Analog input voltage at VINP, VINN	GND1 – 0.5	VDD1 + 0.5	V
Input current to any pin except supply pins	–10	10	mA
Maximum junction temperature, T_J Max		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM) JEDEC standard 22, test method A114-C.01(1)	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature range	–40		105	°C
VDD1	High-side power supply	4.5	5	5.5	V
VDD2	Low-side power supply	2.7	5	5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		AMC1200, AMC1200B		UNIT
		DUB (SOP)	DWV (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.1	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	49.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	56.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.2	16	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.4	55.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All minimum/maximum specifications at T_A = –40°C to 105°C and within the specified voltage range, unless otherwise noted. Typical values are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Maximum input voltage before clipping	VINP – VINN		±320		mV
	Differential input voltage	VINP – VINN	–250		250	mV
V_{CM}	Common mode operating range		–0.16		VDD1	V
V_{OS}	Input offset voltage		–1.5	±0.2	1.5	mV
TCV_{OS}	Input offset thermal drift		–10	±1.5	10	µV/K
CMRR	Common mode rejection ratio	V_{IN} from 0 V to 5 V at 0 Hz		108		dB
		V_{IN} from 0 V to 5 V at 50 kHz		95		dB
C_{IN}	Input capacitance to GND1	VINP or VINN		3		pF
C_{IND}	Differential input capacitance			3.6		pF
R_{IN}	Differential input resistance			28		kΩ
	Small-signal bandwidth		60	100		kHz
OUTPUT						
	Nominal gain			8		
G_{ERR}	Gain error	Initial, at T_A = 25°C	–0.5%	±0.05%	0.5%	
			–1%	±0.05%	1%	
TCG_{ERR}	Gain error thermal drift			±56		ppm/K
	Nonlinearity	4.5 V ≤ VDD2 ≤ 5.5 V	–0.075%	±0.015%	0.075%	
		2.7 V ≤ VDD2 ≤ 3.6 V	–0.1%	±0.023%	0.1%	
	Nonlinearity thermal drift			2.4		ppm/K
	Output noise	VINP = VINN = 0 V		3.1		mV_{RMS}
PSRR	Power-supply rejection ratio	vs VDD1, 10-kHz ripple		80		dB
		vs VDD2, 10-kHz ripple		61		dB
	Rise/fall time	0.5-V step, 10% to 90%		3.66	6.6	µs
	V_{IN} to V_{OUT} signal delay	0.5-V step, 50% to 10%, unfiltered output		1.6	3.3	µs
		0.5-V step, 50% to 50%, unfiltered output		3.15	5.6	µs
		0.5-V step, 50% to 90%, unfiltered output		5.26	9.9	µs
CMTI	Common mode transient immunity	V_{CM} = 1 kV	10	15		kV/µs
	Output common mode voltage	2.7 V ≤ VDD2 ≤ 3.6 V	1.15	1.29	1.45	V
		4.5 V ≤ VDD2 ≤ 5.5 V	2.4	2.55	2.7	V
	Short circuit current			20		mA
R_{OUT}	Output resistance			2.5		Ω
POWER SUPPLY						
VDD1	High-side supply voltage		4.5	5	5.5	V
VDD2	Low-side supply voltage		2.7	5	5.5	V
I_{DD1}	High-side supply current			5.4	8	mA
I_{DD2}	Low-side supply current	2.7 V < VDD2 < 3.6 V		3.8	6	mA
		4.5 V < VDD2 < 5.5 V		4.4	7	mA
P_{DD1}	High-side power dissipation			27	44	mW
P_{DD2}	Low-side power dissipation	2.7 V < VDD2 < 3.6 V		11.4	21.6	mW
		4.5 V < VDD2 < 5.5 V		22	38.5	mW

6.6 Typical Characteristics

At VDD1 = VDD2 = 5 V, VINP = –250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

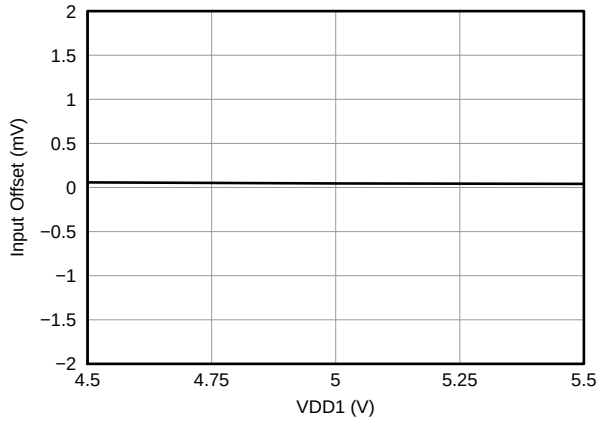


Figure 1. Input Offset vs High-Side Supply Voltage

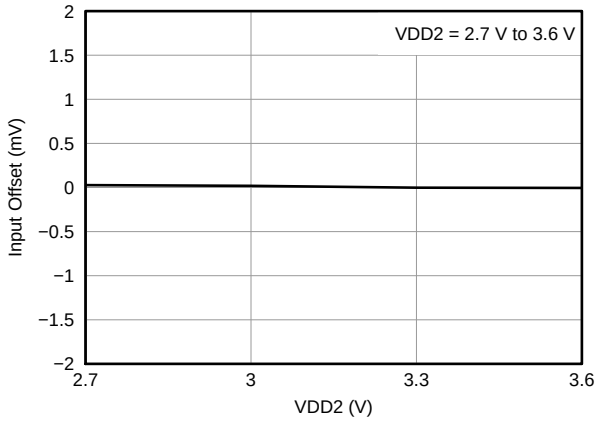


Figure 2. Input Offset vs Low-Side Supply Voltage

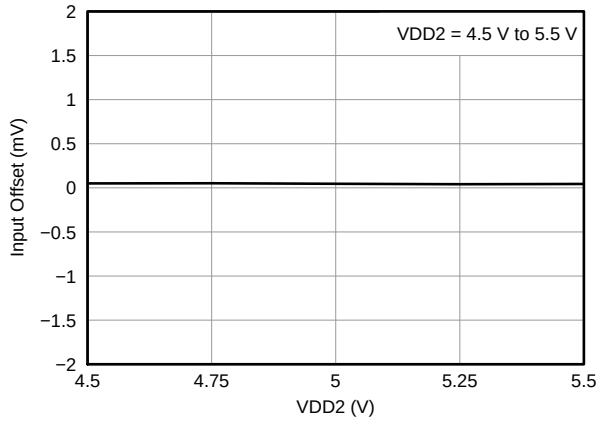


Figure 3. Input Offset vs Low-Side Supply Voltage

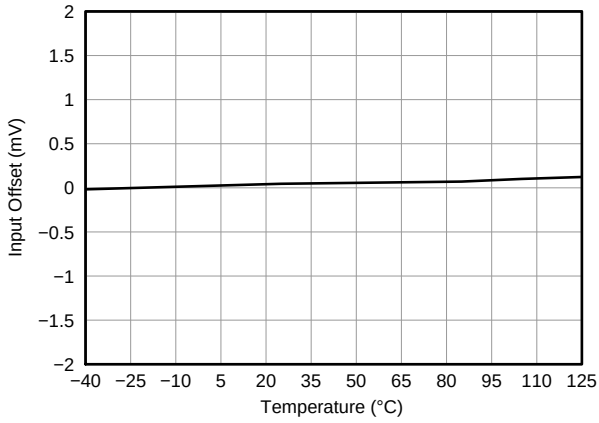


Figure 4. Input Offset vs Temperature

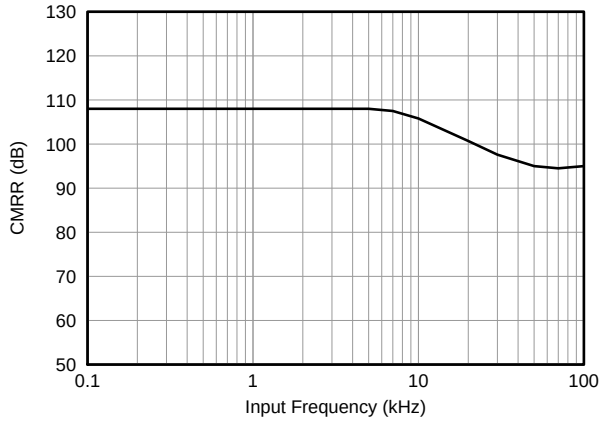


Figure 5. Common Mode Rejection Ratio vs Input Frequency

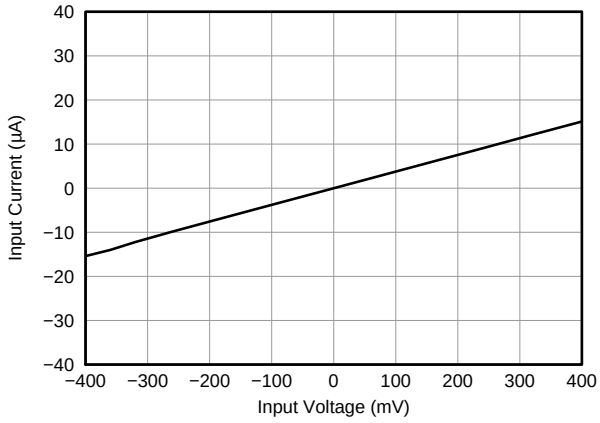


Figure 6. Input Current vs Input Voltage

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

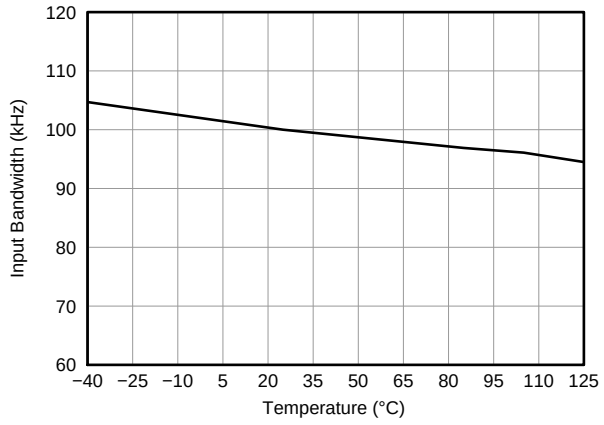


Figure 7. Input Bandwidth vs Temperature

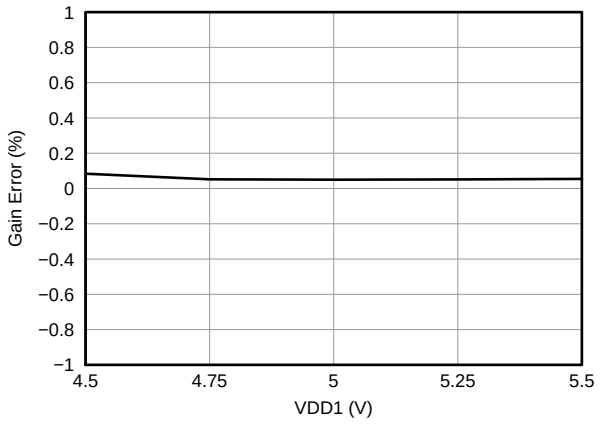


Figure 8. Gain Error vs High-Side Supply Voltage

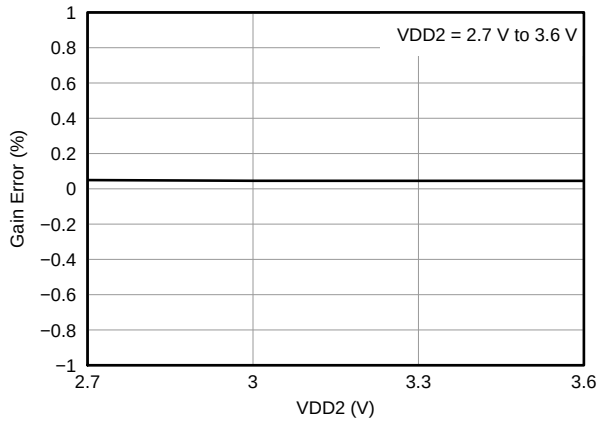


Figure 9. Gain Error vs Low-Side Supply Voltage

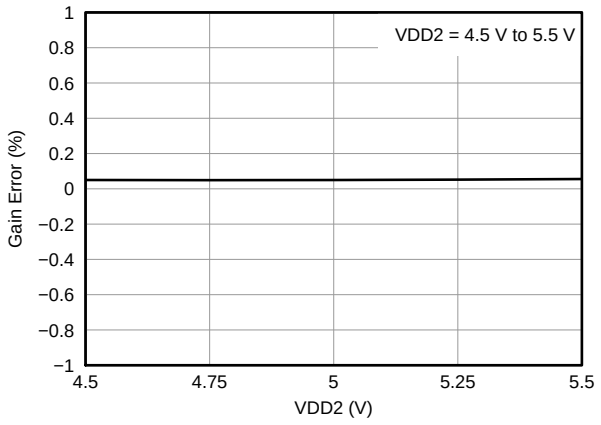


Figure 10. Gain Error vs Low-Side Supply Voltage

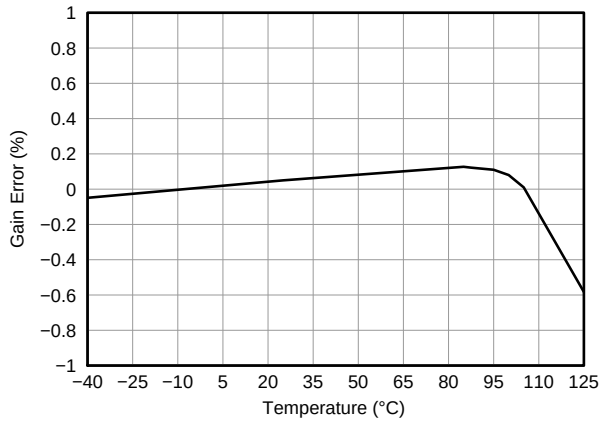


Figure 11. Gain Error vs Temperature

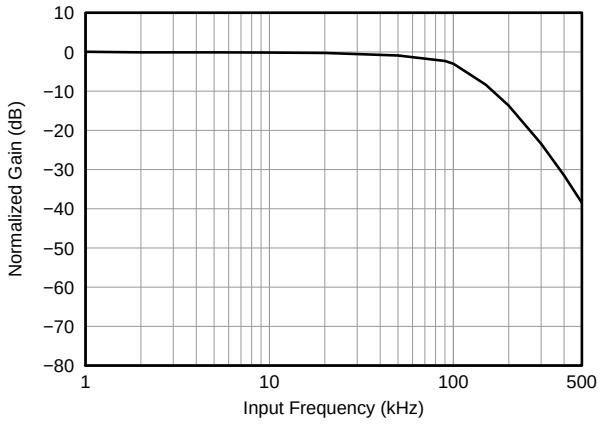


Figure 12. Normalized Gain vs Input Frequency

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

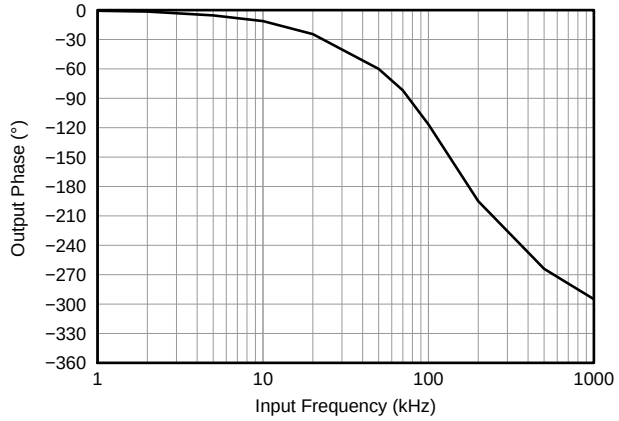


Figure 13. Output Phase vs Input Frequency

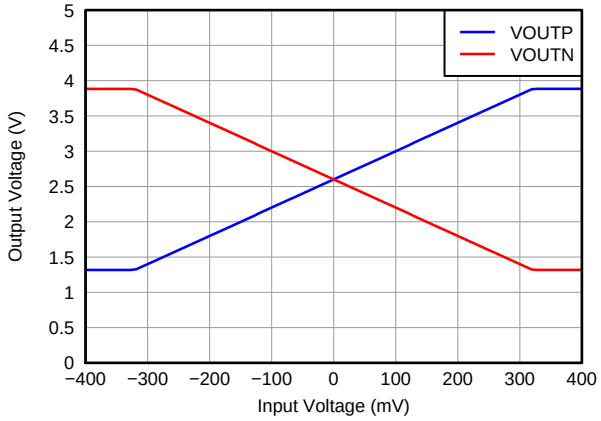


Figure 14. Output Voltage vs Input Voltage

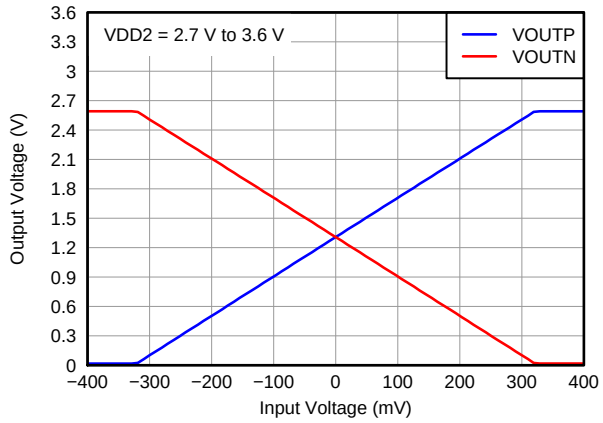


Figure 15. Output Voltage vs Input Voltage

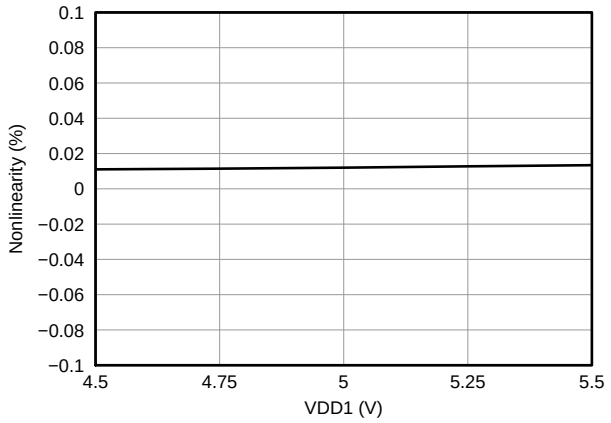


Figure 16. Nonlinearity vs High-Side Supply Voltage

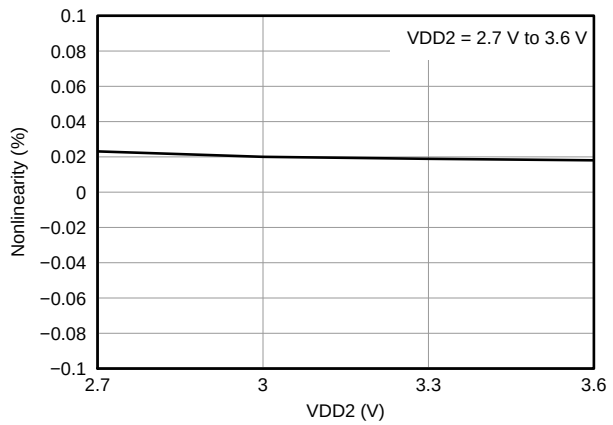


Figure 17. Nonlinearity vs Low-Side Supply Voltage

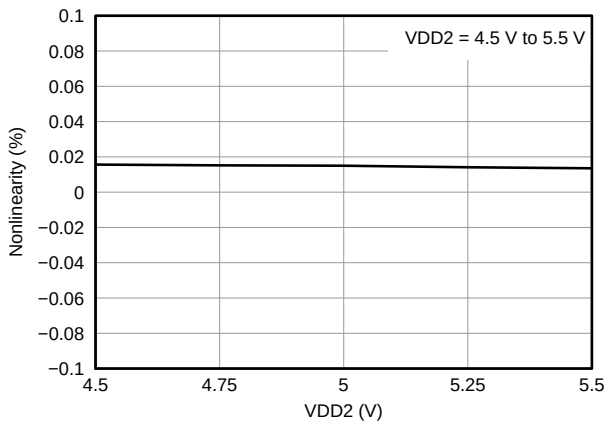


Figure 18. Nonlinearity vs Low-Side Supply Voltage

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

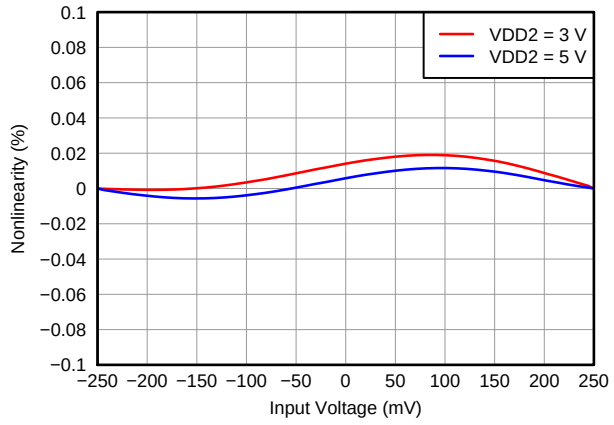


Figure 19. Nonlinearity vs Input Voltage

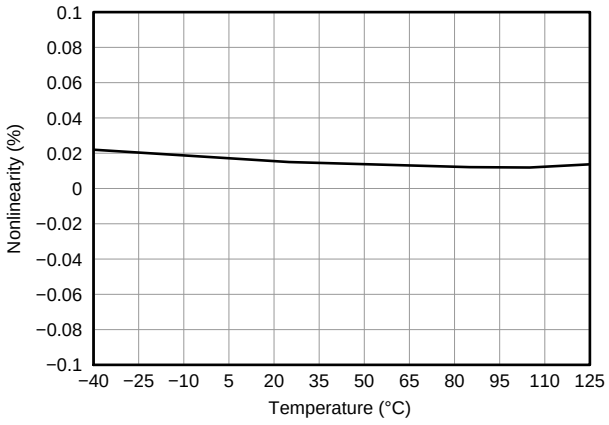


Figure 20. Nonlinearity vs Temperature

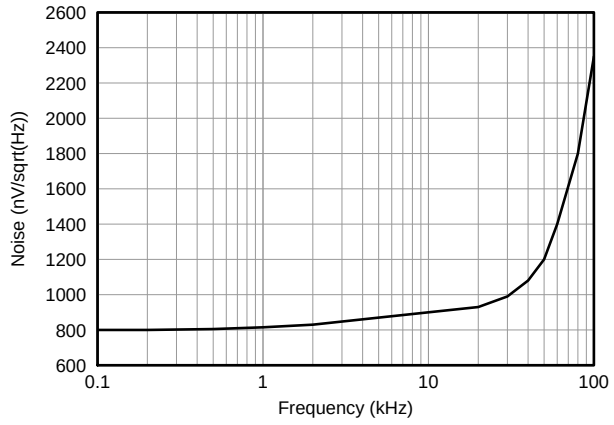


Figure 21. Output Noise Density vs Frequency

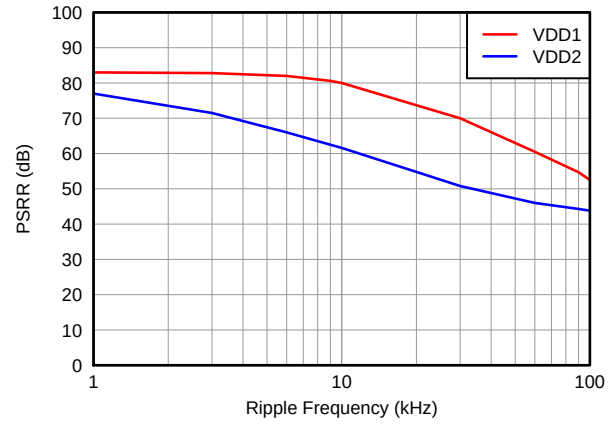


Figure 22. Power-Supply Rejection Ratio vs Ripple Frequency

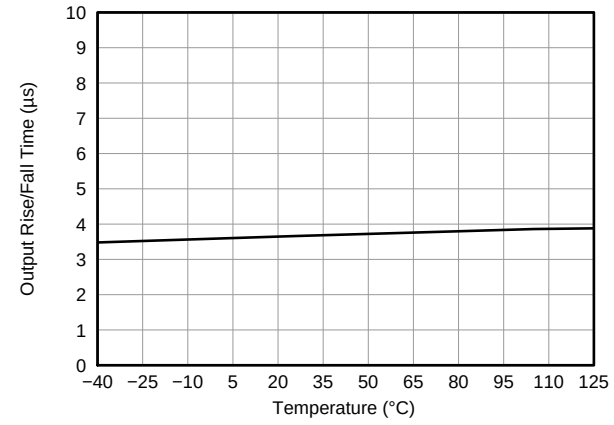


Figure 23. Output Rise and Fall Time vs Temperature

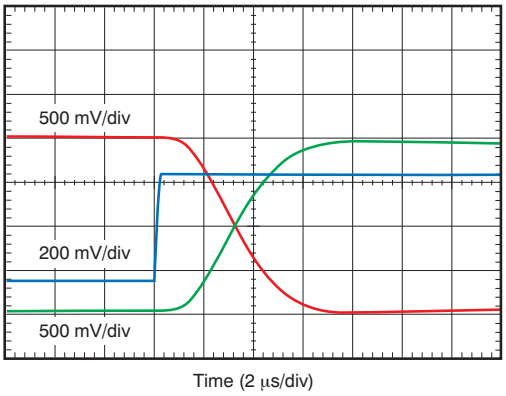


Figure 24. Full-Scale Step Response

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

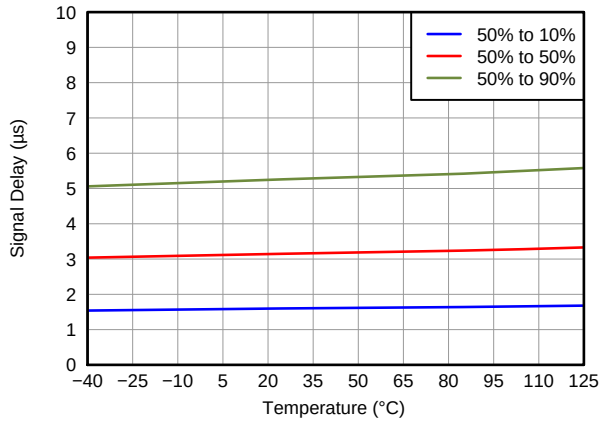


Figure 25. Output Signal Delay Time vs Temperature

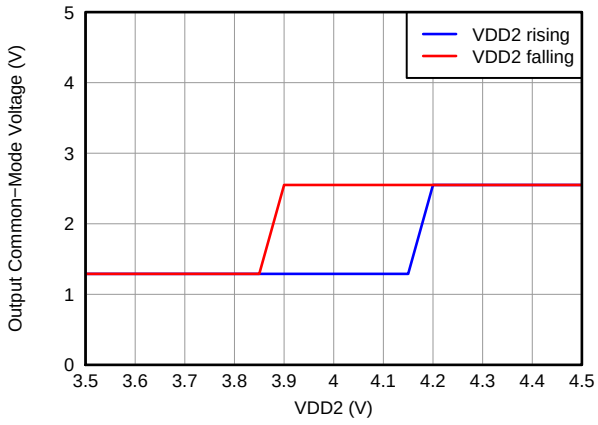


Figure 26. Output Common Mode Voltage vs Low-Side Supply Voltage

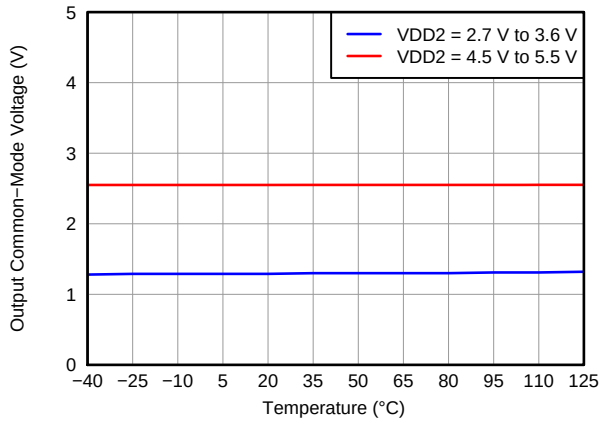


Figure 27. Output Common Mode Voltage vs Temperature

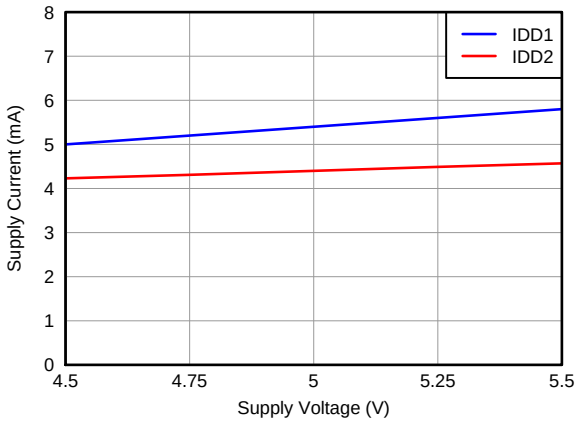


Figure 28. Supply Current vs Supply Voltage

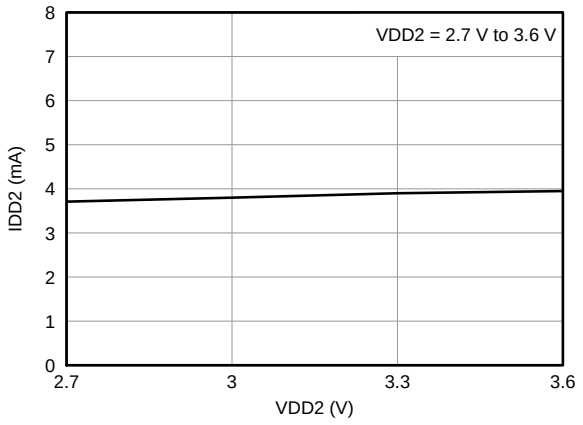


Figure 29. Low-Side Supply Current vs Low-Side Supply Voltage

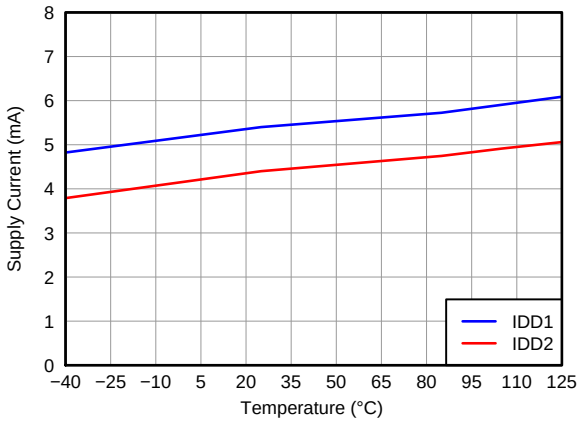


Figure 30. Supply Current vs Temperature

7 Detailed Description

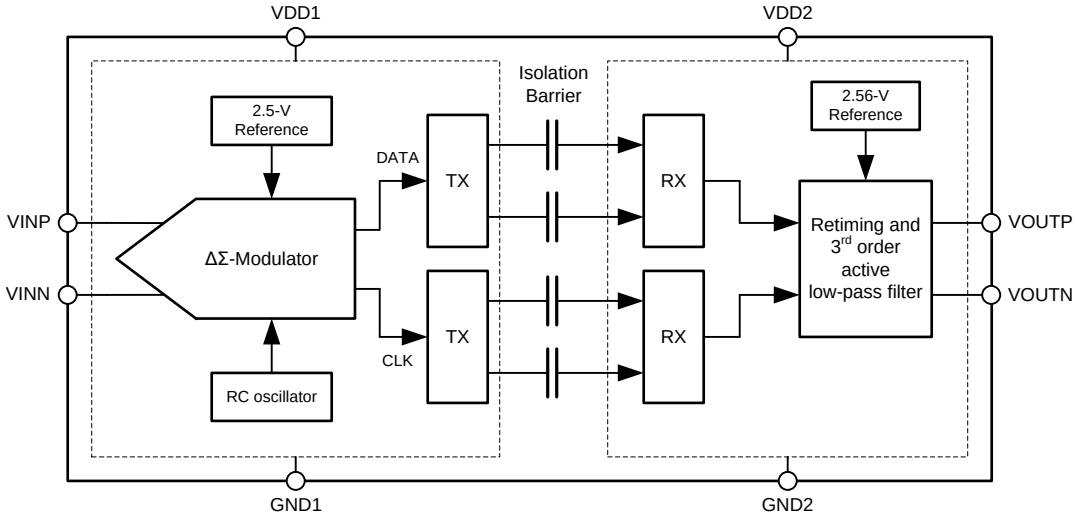
7.1 Overview

The AMC1200 is a fully-differential precision isolation amplifier. The analog input signal is converted to a digital signal and then transferred across a capacitive isolation barrier. The digital modulation used in the AMC1200 together with the isolation barrier characteristics result in excellent reliability and transient immunity.

After processing the digital signal with a low-pass filter, an analog signal is provided at the outputs. The main building blocks are shown in the *Functional Block Diagram* section.

The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity, as described in application report, *ISO72x Digital Isolator Magnetic-Field Immunity* (SLLA181), available for download at www.ti.com.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Insulation Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IORM}	Maximum working insulation voltage					1200	V_{PEAK}
V_{PR}	Input to output test voltage	Qualification test: after Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, partial discharge < 5 pC				1140	V_{PEAK}
		Qualification test: method a, after environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, partial discharge < 5 pC				1920	V_{PEAK}
		100% production test: method b1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s, partial discharge < 5 pC				2250	V_{PEAK}
V_{IOTM}	Transient overvoltage	Qualification test: t = 60 s	AMC1200			4000	V_{PEAK}
			AMC1200B			4250	V_{PEAK}
V_{ISO}	Insulation voltage per UL	Qualification test: $V_{TEST} = V_{ISO}$, t = 60 s	AMC1200			4000	V_{PEAK}
			AMC1200B			4250	V_{PEAK}
		100% production test: V_{TEST} = 1.2 x V_{ISO}, t = 1 s	AMC1200			4800	V_{PEAK}
			AMC1200B			5100	V_{PEAK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S			> 10^9		Ω

Feature Description (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PD	Pollution degree			2		°

7.3.2 IEC 61000-4-5 Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IOSM}	Surge immunity	1.2-µs/50-µs voltage surge and 8-µs/20-µs current surge	±6000	V

7.3.3 IEC 60664-1 Ratings(1)

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-IV
	Rated mains voltage ≤ 400 V_{RMS}	I-III
	Rated mains voltage < 600 V_{RMS}	I-III

(1) Over operating free-air temperature range (unless otherwise noted).

7.3.4 Package Characteristics(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal to terminal distance through air	DWV package	8			mm
			DUB package	7			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal to terminal distance across the package surface	DWV package	8			mm
			DUB package	7			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 part 1		≥ 400			V
	Minimum internal gap (internal clearance)	Distance through the insulation		0.014			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together to create a two-terminal device, T_A < 85°C			> 10^{12}		Ω
		Input to output, V_{IO} = 500 V, 85°C ≤ T_A < T_A max			> 10^{11}		Ω
C_{IO}	Barrier capacitance input to output	V_I = 0.5 V_{PP} at 1 MHz			1.2		pF
C_I	Input capacitance to ground	V_I = 0.5 V_{PP} at 1 MHz			3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of a specific application. Take care to maintain the creepage and clearance distance of the board design to ensure that the mounting pads of the isolator on the printed-circuit-board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal according to the measurement techniques shown in the TI Isolation Glossary. Techniques such as inserting grooves and/or ribs on the PCB are used to help increase these specifications.

7.3.5 IEC Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 246°C/W, V_{IN} = 5.5 V, T_J = 150°C, T_A = 25°C			10	mA
T_C	Maximum case temperature				150	°C

The safety-limiting constraint is the operating virtual junction temperature range specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determine the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages* and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.3.6 Regulatory Information

VDE/IEC	UL
Certified according to VDE V 0884-10	Recognized under 1577 component recognition program
Certificate number: 40016131	File number: E181974

7.3.7 Isolation Amplifier

The AMC1200 device consists of a second order delta-sigma modulator input stage including an internal reference and clock generator. The output of the modulator and clock signal are differentially transmitted over the integrated capacitive isolation barrier that separates the high- and low-voltage domains. The received bitstream and clock signals are synchronized and processed by a third-order analog filter with a nominal gain of 8 on the low-side and presented as a differential output of the device, as shown in *Functional Block Diagram* section.

7.3.8 Analog Input

The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. However, there are two restrictions on the analog input signals, VINP and VINN. If the input voltage exceeds the range AGND – 0.5 V to AVDD + 0.5 V, the input current must be limited to 10 mA to prevent the implemented input protection diodes from damage. In addition, the linearity and the noise performance of the device are ensured only when the differential analog input voltage remains within ±250 mV.

The differential analog input of the AMC1200 and AMC1200B devices is a switched-capacitor circuit based on a second-order modulator stage that digitizes the input signal into a 1-bit output stream. These devices compare the differential input signal (V_{IN} = VINP – VINN) against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged with a typical frequency of 10 MHz. With the S1 switches closed, C_{IND} charges to the voltage difference across VINP and VINN. For the discharge phase, both S1 switches open first and then both S2 switches close. C_{IND} discharges to approximately AGND + 0.8 V during this phase. Figure 31 shows the simplified equivalent input circuitry.

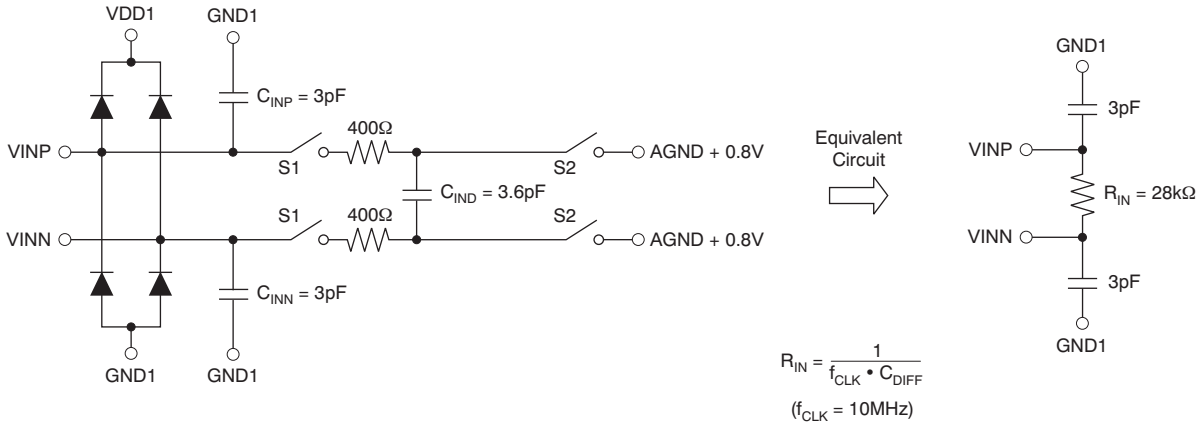


Figure 31. Equivalent Input Circuit

7.4 Device Functional Modes

The AMC1200 is operational when the power supplies VDD1 and VDD2 are applied as specified in the *Recommended Operating Conditions* section.

Device Functional Modes (continued)

The AMC1200 does not have any additional functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

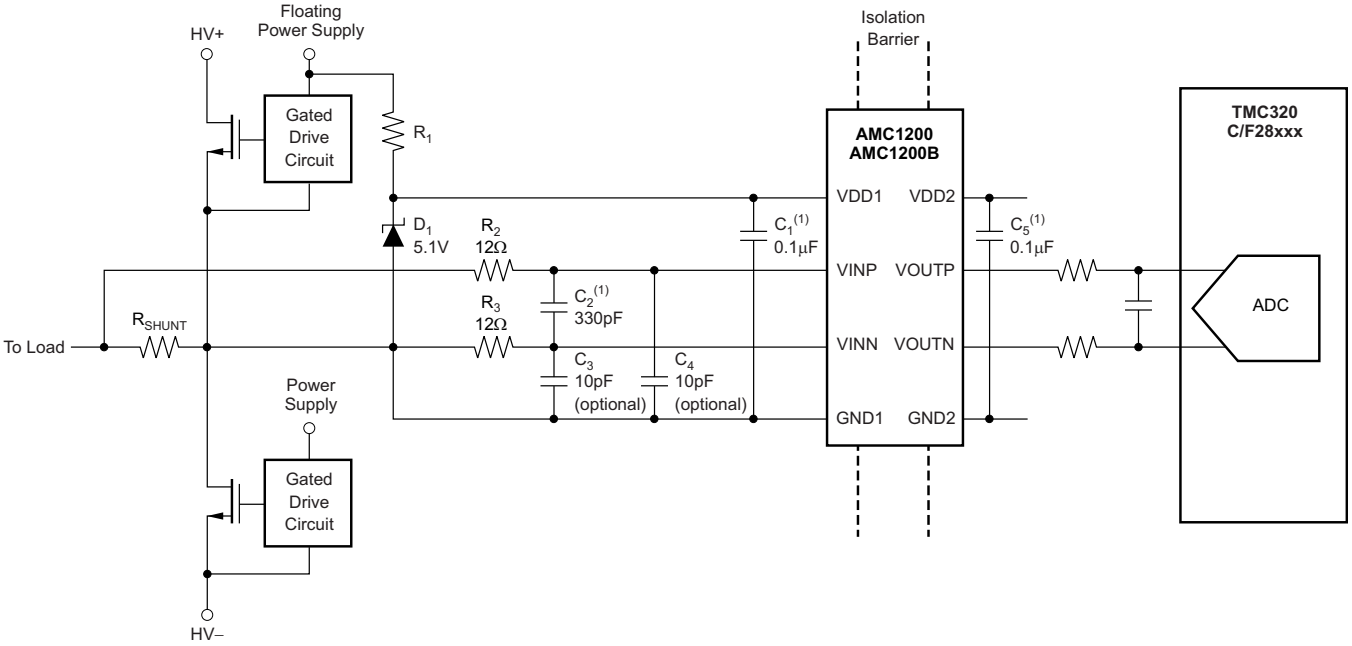
8.1 Application Information

The AMC1200 and AMC1200B devices offer unique linearity, high input common mode rejection, low DC errors and low temperature drift. These features make the AMC1200 a robust, high-performance isolation amplifier for industrial applications where high voltage isolation is required.

8.2 Typical Applications

8.2.1 Motor Control

Figure 32 shows a typical operation of the AMC1200 and AMC1200B devices in a motor-control application. Measurement of the motor phase current is done through the shunt resistor, R_{SHUNT} (in this case, a two-terminal shunt).



(1) Place these capacitors as close as possible to the AMC device.

Figure 32. Typical Application Diagram

The high-side power supply (VDD1) for the AMC1200 and AMC1200B are derived from the power supply of the upper gate driver. Further details are provided in the *Power Supply Recommendations* section.

The high transient immunity of the AMC1200 and AMC1200B ensures reliable and accurate operation even in high-noise environments such as the power stages of the motor drives.

As shown in Figure 37, TI recommends placing the bypass and filter capacitors as close as possible to the AMC device to ensure best performance.

Typical Applications (continued)

8.2.1.1 Design Requirements

For better performance, the differential input signal is filtered using RC filters (components R_2, R_3, and C_2). Optionally, C_3 and C_4 can be used to reduce charge dumping from the inputs. In this case, take care when choosing the quality of these capacitors; mismatch in values of these capacitors leads to a common mode error at the modulator input. If implemented, TI recommends using NP0 capacitors for C_2, C_3 and C_4.

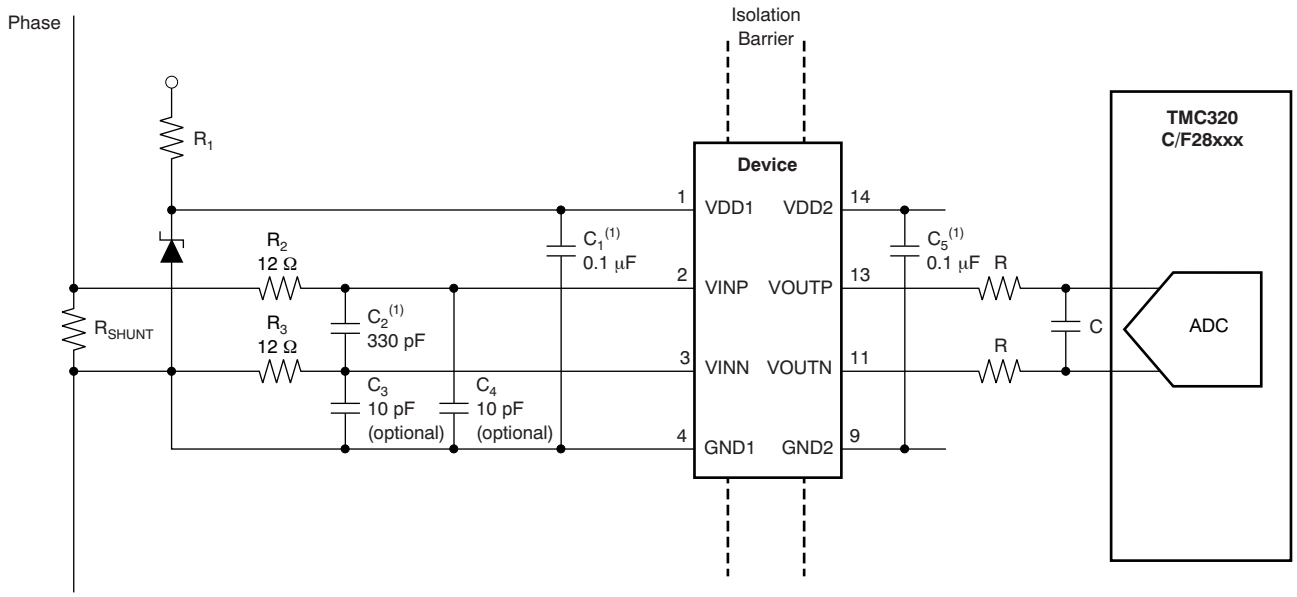


Figure 33. Shunt-Based Current Sensing with the AMC1200

Similar to the current measurements, isolated voltage measurements can be performed as described in the .

8.2.1.2 Detailed Design Procedure

The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input of the AMC1200 (VINN). If a four-terminal shunt is used, the inputs of the AMC1200 are connected to the inner leads and GND1 is connected to one of the outer shunt leads. The differential input of the AMC1200 ensures accurate operation even in noisy environments.

TI recommends limiting the value of resistors R_2 and R_3 to less than 24 Ω to avoid the incomplete settling of the AMC1200 input circuitry. The section provides more details on the AMC1200 input circuitry.

The differential output of the AMC1200 can either directly drive an analog-to-digital converter (ADC) input or can be further filtered before being processed by the ADC. For more information on the general procedure to design the filtering and driving stages for SAR ADCs, consult the TI Precision Designs *18 bit, 1Msps Data Acquisition Block Optimized for Lowest Distortion and Noise* (SLAU515), and *18 bit Data Acquisition Block Optimized for Lowest Power* (SLAU513) available for download at www.ti.com

Typical Applications (continued)

8.2.1.3 Application Curve

In frequency inverter applications the power switches must be protected in case of an overcurrent condition. To allow fast powering off of the system, low delay caused by the isolation amplifier is required. Figure 34 shows the typical full-scale step response of the AMC1200.

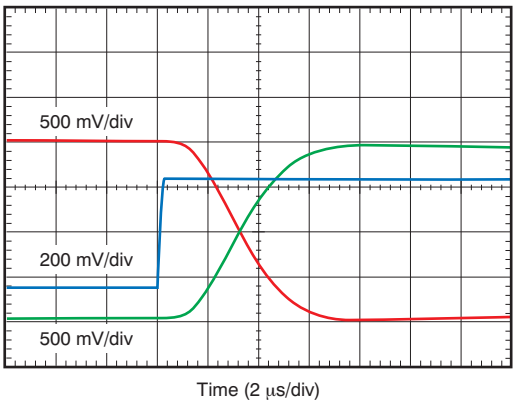


Figure 34. Typical Step Response of the AMC1200

8.2.2 Isolated Voltage Measurement

The AMC1200 and AMC1200B can also be used for isolated voltage measurement applications, as shown in a simplified way in Figure 35. In such applications, usually a resistor divider (R_1 and R_2 in Figure 35) is used to match the relatively small input voltage range of the AMC device. R_2 and the input resistance R_{IN} of the AMC1200 also create a resistance divider that results in additional gain error. With the assumption that R_1 and R_{IN} have a considerably higher value than R_2, the resulting total gain error can be estimated using Equation 1:

$$G_{ERRTOT} = G_{ERR} + \frac{R_2}{R_{IN}} \quad (1)$$

where

- G_{ERR} = the gain error of AMC device.

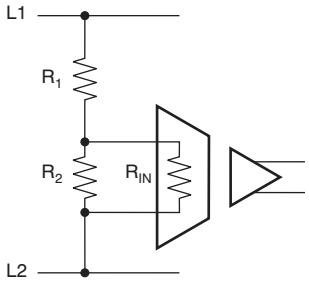


Figure 35. Voltage Measurement Application

9 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply for the AMC1200 (VDD1) is derived from the system supply, as shown in Figure 36. For lowest cost, a Zener diode can be used to limit the voltage to 5 V ± 10%. TI recommends using a 0.1-µF, low-ESR decoupling capacitor for filtering this power-supply. TI also recommends using a 0.1-µF decoupling capacitor for filtering the power-supply on the VDD2 side. For best performance, place these capacitors (C_1 and C_4) as close as possible to the VDD1 and VDD2 pins respectively. If better filtering is required, an additional 1-µF to 10-µF capacitor can be used in parallel to C_1 and C_4.

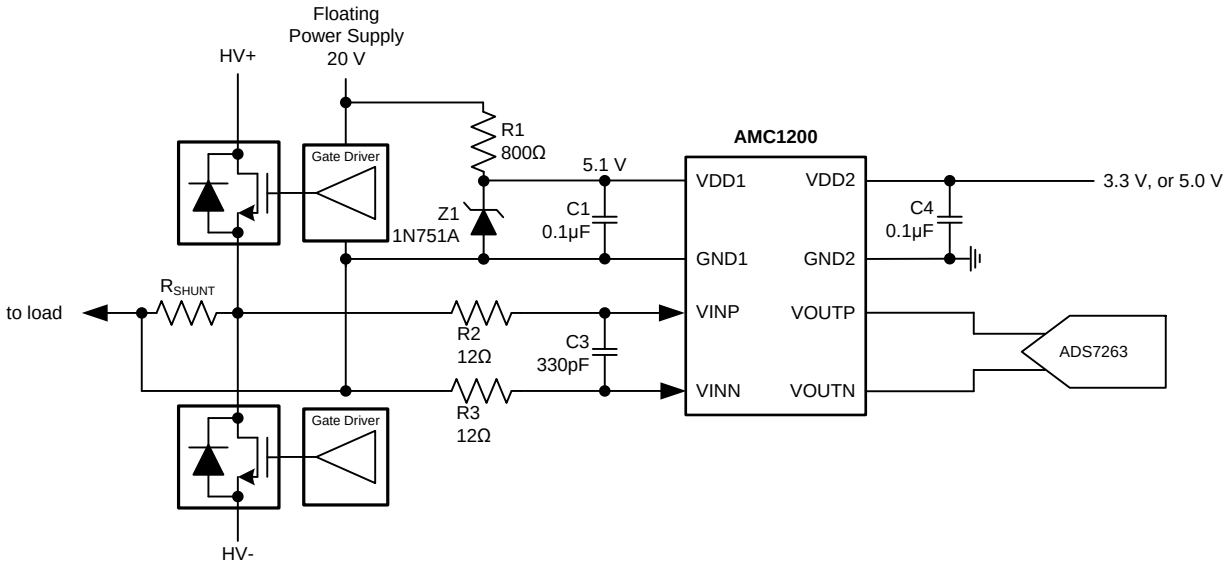


Figure 36. Zener Diode Based High-Side Supply

For higher power efficiency and better performance, a buck converter can be used; an example of such an approach is based on the LM5017. A reference design including performance test results and layout documentation can be downloaded at PMP9480, *Isolated Bias Supplies + Isolated Amplifier Combo for Line Voltage or Current Measurement*.

10 Layout

10.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors that be placed as close as possible to the AMC1200 while maintaining a differential routing of the input signals is shown in Figure 37.

To maintain the isolation barrier and the high CMTI of the device, the distance between the high-side ground (GND1) and the low-side ground (GND2) should be kept at maximum; that is, the entire area underneath the device should be kept free of any conducting materials.

10.2 Layout Example

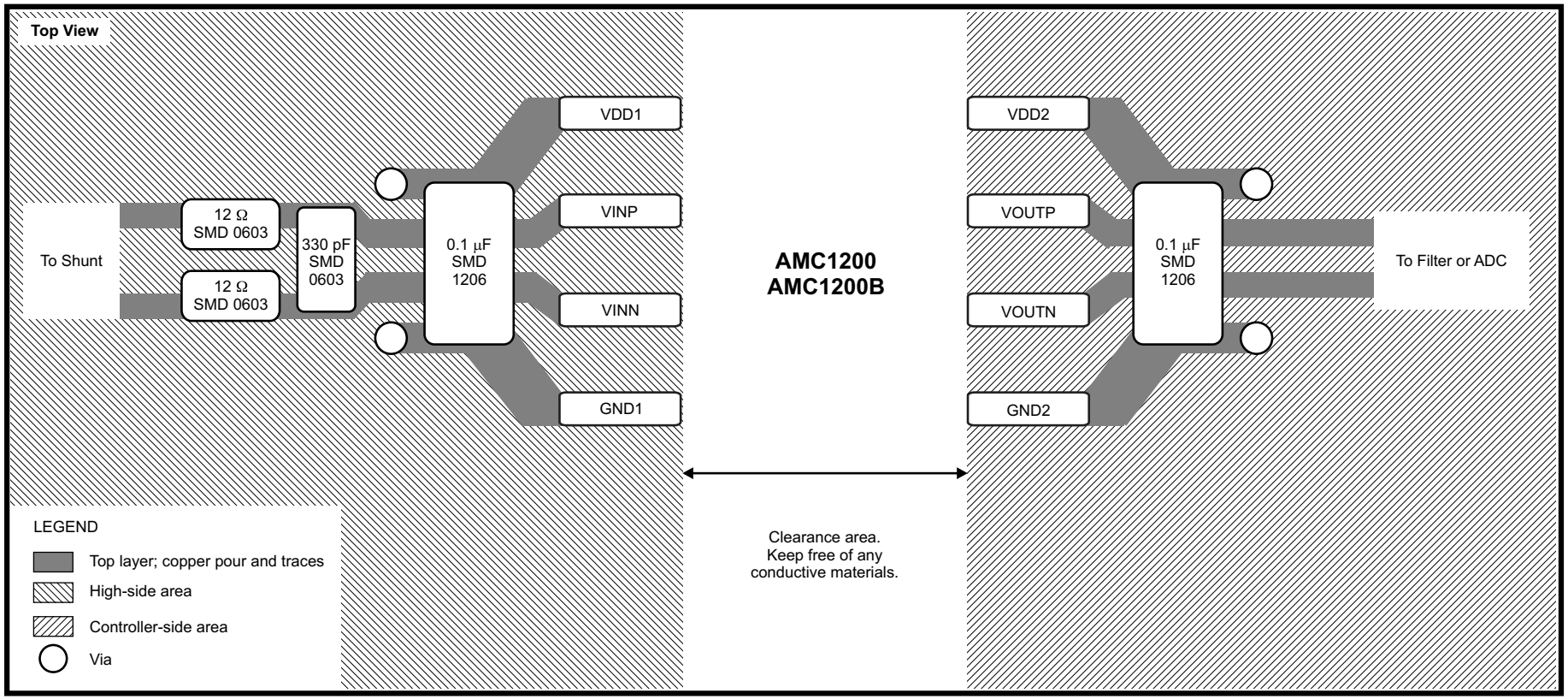


Figure 37. Layout Recommendation

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- *《TI 隔离相关术语》*，SLLA353
- *《针对最低失真和最低噪声进行优化的 18 位 1Msps 数据采集模块》*，SLAU515
- *《针对最低功耗进行优化的 18 位数据采集模块》*，SLAU513
- *《ISO72x 系列数字隔离器高压使用寿命》*，SLLA197
- *《ISO72x 数字隔离器磁场抗扰度》*，SLLA181
- *《AMC1100：使用隔离放大器替代逆变器中的输入主感应变压器》*，SLAA552
- *隔离型电流感测参考设计解决方案，5A，2kV*，TIPD121
- *用于线路电压或电流测量的隔离式偏置电源 + 隔离式放大器组合*，PMP9480
- 《TPS62120 数据表》，SLVSAD5
- 《MSP430F471xx 数据表》，SLAS626
- 《SN6501 数据表》，SLLSEA0
- 《LM5017 数据表》，SNVS783

11.2 相关链接

下面的表格中列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
AMC1200	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
AMC1200B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1200BDUB	ACTIVE	SOP	DUB	8	50	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 105	1200B	Samples
AMC1200BDUBR	ACTIVE	SOP	DUB	8	350	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	1200B	Samples
AMC1200BDWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	AMC1200B	Samples
AMC1200BDWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	AMC1200B	Samples
AMC1200SDUB	ACTIVE	SOP	DUB	8	50	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 105	AMC1200	Samples
AMC1200SDUBR	ACTIVE	SOP	DUB	8	350	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC1200	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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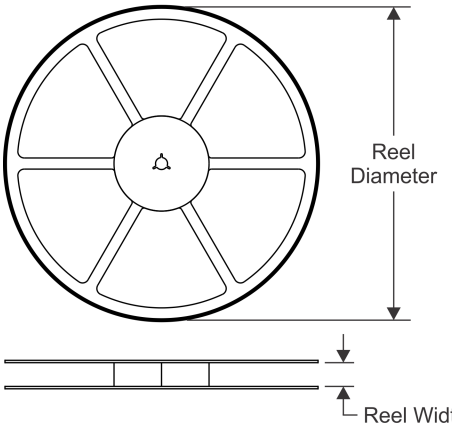
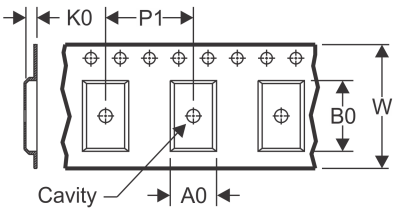
TAPE AND REEL INFORMATION

REEL DIMENSIONS

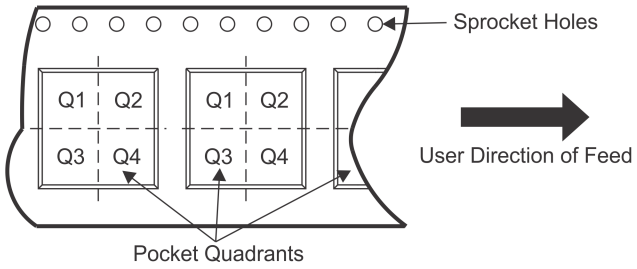


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

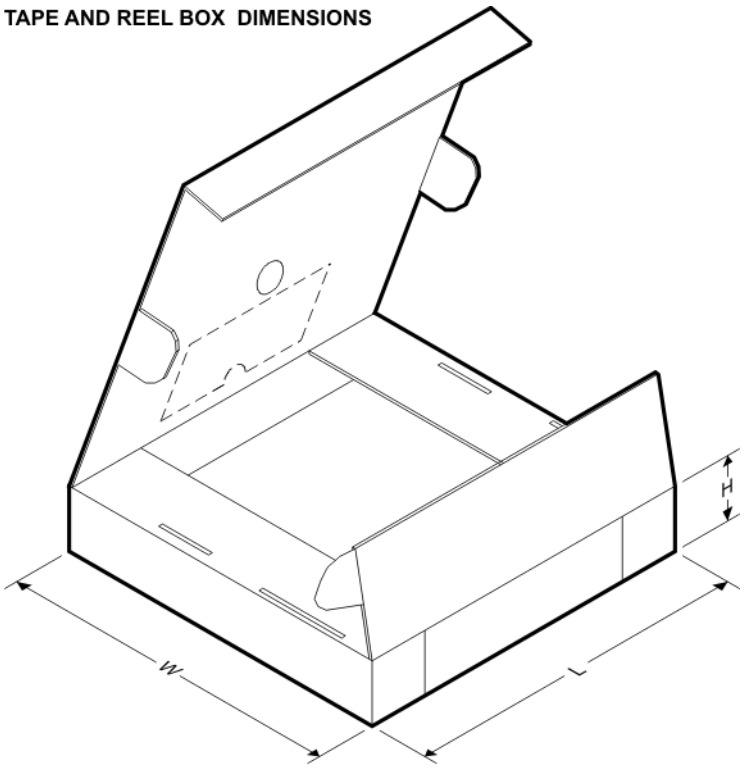
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1200BDUBR	SOP	DUB	8	350	330.0	24.4	13.1	9.75	6.0	16.0	24.0	Q1
AMC1200BDUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1
AMC1200BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1200SDUBR	SOP	DUB	8	350	330.0	24.4	13.1	9.75	6.0	16.0	24.0	Q1
AMC1200SDUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



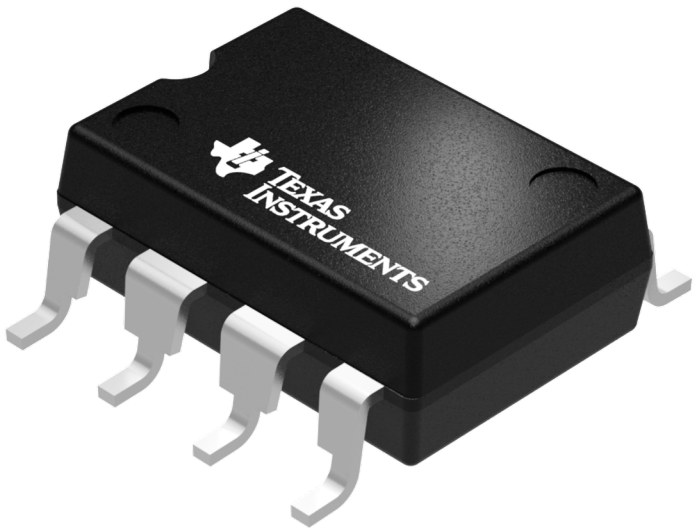
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1200BDUBR	SOP	DUB	8	350	367.0	367.0	45.0
AMC1200BDUBR	SOP	DUB	8	350	346.0	346.0	29.0
AMC1200BDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1200SDUBR	SOP	DUB	8	350	367.0	367.0	45.0
AMC1200SDUBR	SOP	DUB	8	350	346.0	346.0	41.0

GENERIC PACKAGE VIEW

DUB 8 SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

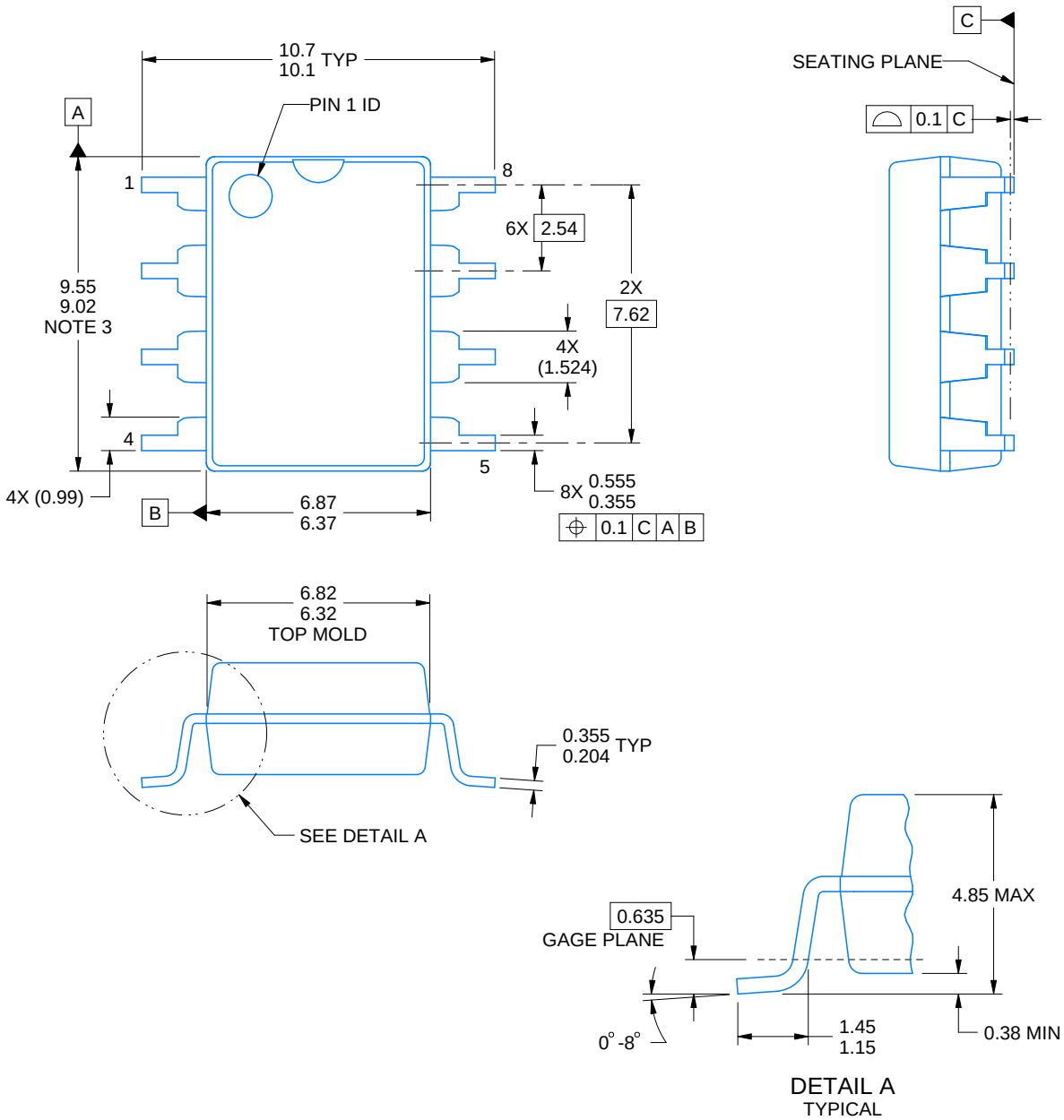
4207614/E

PACKAGE OUTLINE

DUB0008A

SOP - 4.85 mm max height

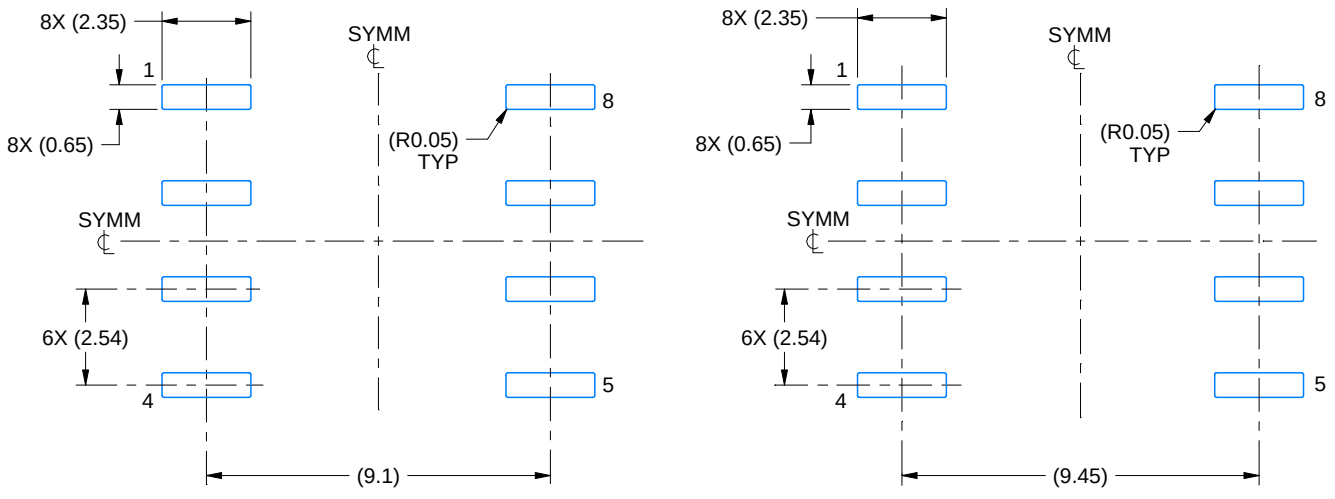
SMALL OUTLINE PACKAGE



4222355/G 04/2019

NOTES:

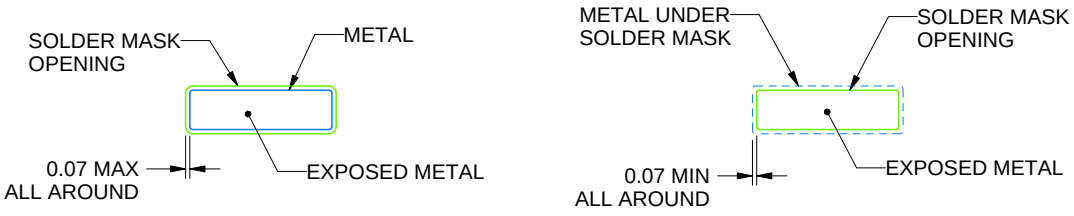
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.254 mm per side.



IPC-7351 NOMINAL
6.75 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
7.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE:5X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4222355/G 04/2019

NOTES: (continued)

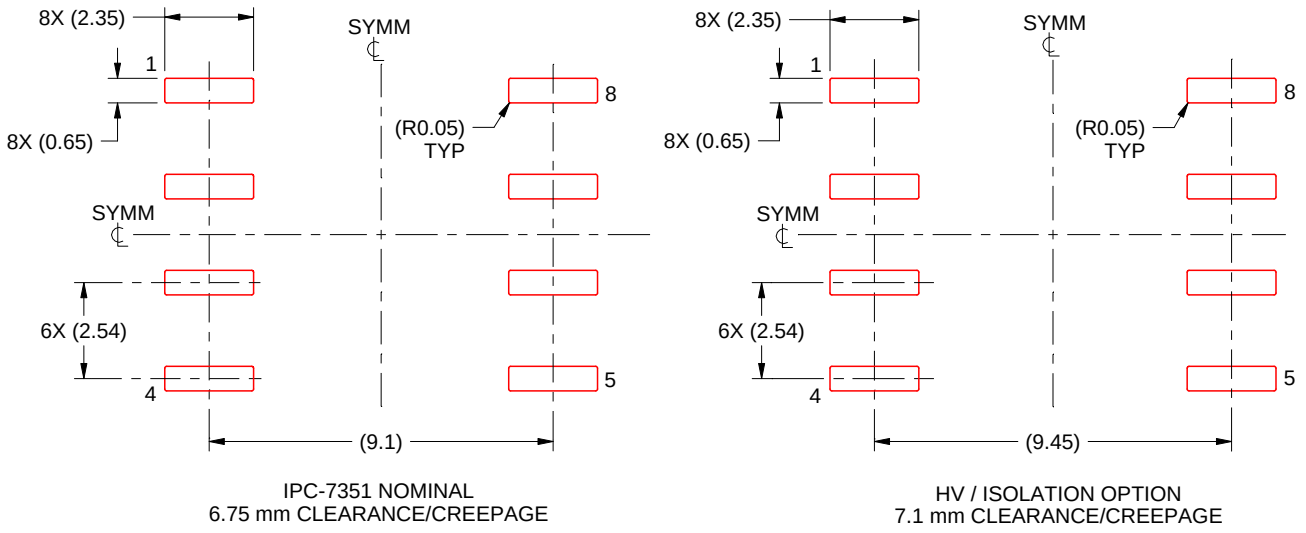
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DUB0008A

SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
6.75 mm CLEARANCE/CREEPAGE

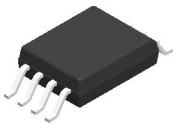
HV / ISOLATION OPTION
7.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:5X

4222355/G 04/2019

NOTES: (continued)

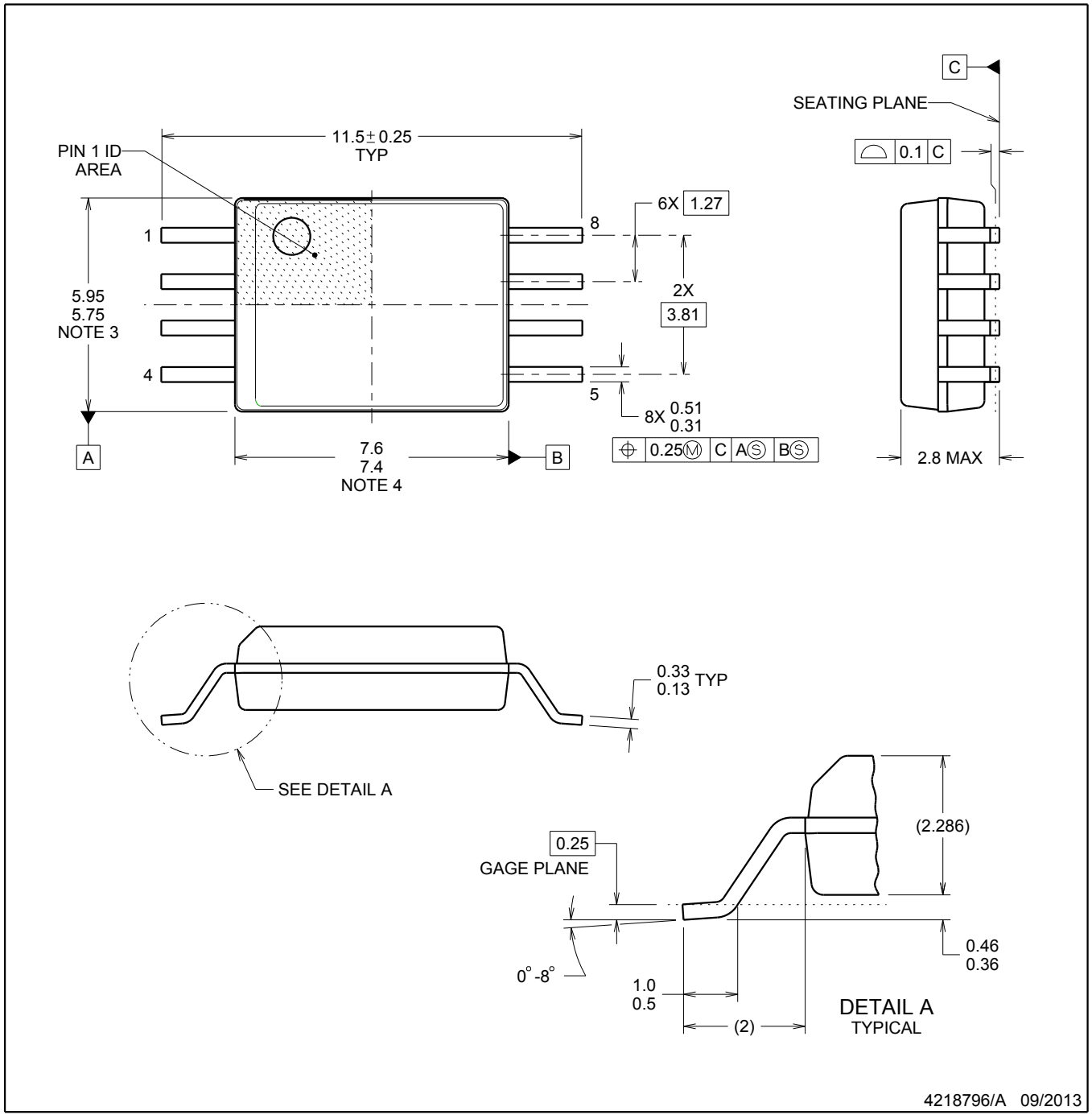
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



DWV0008A

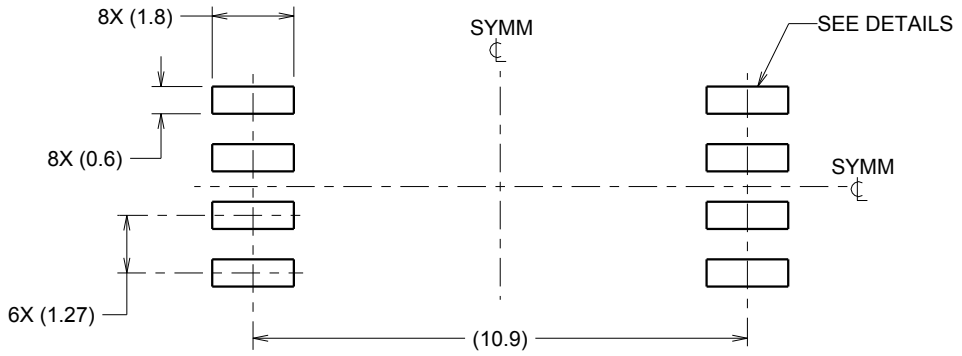
SOIC - 2.8 mm max height

SOIC

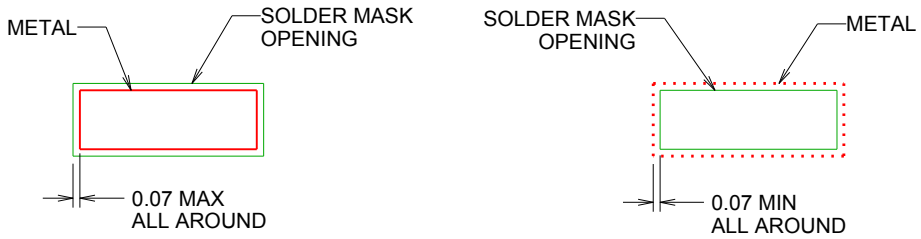


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

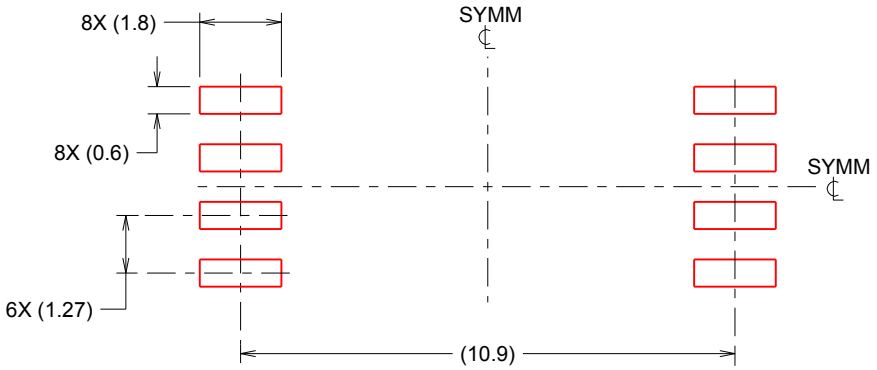
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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