

AMC3302

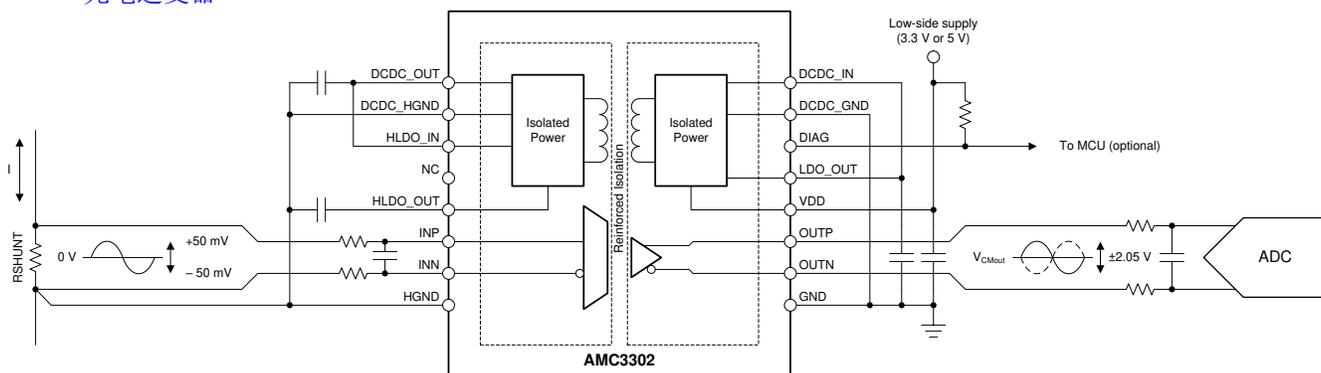
具有集成直流/直流转换器的高精度、 $\pm 50\text{mV}$ 输入、增强型隔离放大器

1 特性

- 3.3V 或 5V 单电源，具有集成直流/直流转换器
- $\pm 50\text{mV}$ 输入电压范围，针对使用分流电阻器测量电流进行了优化
- 固定增益：41
- 低直流误差：
 - 失调电压： $\pm 50\mu\text{V}$ (最大值)
 - 温漂： $\pm 0.5\mu\text{V}/^\circ\text{C}$ (最大值)
 - 增益误差： $\pm 0.2\%$ (最大值)
 - 增益误差漂移： $\pm 35\text{ppm}/^\circ\text{C}$ (最大值)
 - 非线性度： $\pm 0.03\%$ (最大值)
- 高 CMTI: $85\text{kV}/\mu\text{s}$ (最小值)
- 系统级诊断功能
- 符合 CISPR-11 和 CISPR-25 EMI 标准
- 安全相关认证：
 - 符合 DIN VDE V 0884-11 标准的 $6000\text{V}_{1\text{PK}}2$ 增强型隔离
 - 符合 UL1577 标准且长达 1 分钟的 $4250\text{V}_{1\text{RMS}}2$ 隔离
- 可在扩展工业温度范围内正常工作： -40°C 至 $+125^\circ\text{C}$

2 应用

- 可用于以下应用的隔离式电流感应：
 - 保护继电器
 - 电机驱动器
 - 电源
 - 光电逆变器



典型应用

3 说明

AMC3302 是一款精密的隔离放大器，针对基于分流器的电流测量进行了优化。这款完全集成的隔离式直流/直流转换器可实现器件低侧的单电源运行，使该器件成为空间受限应用的独特解决方案。增强型电容式隔离栅已通过 VDE V 0884-11 和 UL1577 认证，并支持高达 1.2kVRMS 的工作电压。

该隔离栅可将系统中以不同共模电压电平运行的各器件隔开，并保护电压较低的器件免受高电压冲击。

AMC3302 的输入针对直接连接低阻抗分流电阻器或另一个具有低信号电平的低阻抗电压源的情况进行了优化。出色的直流精度和低温漂支持在 -40°C 至 $+125^\circ\text{C}$ 的扩展工业温度范围内进行精确的电流测量。

AMC3302 的集成直流/直流转换器故障检测和诊断输出引脚可简化系统级设计和诊断。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
AMC3302	SOIC (16)	10.30mm × 7.50mm

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (August 2020) to Revision A (February 2021)	Page
• 将文档状态从预告信息更改为量产数据.....	1

5 Pin Configuration and Functions

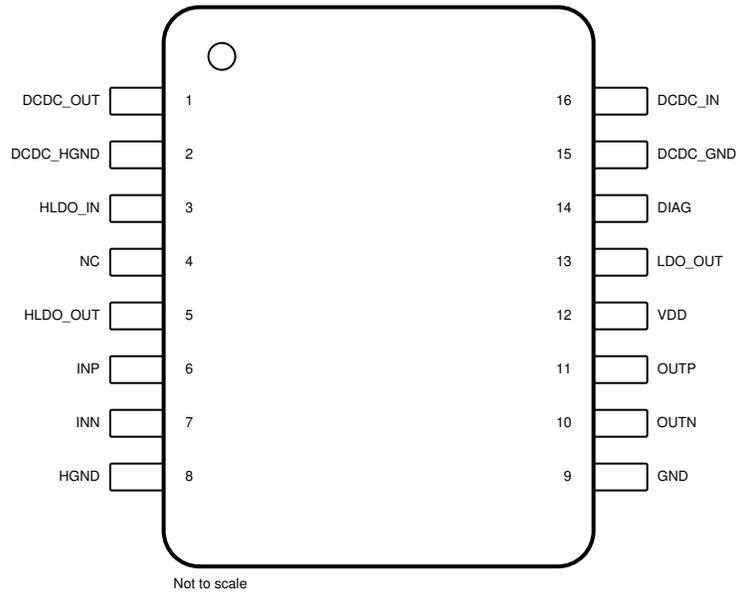


图 5-1. DWE Package, 16-Pin SOIC, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DCDC_OUT	Power	High-side output of the isolated DC/DC converter; connect this pin to the HLDO_IN pin. ⁽¹⁾
2	DCDC_HGND	High-side power ground	High-side ground reference for the isolated DC/DC converter; connect this pin to the HGND pin.
3	HLDO_IN	Power	Input of the high-side LDO; connect this pin to the DCDC_OUT pin. ⁽¹⁾
4	NC	—	No internal connection; connect this pin to HGND or leave this pin unconnected.
5	HLDO_OUT	Power	Output of the high-side LDO. ⁽¹⁾
6	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage. ⁽²⁾
7	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage. ⁽²⁾
8	HGND	High-side signal ground	High-side analog ground; connect this pin to the DCDC_HGND pin.
9	GND	Low-side signal ground	Low-side analog ground; connect this pin to the DCDC_GND pin.
10	OUTN	Analog output	Inverting analog output.
11	OUTP	Analog output	Noninverting analog output.
12	VDD	Low-side power	Low-side power supply. ⁽¹⁾
13	LDO_OUT	Power	Output of the low-side LDO; connect this pin to the DCDC_IN pin. ⁽¹⁾
14	DIAG	Digital output	Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used.
15	DCDC_GND	Low-side power ground	Low-side ground reference for the isolated DC/DC converter; connect this pin to the GND pin.
16	DCDC_IN	Power	Low-side input of the isolated DC/DC converter; connect this pin to the LDO_OUT pin. ⁽¹⁾

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

(2) See the [Layout](#) section for details.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	- 0.3	6.5	V
Analog input voltage	INP, INN	HGND - 6	V _{HLD0_OUT} + 0.5	V
Analog output voltage	OUTP, OUTN	GND - 0.5	VDD + 0.5	V
Digital output voltage	DIAG	GND - 0.5	6.5	V
Input current	Continuous, any pin except power-supply pins	- 10	10	mA
Temperature	Junction, T _J		150	°C
	Storage, T _{stg}	- 65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JESD22-C101 (2)	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
POWER SUPPLY							
VDD	Low-side power supply	VDD to GND		3	3.3	5.5	V
ANALOG INPUT							
V _{Clipping}	Differential input voltage before clipping output	V _{IN} = V _{INP} - V _{INN}		±64			mV
V _{FSR}	Specified linear differential full-scale voltage	V _{IN} = V _{INP} - V _{INN}		- 50		50	mV
	Absolute common-mode input voltage (1)	(V _{INP} + V _{INN}) / 2 to HGND		- 2		V _{HLD0_OUT}	V
V _{CM}	Operating common-mode input voltage	(V _{INP} + V _{INN}) / 2 to HGND		- 0.032		1	V
TEMPERATURE RANGE							
T _A	Specified ambient temperature			- 40		125	°C

- (1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AMC3302	UNIT
		DWE (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	°C/W
Y_{JT}	Junction-to-top characterization parameter	16.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	VDD = 5.5 V			231	mW
		VDD = 3.6 V			151	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage ⁽¹⁾	Shortest pin-to-pin distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance - capacitive signal isolation)	≥ 21	μm
		Minimum internal gap (internal clearance - transformer power isolation)	≥ 120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	At AC voltage (bipolar)	1700	V _{PK}
V _{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	1200	V _{RMS}
		At DC voltage	1700	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification test)	6000	V _{PK}
		V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test)	7200	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50-μs waveform, V _{TEST} = 1.6 × V _{IOSM} = 10000 V _{PK} (qualification)	6250	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a, after input/output safety test subgroup 2 / 3, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s, V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.5 V _{PP} at 1 MHz	~3.5	pF
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V at T _A = 25°C	> 10 ¹²	Ω
		V _{IO} = 500 V at 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 4250 V _{RMS} or 6000 V _{DC} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production test)	4250	V _{RMS}

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings must be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

Safety limiting ⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety input, output, or supply current	R _{θJA} = 73.5°C/W, VDD = 5.5 V, T _J = 150°C, T _A = 25°C			309	mA
		R _{θJA} = 73.5°C/W, VDD = 3.6 V, T _J = 150°C, T _A = 25°C			472	
P _S	Safety input, output, or total power	R _{θJA} = 73.5°C/W, T _J = 150°C, T _A = 25°C			1700	mW
T _S	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where T_{J(max)} is the maximum junction temperature.

$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum low-side voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ to 5.5 V , $\text{INP} = -50\text{ mV}$ to $+50\text{ mV}$, $\text{INN} = \text{HGND} = 0\text{ V}$, and the external components listed in the *Typical Application* section; typical specifications are at $T_A = 25^\circ\text{C}$, and $V_{DD} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Single-ended input resistance	$\text{INN} = \text{HGND}$		4.75		$\text{k}\Omega$
R_{IND}	Differential input resistance			4.9		
I_{IB}	Input bias current	$\text{INP} = \text{INN} = \text{HGND}$; $I_{\text{IB}} = (I_{\text{IBP}} + I_{\text{IBN}}) / 2$	-48.5	-36	-28.5	μA
I_{IO}	Input offset current	$I_{\text{IO}} = I_{\text{IBP}} - I_{\text{IBN}}$; $\text{INP} = \text{INN} = \text{HGND}$		± 10		nA
C_{IN}	Single-ended input capacitance	$\text{INN} = \text{HGND}$, $f_{\text{IN}} = 275\text{ kHz}$		4		pF
C_{IND}	Differential input capacitance	$f_{\text{IN}} = 275\text{ kHz}$		2		pF
ANALOG OUTPUT						
	Nominal gain			41		V/V
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
V_{CLIPout}	Clipping differential output voltage	$V_{\text{OUT}} = (V_{\text{OUTP}} - V_{\text{OUTN}})$; $ V_{\text{IN}} = V_{\text{INP}} - V_{\text{INN}} > V_{\text{Clipping}}$	-2.52	± 2.49	2.52	V
V_{Failsafe}	Failsafe differential output voltage	$V_{\text{OUT}} = (V_{\text{OUTP}} - V_{\text{OUTN}})$; $V_{\text{DCDC_OUT}} \leq V_{\text{DCDCUV}}$, or $V_{\text{HLDO_OUT}} \leq V_{\text{HLDOUV}}$	-2.63	-2.57	-2.53	V
BW	Output bandwidth		300	340		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		0.2		Ω
	Output short-circuit current	On OUTP or OUTN , sourcing or sinking, $\text{INP} = \text{INN} = \text{HGND}$, outputs shorted to either GND or VDD		14		mA
CMTI	Common-mode transient immunity	$ \text{HGND} - \text{GND} = 2\text{ kV}$	85	135		$\text{kV}/\mu\text{s}$
ACCURACY						
V_{OS}	Input offset voltage ⁽¹⁾	$T_A = 25^\circ\text{C}$, $\text{INP} = \text{INN} = \text{HGND}$	-50	± 15	50	μV
TCV_{OS}	Input offset drift ⁽¹⁾		-0.5	± 0.1	0.5	$\mu\text{V}/^\circ\text{C}$
E_{G}	Gain error ⁽¹⁾	$T_A = 25^\circ\text{C}$	-0.2%	$\pm 0.04\%$	0.2%	
TCE_{G}	Gain error drift ⁽¹⁾		-35	± 10	35	$\text{ppm}/^\circ\text{C}$
	Nonlinearity ⁽¹⁾		-0.03%	$\pm 0.002\%$	0.03%	
SNR	Signal-to-noise ratio	$V_{\text{IN}} = 0.1 V_{\text{PP}}$, $f_{\text{IN}} = 1\text{ kHz}$, $\text{BW} = 10\text{ kHz}$, 10 kHz filter	77	81		dB
		$V_{\text{IN}} = 0.1 V_{\text{PP}}$, $f_{\text{IN}} = 10\text{ kHz}$, $\text{BW} = 100\text{ kHz}$, 1 MHz filter		70		
		$V_{\text{IN}} = 0.1 V_{\text{PP}}$, $f_{\text{IN}} = 1\text{ kHz}$, $\text{BW} = 10\text{ kHz}$, 1 MHz filter	77	81		
THD	Total harmonic distortion	$V_{\text{IN}} = 0.1 V_{\text{pp}}$, $f_{\text{IN}} = 10\text{ kHz}$, $\text{BW} = 100\text{ kHz}$		-85		dB
	Output noise	$\text{INP} = \text{INN} = \text{HGND}$, $f_{\text{IN}} = 0\text{ Hz}$, $\text{BW} = 100\text{ kHz}$		340		μV_{RMS}
CMRR	Common-mode rejection ratio	$f_{\text{IN}} = 0\text{ Hz}$, $V_{\text{CM min}} \leq V_{\text{CM}} \leq V_{\text{CM max}}$		-101		dB
		$f_{\text{IN}} = 10\text{ kHz}$, $V_{\text{CM min}} \leq V_{\text{CM}} \leq V_{\text{CM max}}$		-101		
PSRR	Power-supply rejection ratio	V_{DD} from 3.0 V to 5.5 V, at dc, input referred		-120		dB
		$\text{INP} = \text{INN} = \text{HGND}$, V_{DD} from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple, input referred		-108		

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ to 5.5 V , $\text{INP} = -50\text{ mV}$ to $+50\text{ mV}$, $\text{INN} = \text{HGND} = 0\text{ V}$, and the external components listed in the *Typical Application* section; typical specifications are at $T_A = 25^\circ\text{C}$, and $V_{DD} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I _{DD}	Low-side supply current	no external load on HLDO		27.5	40	mA
		1 mA external load on HLDO		29.5	42	
V _{DCDC_OUT}	DCDC output voltage	DCDC_OUT to HGND	3.1	3.5	4.65	V
V _{DCDCUV}	DCDC output undervoltage detection threshold voltage	DCDC output falling	2.1	2.25		V
V _{HLDO_OUT}	High-side LDO output voltage	HLDO to HGND, up to 1 mA external load	3	3.2	3.4	V
V _{HLDOUV}	High-side LDO output undervoltage detection threshold voltage	HLDO output falling	2.4	2.6		V
I _H	High-side supply current for auxiliary circuitry	Load connected from HLDO_OUT to HGND, non-switching			1	mA
t _{AS}	Analog settling time	VDD step to 3.0 V, to OUTP and OUTN valid, 0.1% settling		0.9	1.4	ms

(1) The typical value includes one standard deviation ("sigma") at nominal operating conditions.

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _r	Output signal rise time			1.3		μs
t _f	Output signal fall time			1.3		μs
	V _{INx} to V _{OUTx} signal delay (50% - 10%)	Unfiltered output		1.2	1.5	μs
	V _{INx} to V _{OUTx} signal delay (50% - 50%)	Unfiltered output		1.6	2.1	μs
	V _{INx} to V _{OUTx} signal delay (50% - 90%)	Unfiltered output		2.3	3	μs

6.11 Timing Diagram

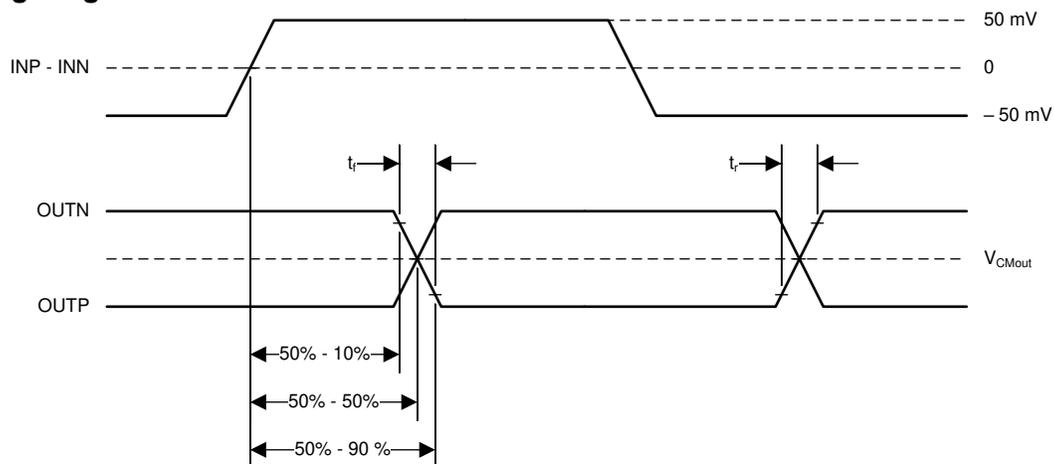
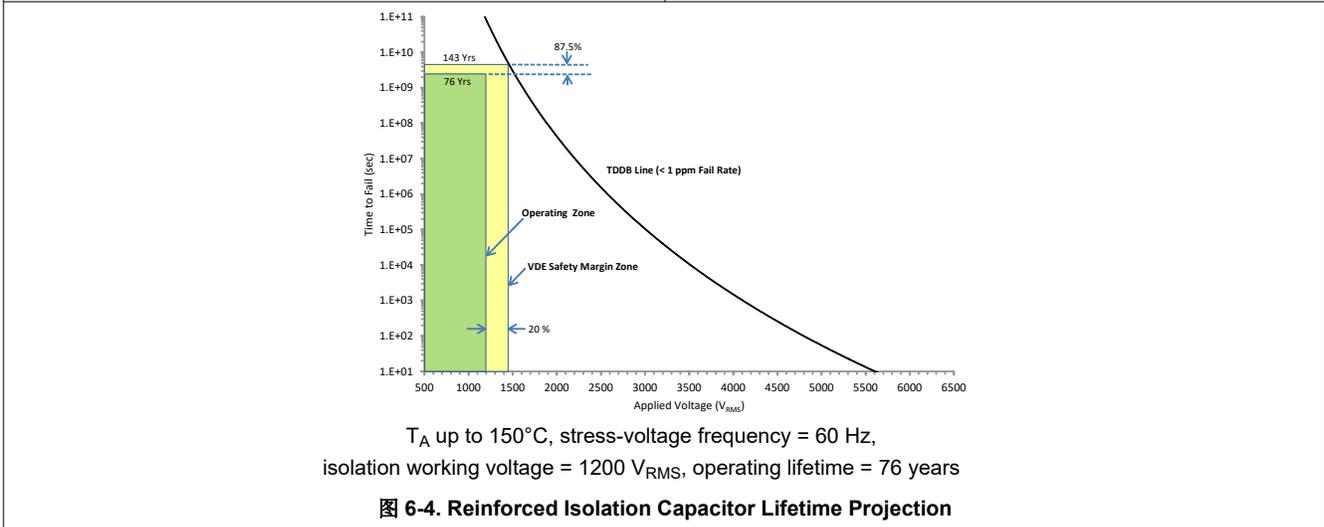
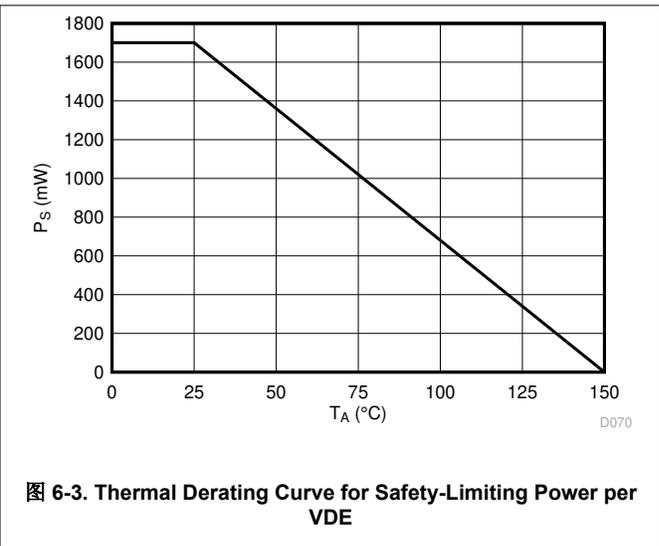
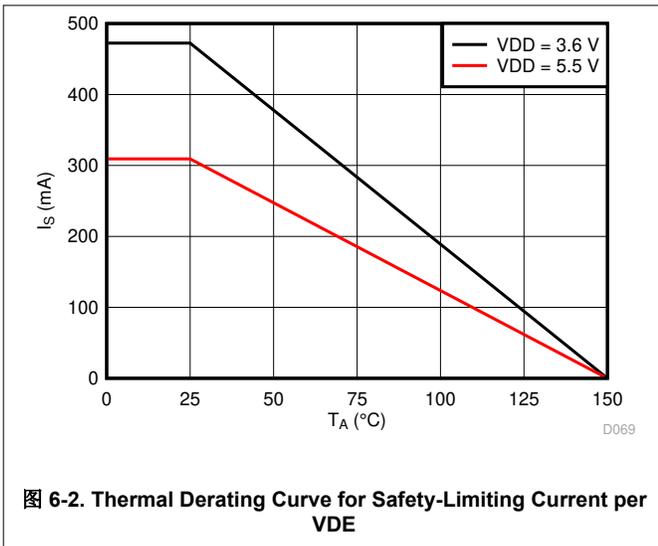


图 6-1. Rise, Fall, and Delay Time Waveforms

6.12 Insulation Characteristics Curves



6.13 Typical Characteristics

at VDD = 3.3 V, INP = - 50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

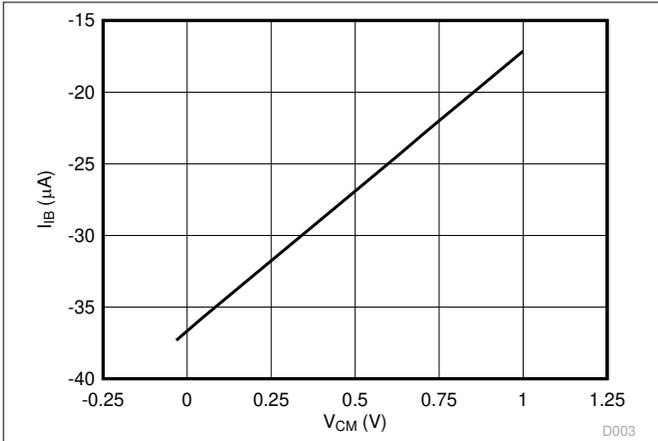


图 6-5. Input Bias Current vs Common-Mode Input Voltage

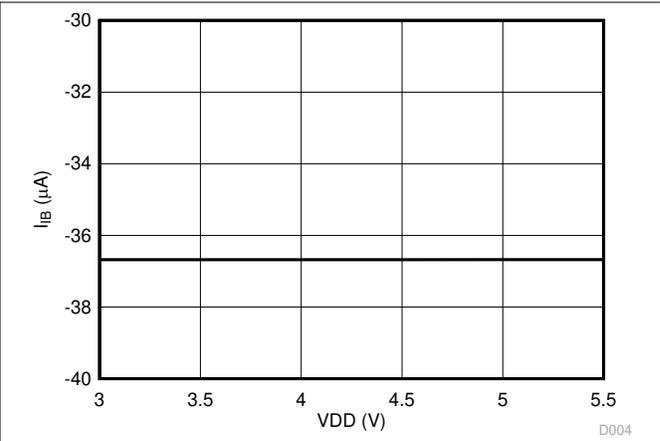


图 6-6. Input Bias Current vs Supply Voltage

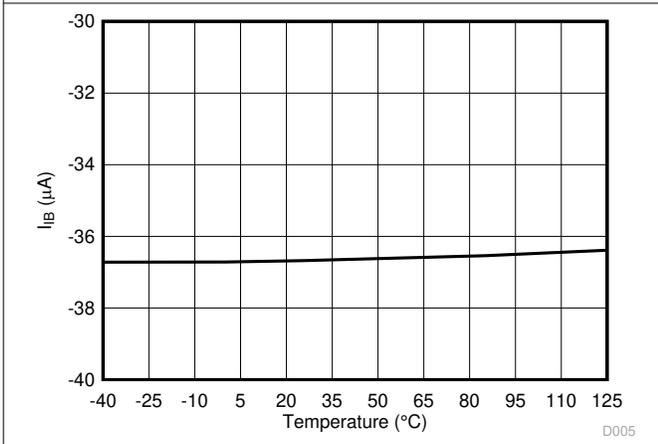


图 6-7. Input Bias Current vs Temperature

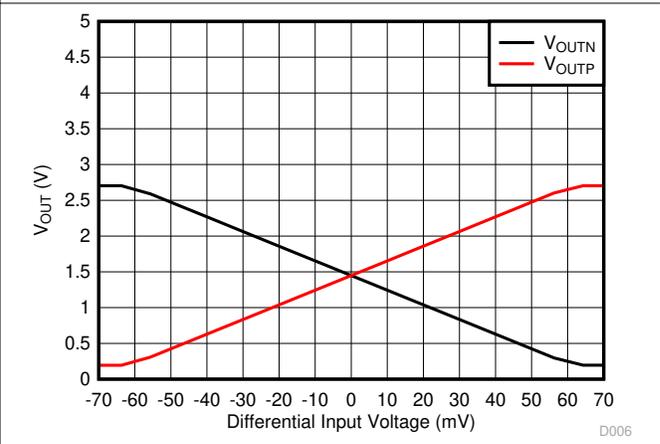


图 6-8. Output Voltage vs Input Voltage

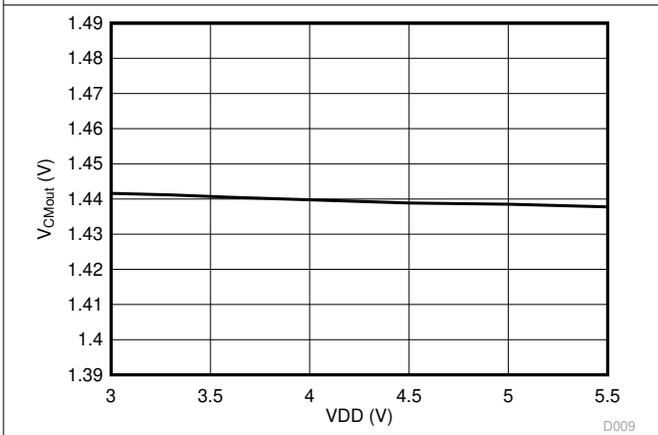


图 6-9. Output Common-Mode Voltage vs Supply Voltage

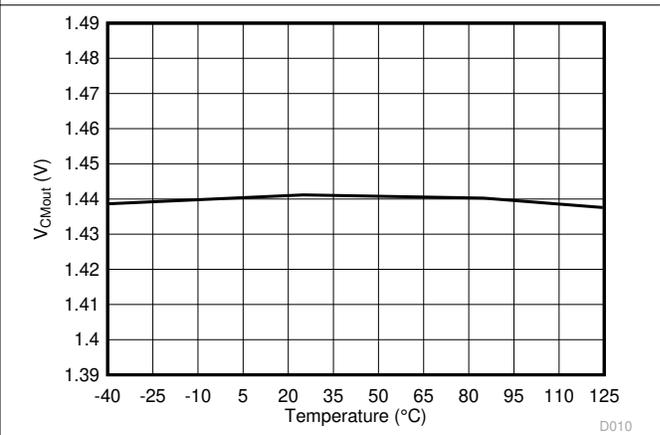


图 6-10. Output Common-Mode Voltage vs Temperature

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = - 50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

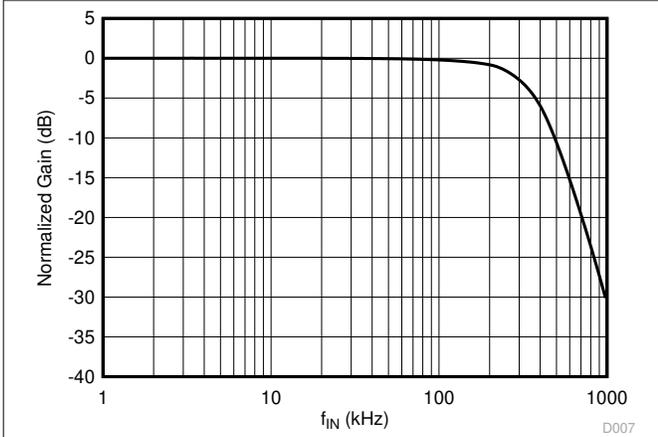


图 6-11. Normalized Gain vs Input Frequency

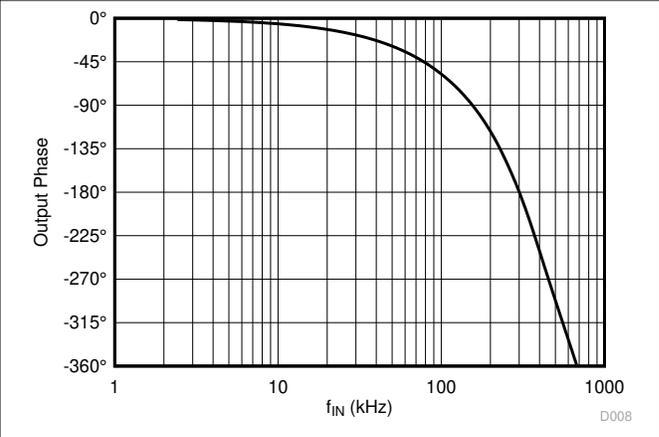


图 6-12. Output Phase vs Input Frequency

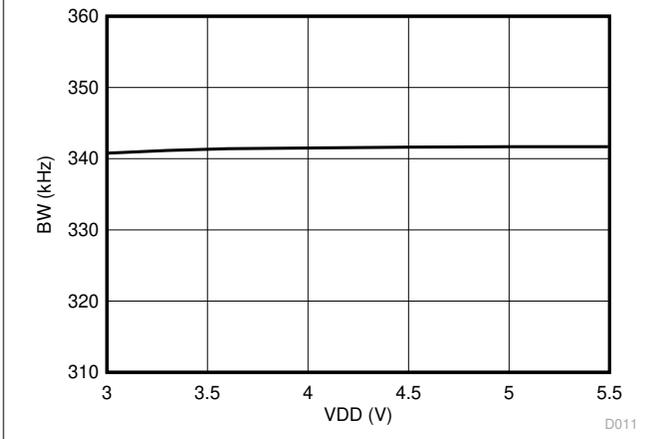


图 6-13. Output Bandwidth vs Supply Voltage

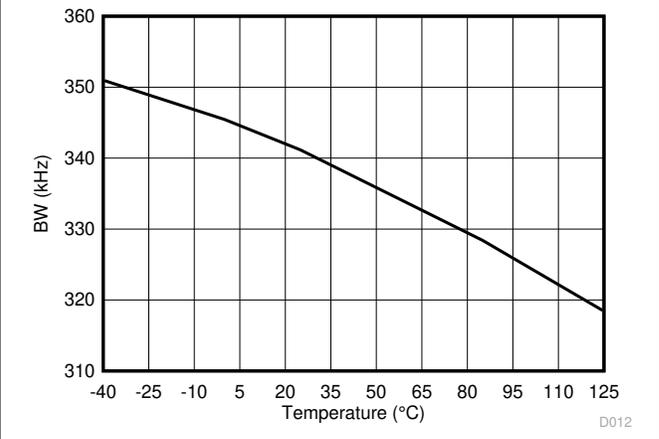


图 6-14. Output Bandwidth vs Temperature

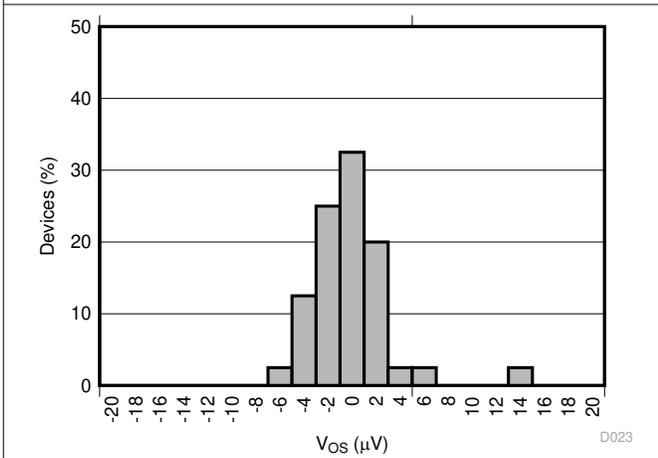


图 6-15. Input Offset Voltage Histogram

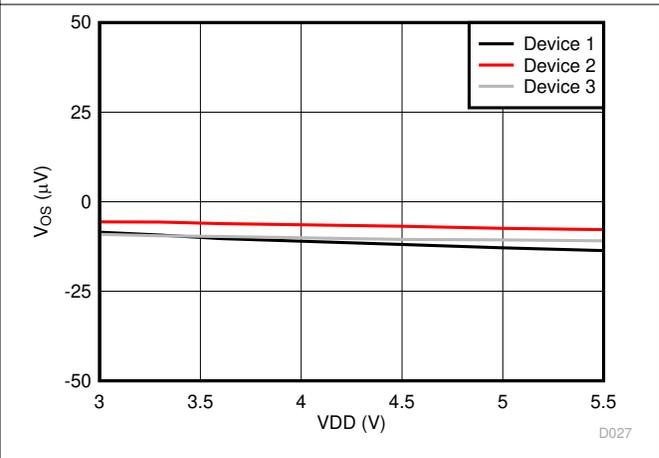
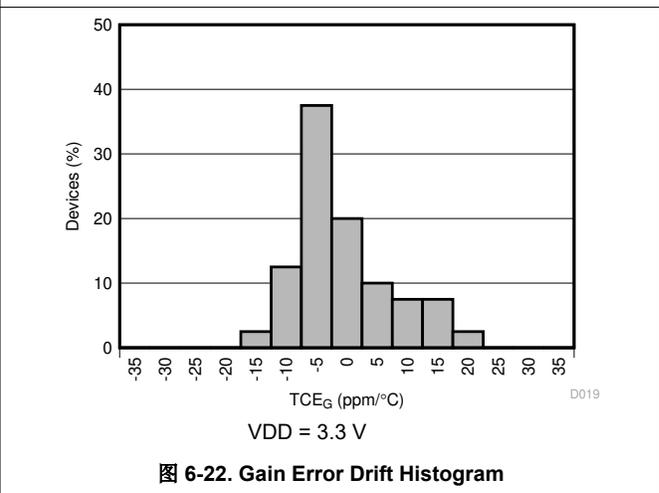
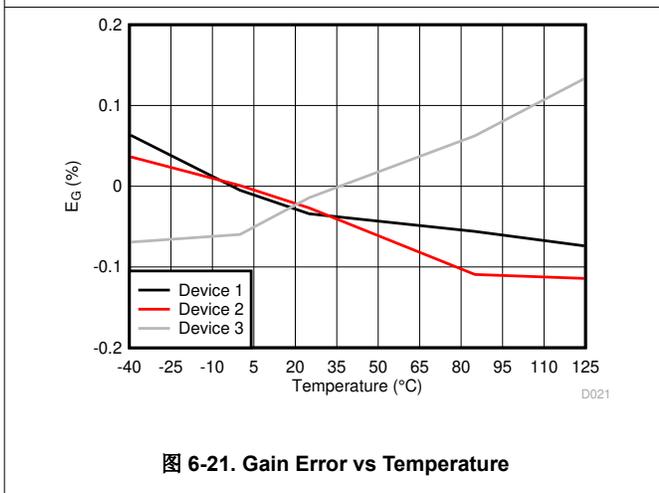
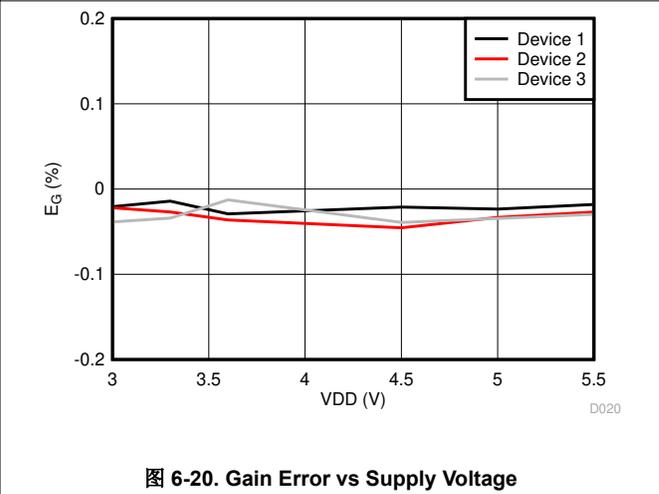
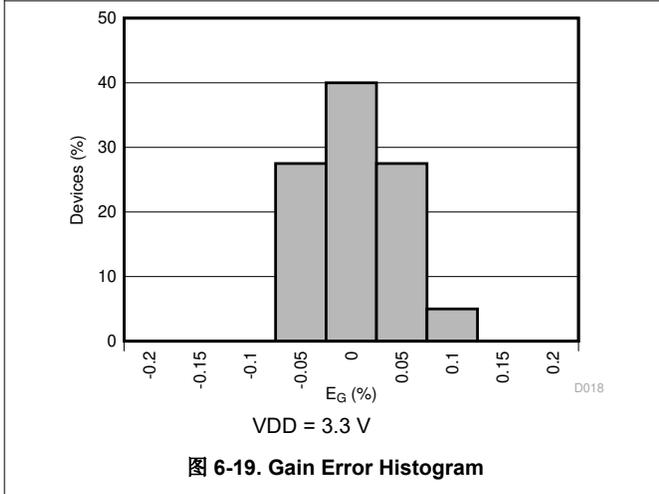
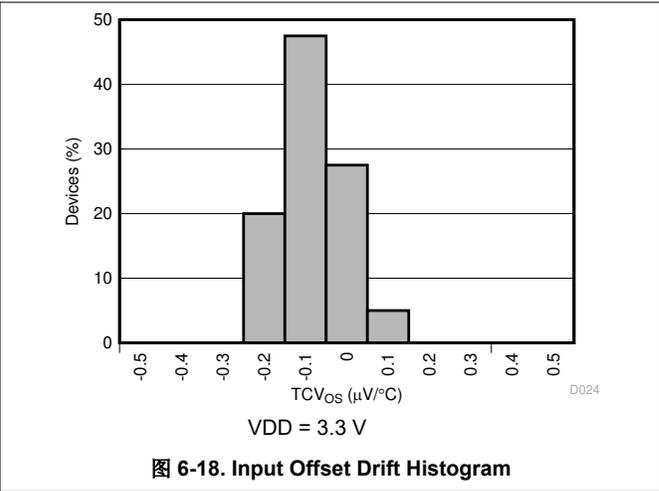
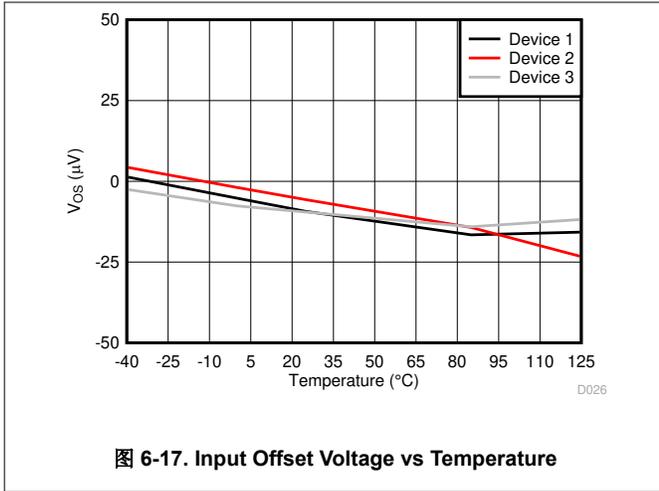


图 6-16. Input Offset Voltage vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = -50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)



6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = - 50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

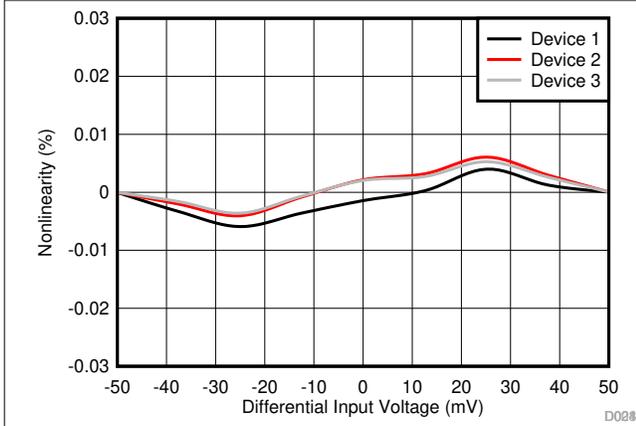


图 6-23. Nonlinearity vs Input Voltage

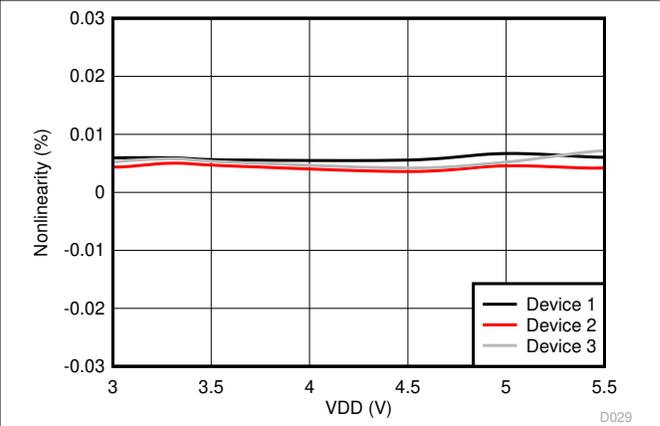


图 6-24. Nonlinearity vs Supply Voltage

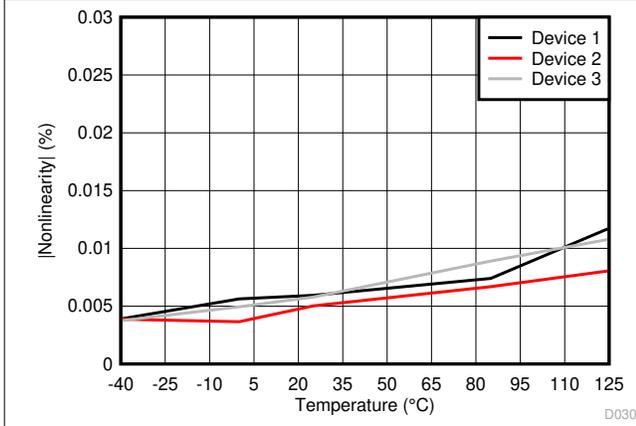


图 6-25. Nonlinearity vs Temperature

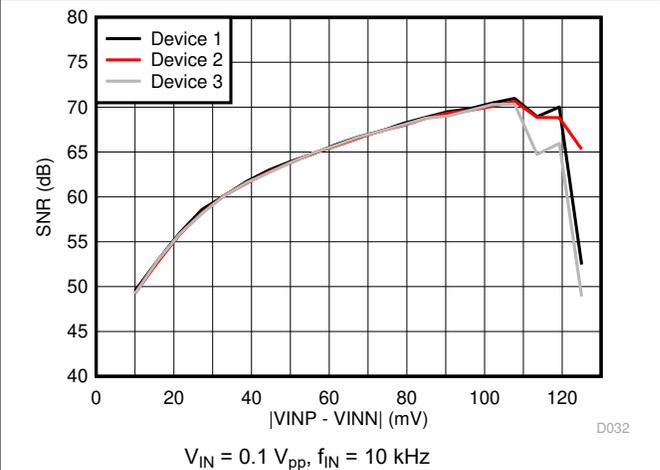


图 6-26. Signal-to-Noise Ratio vs Input Voltage

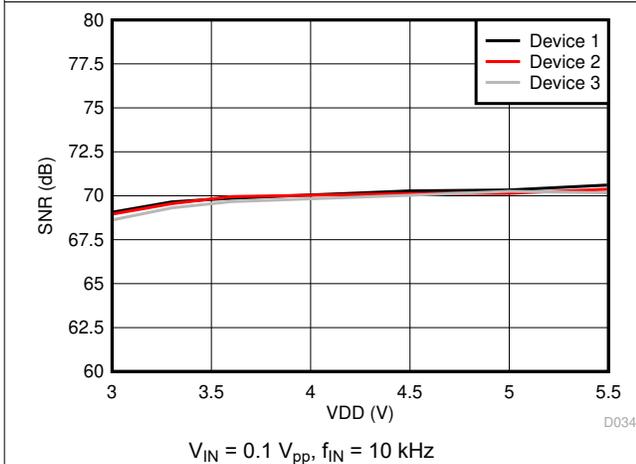


图 6-27. Signal-to-Noise Ratio vs Supply Voltage

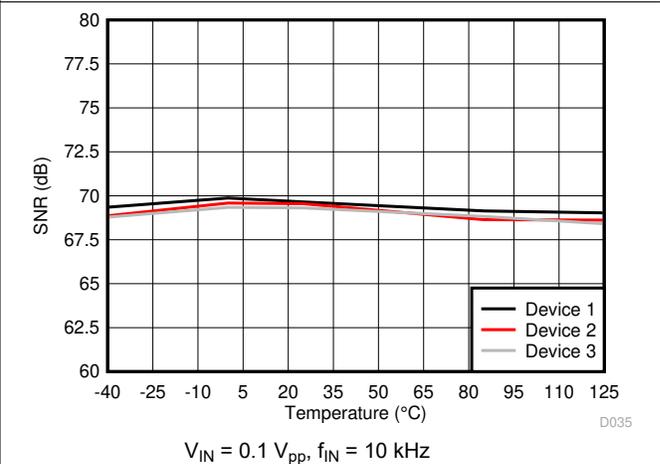


图 6-28. Signal-to-Noise Ratio vs Temperature

6.13 Typical Characteristics (continued)

at $V_{DD} = 3.3\text{ V}$, $INP = -50\text{ mV to }+50\text{ mV}$, $INN = HGND = 0\text{ V}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

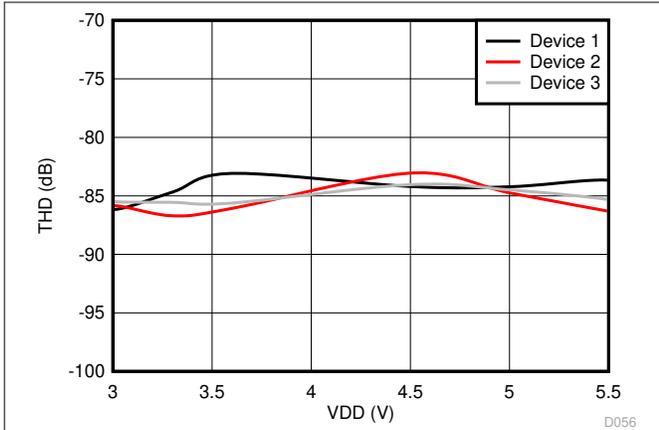


图 6-29. Total Harmonic Distortion vs Supply Voltage

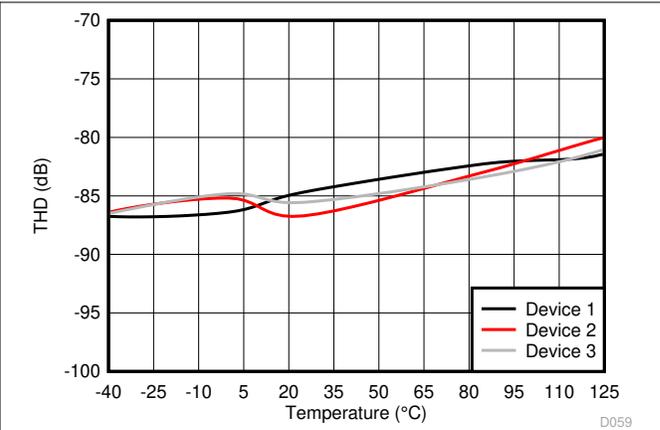


图 6-30. Total Harmonic Distortion vs Temperature

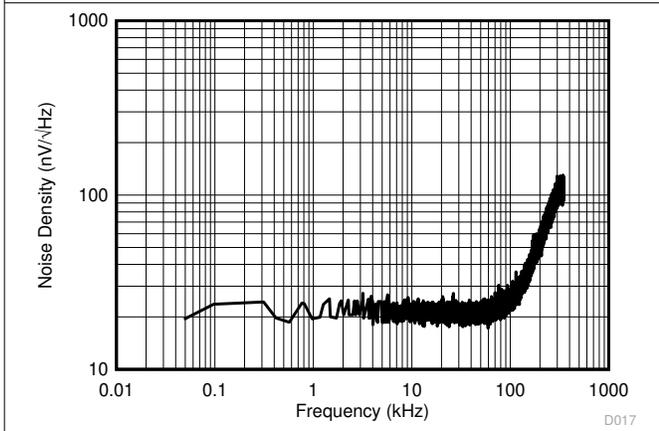


图 6-31. Input-Referred Noise Density vs Frequency

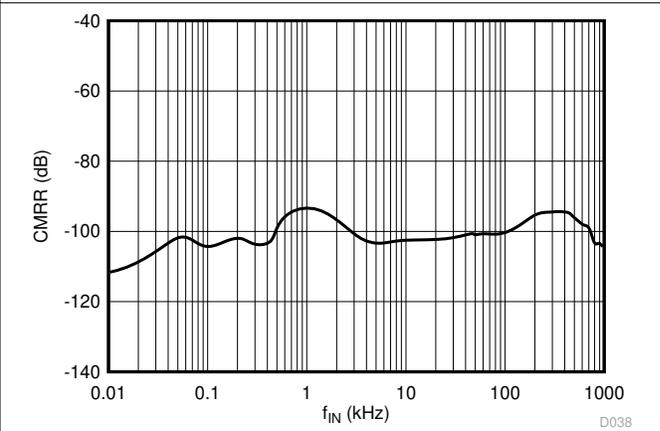


图 6-32. Common-Mode Rejection Ratio vs Input Frequency

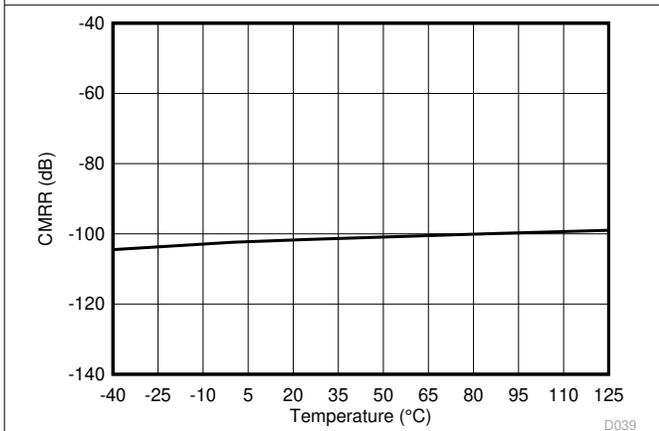


图 6-33. Common-Mode Rejection Ratio vs Temperature

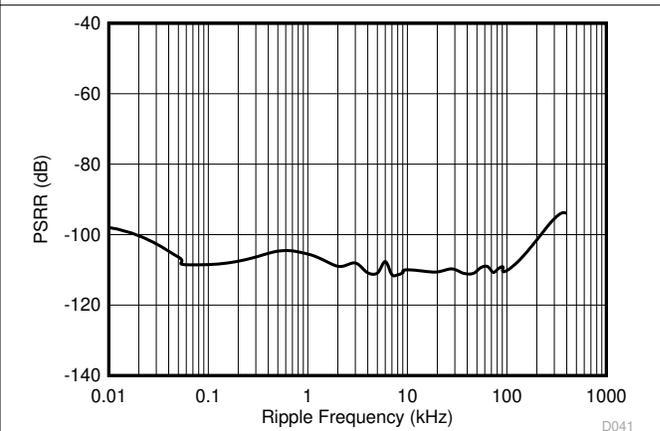


图 6-34. Power-Supply Rejection Ratio vs Ripple Frequency

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = - 50 mV to +50 mV, INN = HGND = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

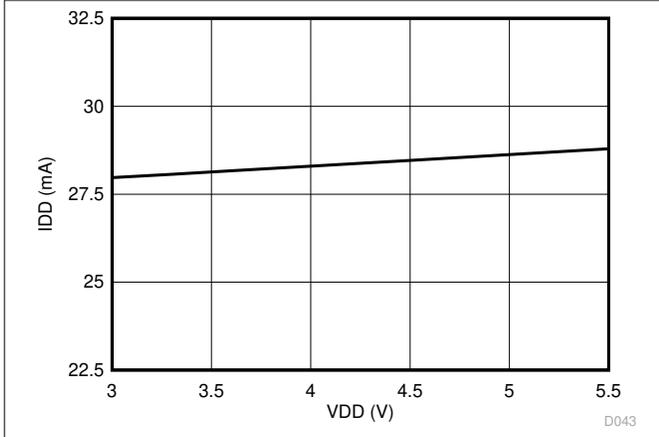


图 6-35. Supply Current vs Supply Voltage

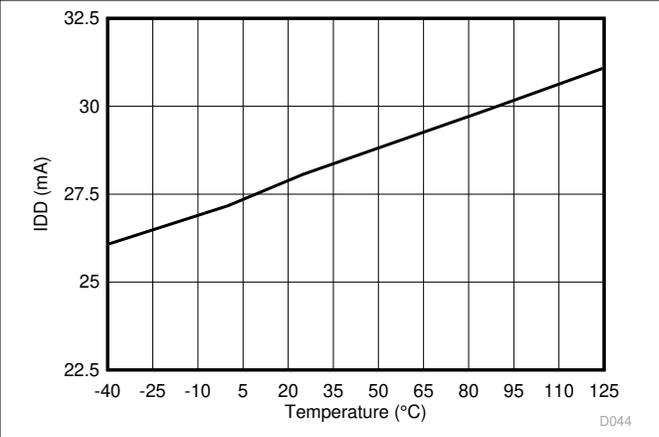


图 6-36. Supply Current vs Temperature

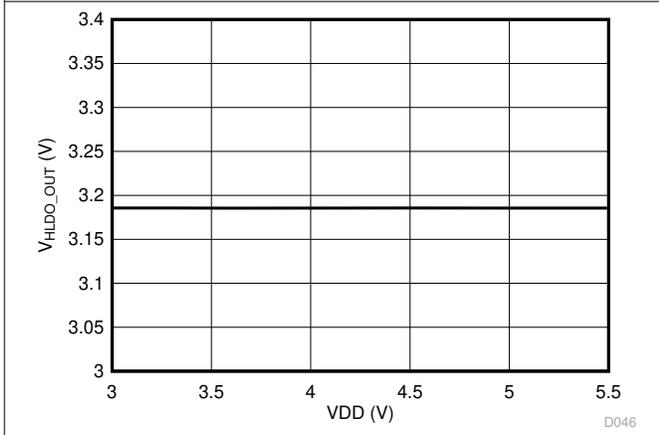


图 6-37. High-Side LDO Line Regulation

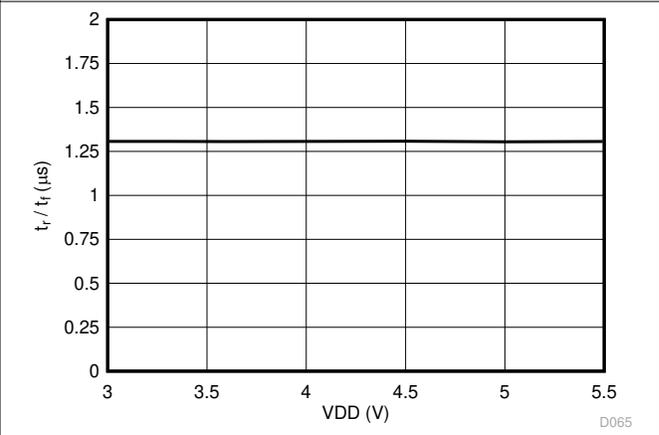


图 6-38. Output Rise and Fall time vs Supply Voltage

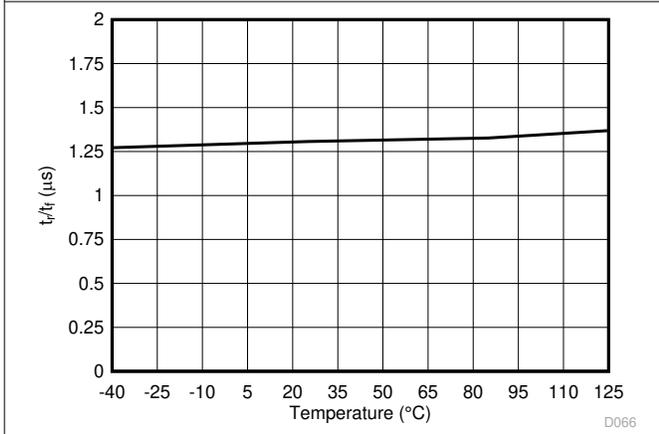


图 6-39. Output Rise and Fall Time vs Temperature

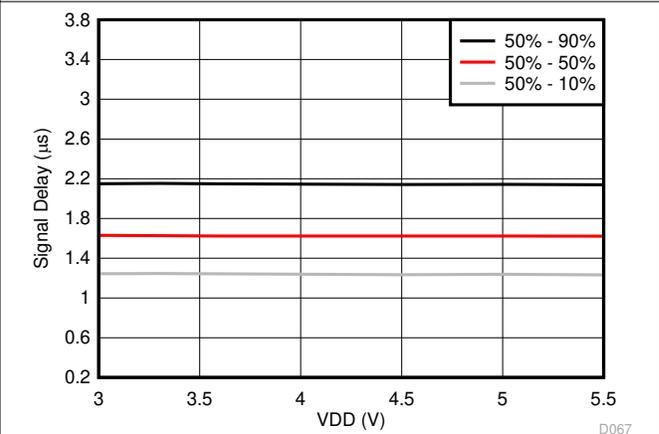


图 6-40. V_{IN} to V_{OUT} Signal Delay vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = - 50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

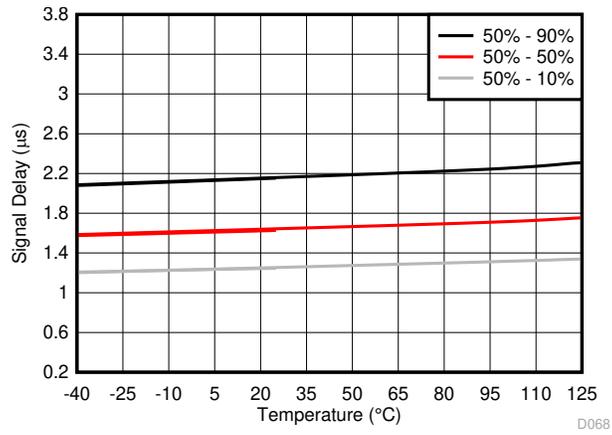


图 6-41. V_{IN} to V_{OUT} Signal Delay vs Temperature

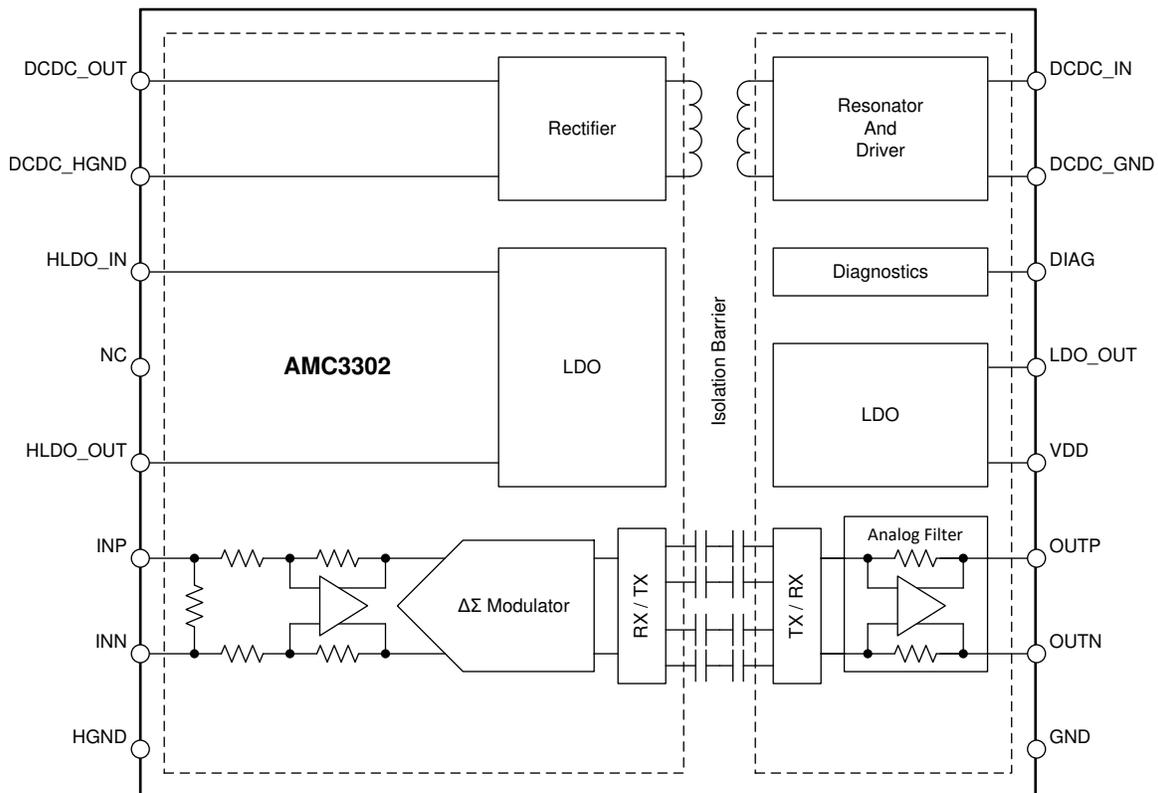
7 Detailed Description

7.1 Overview

The AMC3302 is a fully differential, precision, isolated amplifier with an integrated DC/DC converter that can supply the device from a single 3.3-V or 5-V voltage supply on the low-side. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the highside from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUP and OUTN pins that is proportional to the input signal.

The signal path is isolated by a double capacitive silicon dioxide (SiO_2) insulation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC3302 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND} . The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the [Data Isolation Channel Signal Transmission](#) section.

There are two restrictions on the analog input signals (INP and INN). First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the [Absolute Maximum Ratings](#) table, the input current must be limited to the absolute maximum value, because the device input electrostatic discharge (ESD) diodes turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the [Recommended Operating Conditions](#) table.

7.3.2 Data Isolation Channel Signal Transmission

The AMC3302 uses an on-off keying (OOK) modulation scheme, as shown in [图 7-1](#), to transmit the modulator output bitstream across the capacitive SiO₂-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC3302 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and produces the output. The AMC3302 transmission (TX) channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

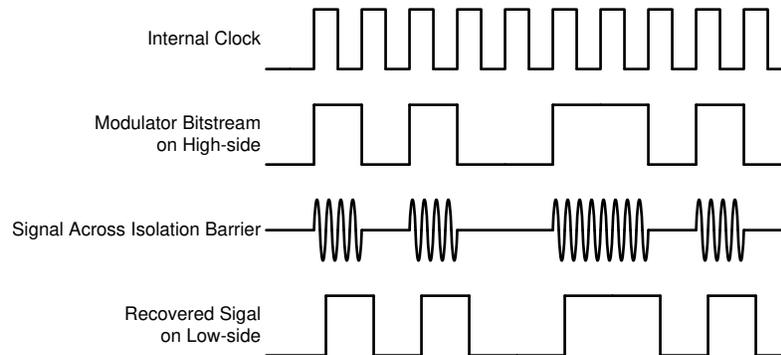


图 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC3302 offers a differential analog output comprised of the OOUTP and OOUTN pins. For differential input voltages ($V_{INP} - V_{INN}$) in the range from -50 mV to 50 mV, the device provides a linear response with a nominal gain of 41. For example, for a differential input voltage of 50 mV, the differential output voltage ($V_{OOUTP} - V_{OOUTN}$) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage V_{CMout} , as specified in the [Electrical Characteristics](#) table. For absolute differential input voltages greater than 50 mV but less than 64 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in [Figure 7-2](#), if the differential input voltage exceeds the $V_{Clipping}$ value.

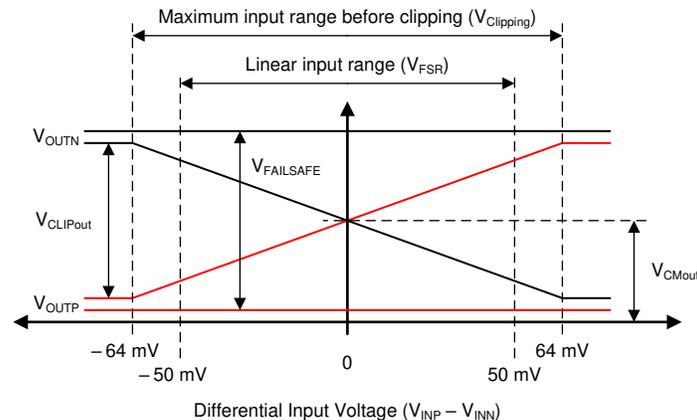


图 7-2. Output Behavior of the AMC3302

The AMC3302 provides a failsafe output that simplifies diagnostics on system level. [Figure 7-2](#) shows the failsafe mode, in which the AMC3302 outputs a negative differential output voltage that does not occur under normal operating conditions. The failsafe output is active in two cases:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high side)
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out)

Use the maximum $V_{FAILSAFE}$ voltage specified in the [Electrical Characteristics](#) table as a reference value for the failsafe detection on the system level.

7.3.4 Isolated DC/DC Converter

The AMC3302 offers a fully integrated isolated DC/DC converter that includes following components illustrated in the [Functional Block Diagram](#):

- Low-dropout regulator (LDO) on the low-side side to stabilize the supply voltage V_{DD} that drives the low-side of the converter
- Low-side full-bridge inverter and drivers
- Laminate-based, air-core transformer for high immunity to magnetic fields
- High-side full-bridge rectifier
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronized to the operation of the $\Delta\Sigma$ modulator to minimize the interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3302 and can source up to I_H of additional DC current for an optional auxiliary circuit such as an active filter, pre-amplifier, or comparator. I_H is specified in the [Electrical Characteristics](#) table as a DC, non-switching current.

7.3.5 Diagnostic Output

As shown in [图 7-3](#), the open-drain DIAG pin can be monitored to confirm the device is operational and the output voltage is valid. During power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the device operates properly. During normal operation, the DIAG pin is in high-impedance (Hi-Z) state and is pulled high through an external pullup resistor. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high side). In this case, the amplifier outputs are driven to the V_{FAILSAFE} value, see [图 7-2](#).
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out). In this case, the low-side may still receive data from the high-side but the data may not be valid. The amplifier outputs are driven to V_{FAILSAFE} value, see [图 7-2](#).

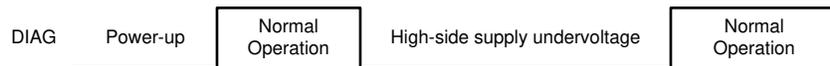


图 7-3. DIAG Output Under Different Operating Conditions

During normal operation, the DIAG pin is in a high-impedance state. Connect the DIAG pin to a pullup resistor or leave open if not used.

7.4 Device Functional Modes

The AMC3302 is operational when the power supply VDD is applied, as specified in the [Recommended Operating Conditions](#) table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the AMC3302 a high-performance solution for industrial applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

8.2 Typical Application

The AMC3302 is ideally suited for shunt-based, current-sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC3302 integrates an isolated power supply for the high-voltage side and therefore makes the device particularly easy to use in applications that do not have a high-side supply readily available or where a high-side supply is referenced to a different ground potential than the signal to be measured.

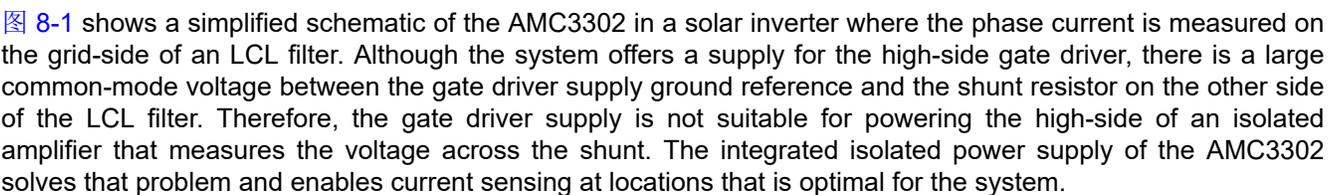
 Figure 8-1 shows a simplified schematic of the AMC3302 in a solar inverter where the phase current is measured on the grid-side of an LCL filter. Although the system offers a supply for the high-side gate driver, there is a large common-mode voltage between the gate driver supply ground reference and the shunt resistor on the other side of the LCL filter. Therefore, the gate driver supply is not suitable for powering the high-side of an isolated amplifier that measures the voltage across the shunt. The integrated isolated power supply of the AMC3302 solves that problem and enables current sensing at locations that is optimal for the system.

 Figure 8-1 also shows the AMC3330 being used for sensing the AC output voltage.

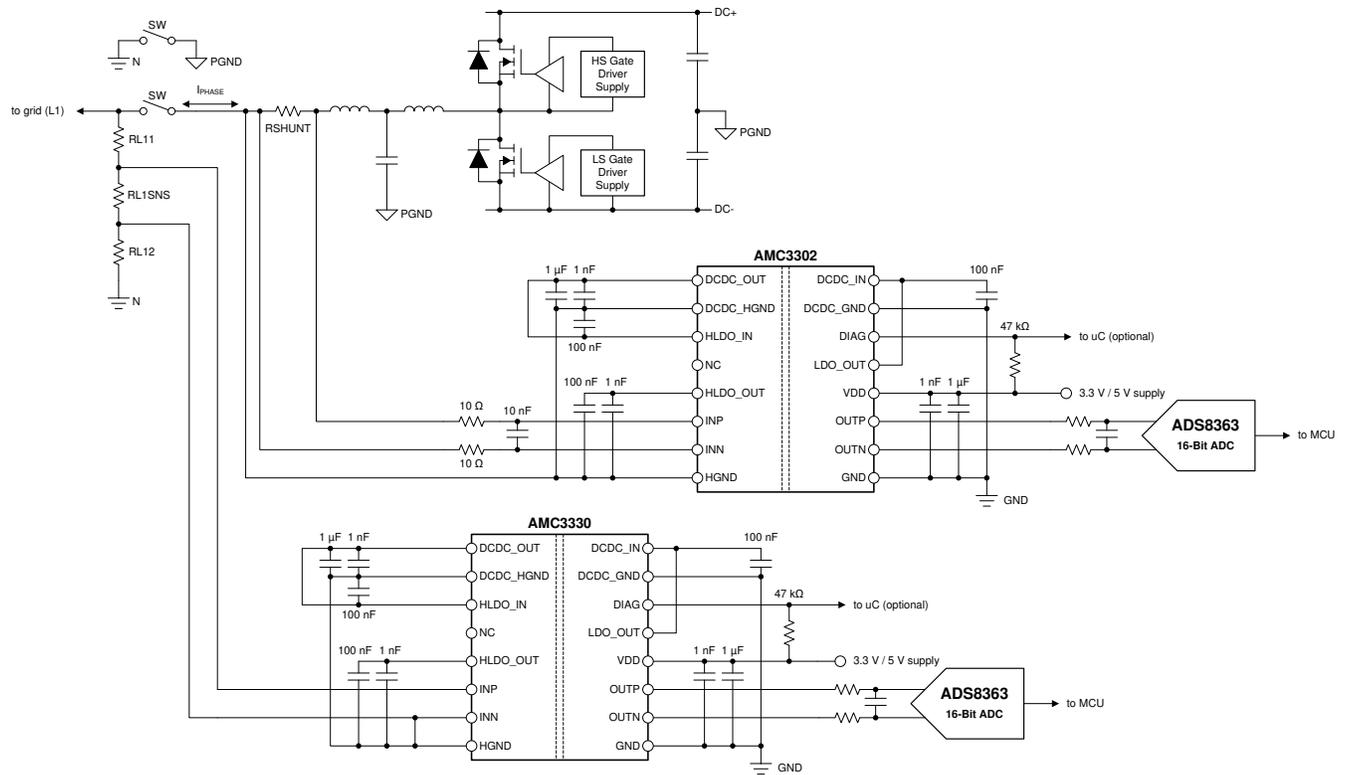


图 8-1. The AMC3302 in a Solar Inverter Application

8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	VALUE
Supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response (V_{SHUNT})	± 50 mV (maximum)

8.2.2 Detailed Design Procedure

The AMC3302 requires a single 3.3-V or 5-V supply on its low side. The high-side supply is internally generated by an integrated DC/DC converter, as explained in the [Isolated DC/DC Converter](#) section.

The ground reference (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input (INN) of the AMC3302. If a four-pin shunt is used, the inputs of the device are connected to the inner leads and HGND is connected to one of the outer leads. To minimize offset and improve accuracy, set the ground connection to a separate trace that connects directly to the shunt resistor rather than shorting HGND to INN directly at the input to the device. See the [Layout](#) section for more details.

8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor, R_{SHUNT} :

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

8.2.2.2 Input Filter Design

TI recommends placing an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the $\Delta \Sigma$ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications the structure shown in 图 8-2 achieves excellent performance.

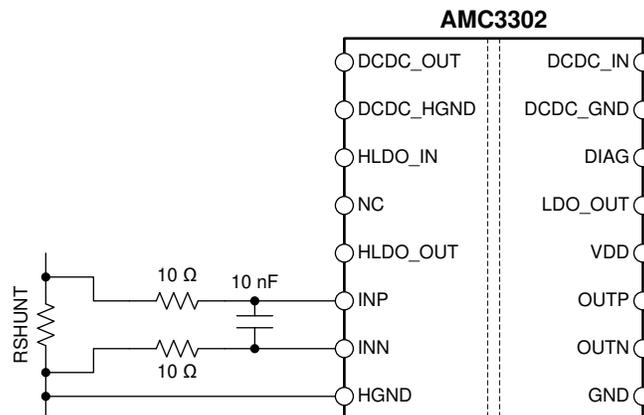


图 8-2. Differential Input Filter

8.2.2.3 Differential to Single-Ended Output Conversion

图 8-3 shows an example of a TLV6001-based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With $R1 = R2 = R3 = R4$, the output voltage equals $(V_{OUTP} - V_{OUTN}) + V_{REF}$. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications, $R1 = R2 = R3 = R4 = 3.3\text{ k}\Omega$ and $C1 = C2 = 330\text{ pF}$ yields good performance.

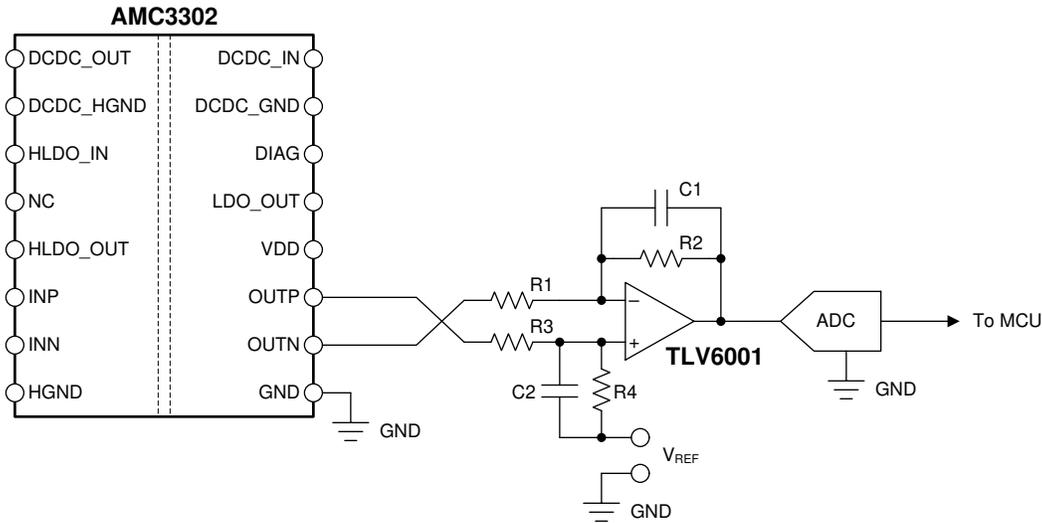


图 8-3. Connecting the AMC3302 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of successive-approximation-register (SAR) ADCs, see the [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise reference guide](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power reference guide](#), available for download at www.ti.com.

8.2.3 Application Curve

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. 图 8-4 shows the typical fullscale step response of the AMC3302.

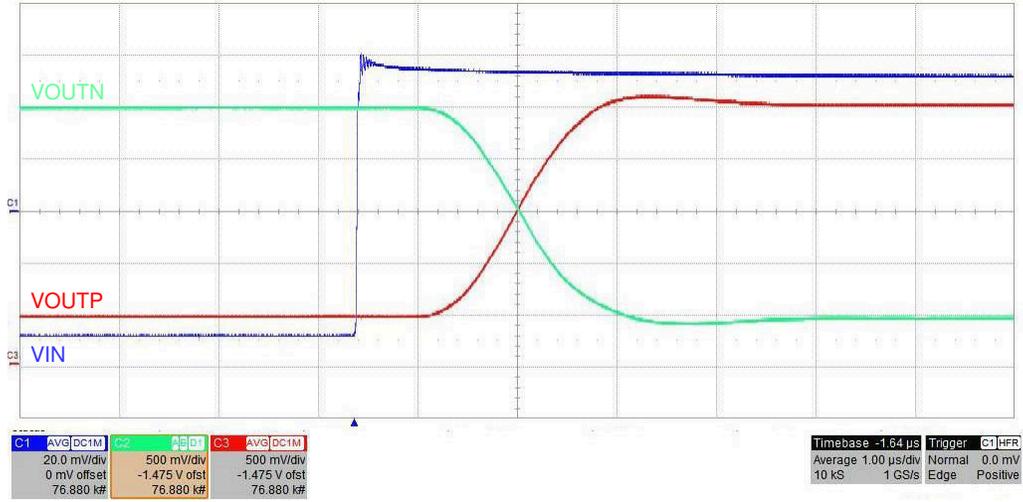


图 8-4. Step Response of the AMC3302

8.3 What to Do and What Not to Do

Do not leave the analog inputs INP and INN of the AMC3302 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage, leaving the output of the device undetermined.

Connect the negative input (INN) to the high-side ground (HGND), either by a hard short or through a resistive path. A DC current path between INN and HGND is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the [Recommended Operating Conditions](#) table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the [Layout](#) section for more details.

9 Power Supply Recommendations

The AMC3302 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V or 5 V. TI recommends a low-ESR decoupling capacitor of 1 nF (C8 in 图 9-1) placed as close as possible to the VDD pin, followed by a 1- μ F capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR 100-nF capacitor (C4) positioned close to the device between the DCDC_IN and DCDC_GND pins. Use a 1- μ F capacitor (C2) to decouple the high-side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC_OUT and DCDC_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3302, followed by a 100-nF decoupling capacitor (C5).

The ground reference for the high-side (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting HGND to INN directly at the device input. The high-side DC/DC ground terminal (DCDC_HGND) is shorted to HGND directly at the device pins.

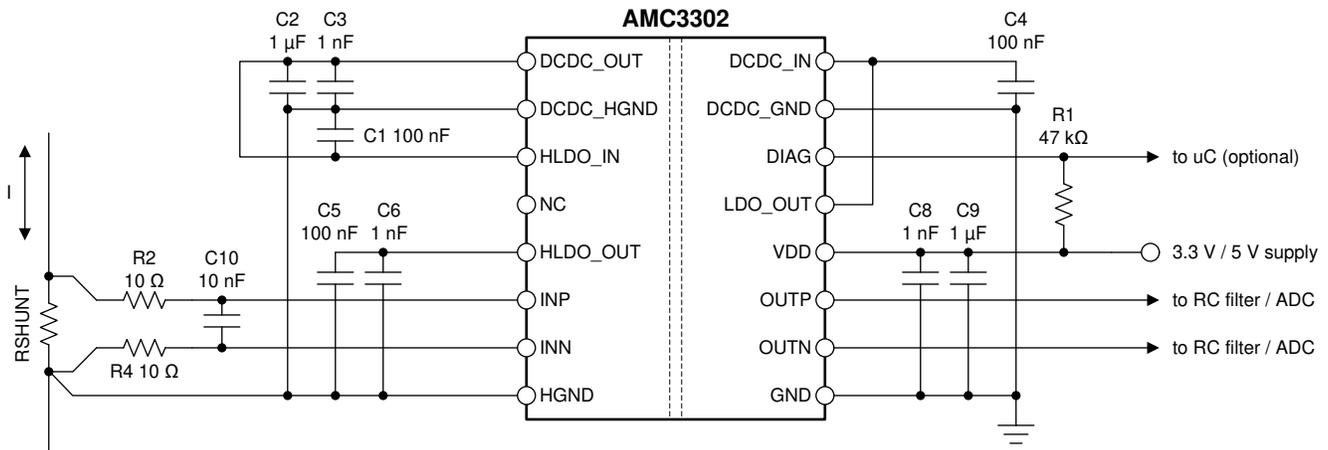


图 9-1. Decoupling the AMC3302

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

表 9-1 lists components suitable for use with the AMC3302. This list is not exhaustive. Other components may exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3302.

表 9-1. Recommended External Components

DESCRIPTION	PART NUMBER	MANUFACTURER	SIZE (EIA, L x W)	
VDD				
C8	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
C9	1 μF ± 10%, X7R, 25 V	12063C105KAT2A	AVX	1206, 3.2 mm x 1.6 mm
DC/DC CONVERTER				
C4	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C3	1 nF ± 10%, X7R, 50 V	C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
C2	1 μF ± 10%, X7R, 25 V	CGA3E1X7R1E105K080AC	TDK	0603, 1.6 mm x 0.8 mm
HLDO				
C1	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C5	100 nF ± 5%, NP0, 50 V	C3216NP01H104J160AA	TDK	1206, 3.2 mm x 1.6 mm
C6	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm

10 Layout

10.1 Layout Guidelines

图 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC3302 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC3302 and keep the layout of both connections symmetrical.

To avoid errors in the measurement caused by the input bias currents of the AMC3302, connect the high-side ground pin (HGND) to the IIN-side of the shunt resistor. Use a separate trace in the layout to make this connection to maintain equal currents in the IIN and INP traces.

10.2 Layout Example

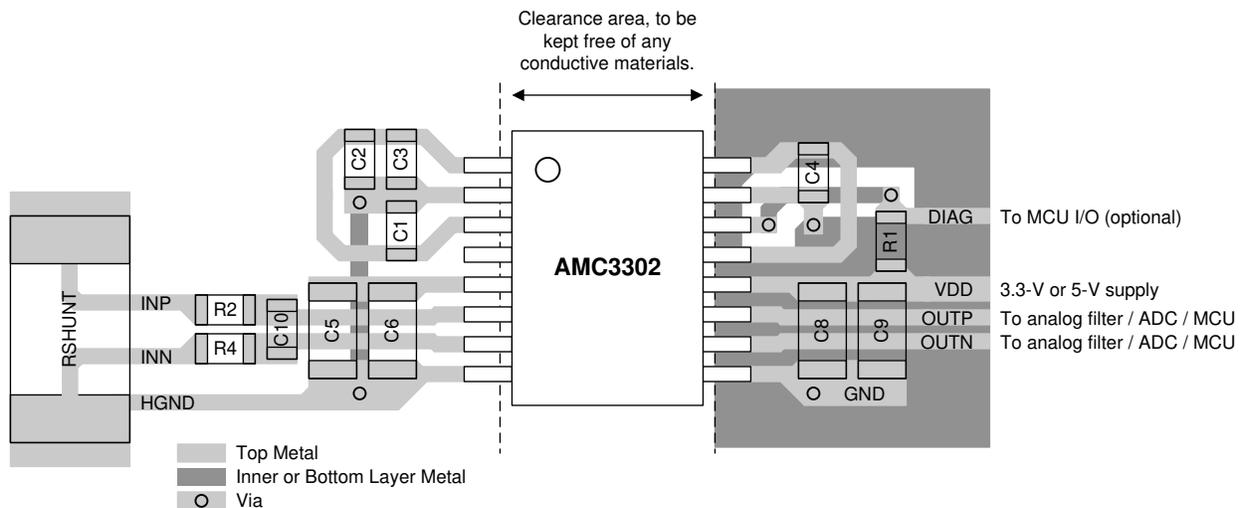


图 10-1. Recommended Layout of the AMC3302

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Texas Instruments, [Isolation Glossary](#)

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application report
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity](#) application report
- Texas Instruments, [AMC3330 Precision, ±1-V Input, Reinforced Isolated Amplifier](#) data sheet
- Texas Instruments, [TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#) data sheet
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) reference guide
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) reference guide
- Texas Instruments, [Isolated Amplifier Voltage Sensing Excel Calculator](#) design tool

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC3302DWE	ACTIVE	SOIC	DWE	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3302	Samples
AMC3302DWER	ACTIVE	SOIC	DWE	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3302	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

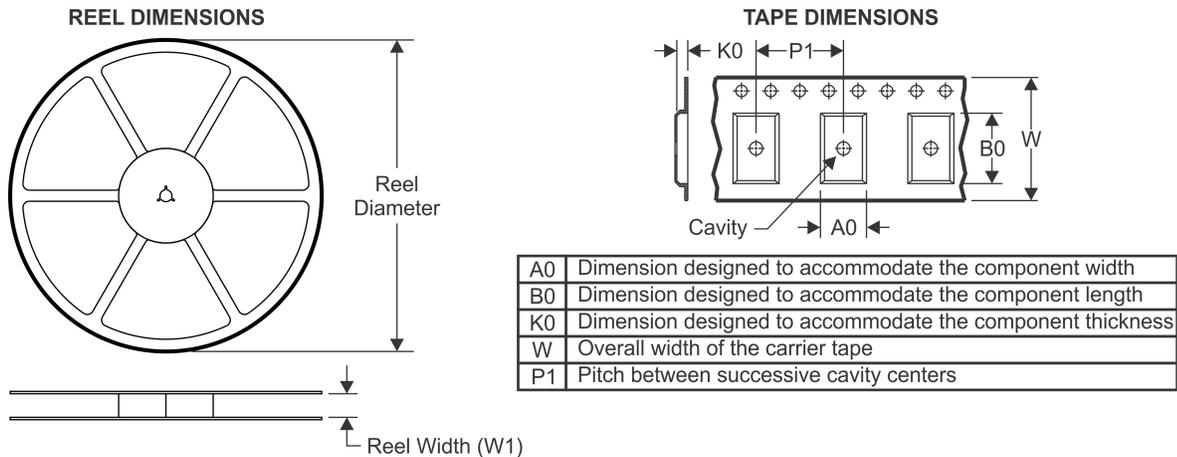
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

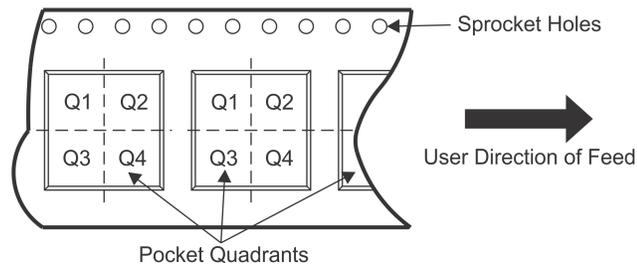
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TAPE AND REEL INFORMATION



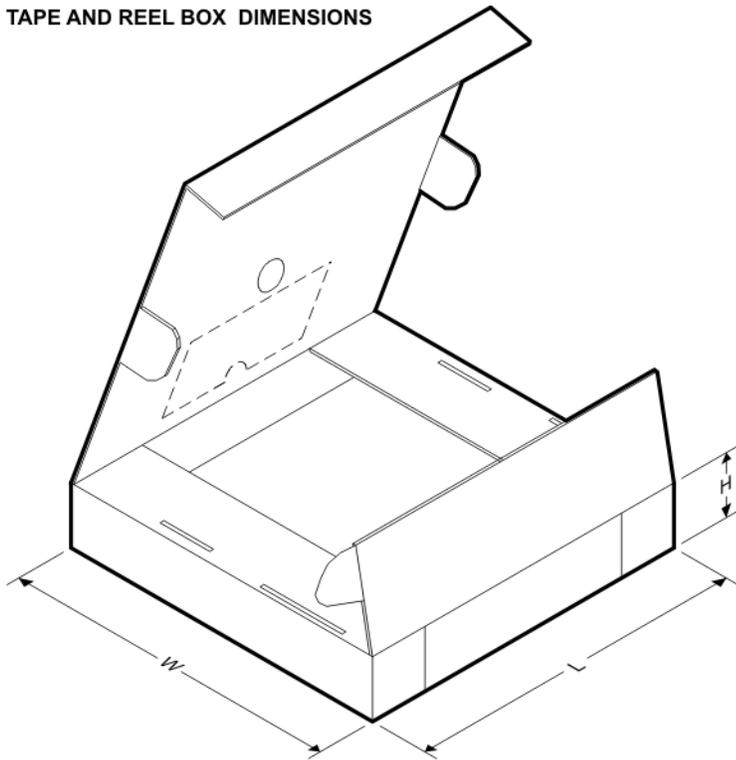
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC3302DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

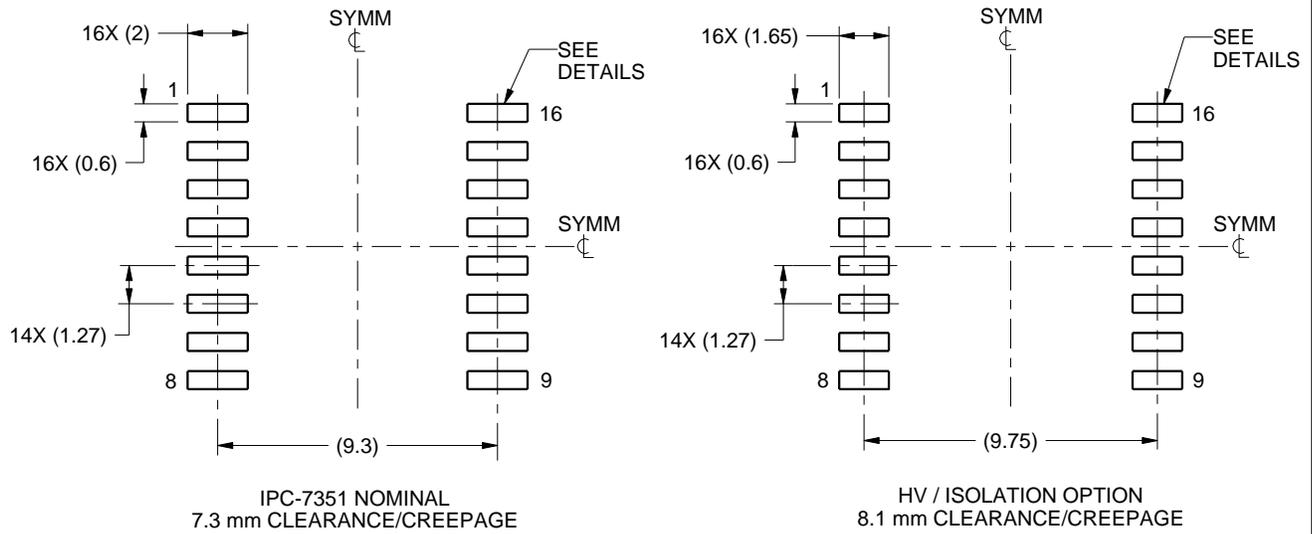
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC3302DWER	SOIC	DWE	16	2000	350.0	350.0	43.0

EXAMPLE BOARD LAYOUT

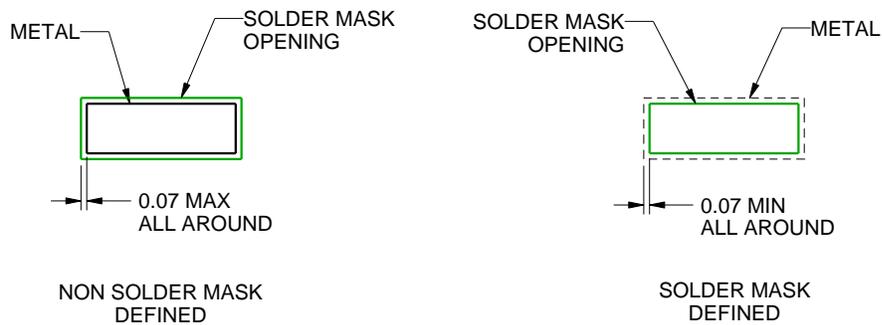
DWE0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4223098/A 07/2016

NOTES: (continued)

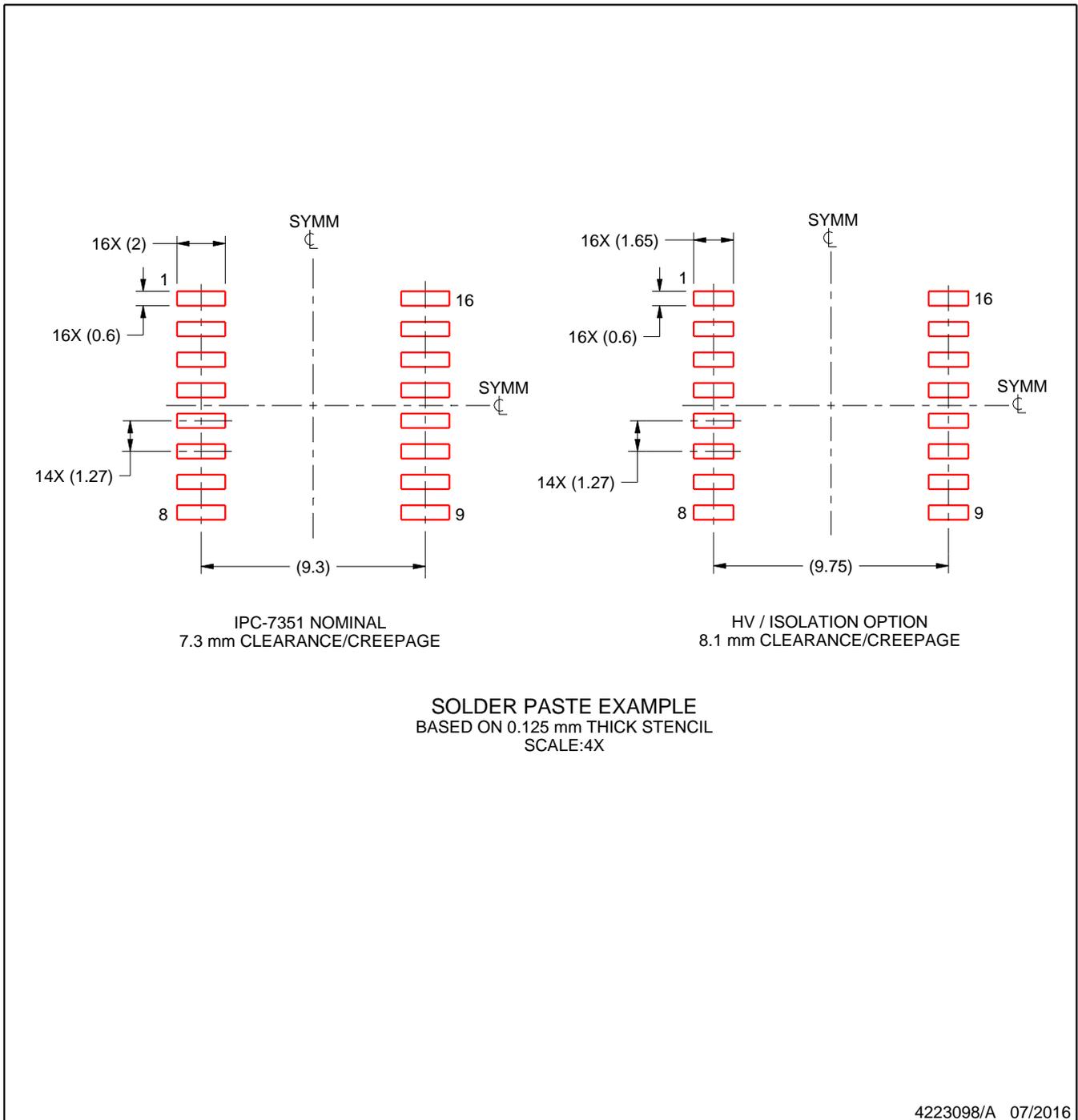
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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