ADVANCED INFORMATION

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D T_A = +25°C
20V	200mΩ @ V_{GS} = 4.5V	1.9A
	280mΩ @ V_{GS} = 2.5V	1.6A

Features and Benefits

- Low On-Resistance
- Very Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

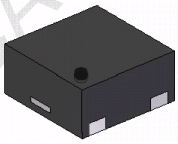
- Power Management Functions
- Battery Operated Systems and Solid-State Relays
- Load Switch

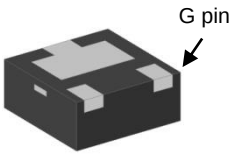
Mechanical Data

- Case: U-DFN1212-3
- Case Material: Molded Plastic; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208 e4
- Terminal Connections: See Diagram
- Weight: 0.005 grams (Approximate)

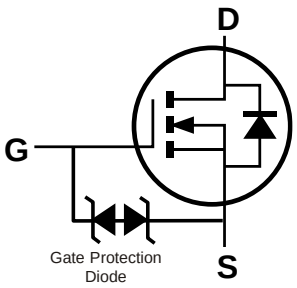
U-DFN1212-3 (Type C)


ESD PROTECTED

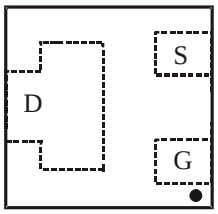

Top View



Bottom View



Equivalent Circuit



Pin-out Top View

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN2310UFD-7	U-DFN1212-3 (Type C)	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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Marking Information

Site 1

U-DFN1212-3 (Type C)

BE5 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: H = 2020)
M = Month (ex: 9 = September)

Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	H	I	J	K	L	M	N	O	P	R	S	T

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2

U-DFN1212-3 (Type C)

BE5 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 0 = 2020)
W = Week (ex: a = week 27; z represents week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	0	1	2	3	4	5	6	7	8	9	0	1

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	±8	V
Continuous Drain Current (Note 6) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	1.9 1.5	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	4.7	A
Maximum Body Diode Forward Current (Note 6)			I_S	1.2	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	0.67	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	187	°C/W
Total Power Dissipation (Note 6)		P_D	1.1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	114	°C/W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	120	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1.0	µA	V_{DS} = 20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.45	—	0.95	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	150	200	mΩ	V_{GS} = 4.5V, I_D = 1A
		—	190	280		V_{GS} = 2.5V, I_D = 750mA
		—	250	380		V_{GS} = 1.8V, I_D = 500mA
		—	320	500		V_{GS} = 1.5V, I_D = 250mA
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 500mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	38	—	pF	V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	10	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	6	—	pF	
Total Gate Charge	Q_g	—	0.7	—	nC	V_{GS} = 4.5V, V_{DS} = 10V, I_D = 1A
Gate-Source Charge	Q_{gs}	—	0.1	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	5.5	—	ns	V_{DD} = 10V, V_{GS} = 5V, R_L = 1.7Ω, R_G = 6Ω
Turn-On Rise Time	t_R	—	2.7	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	183	—	ns	
Turn-Off Fall Time	t_F	—	49	—	ns	

Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1-inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

ADVANCED INFORMATION

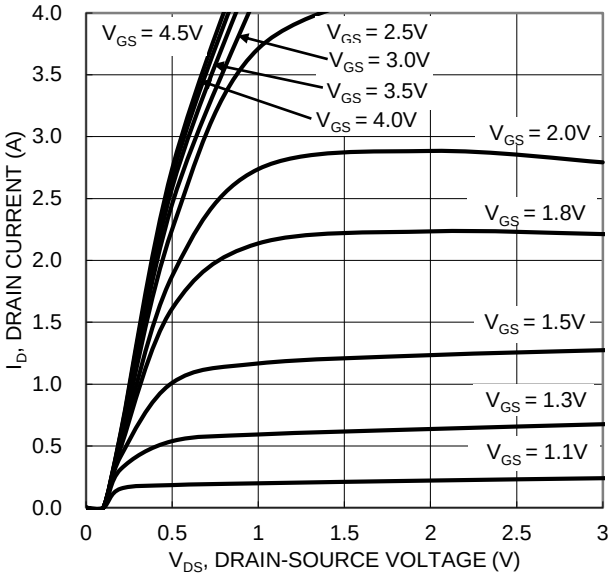

Figure 1. Typical Output Characteristic

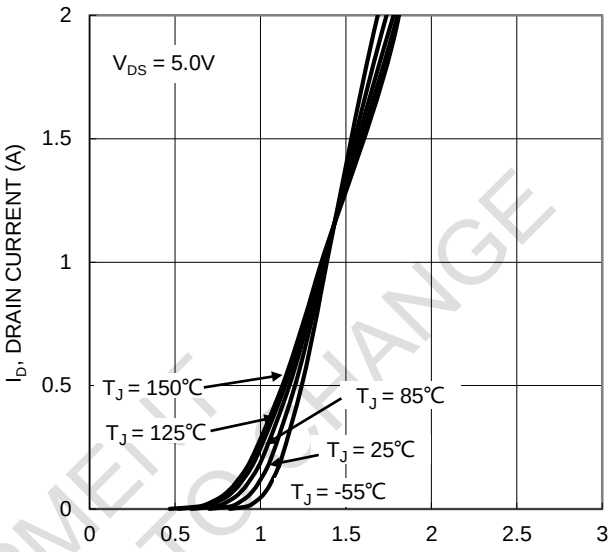

Figure 2. Typical Transfer Characteristic

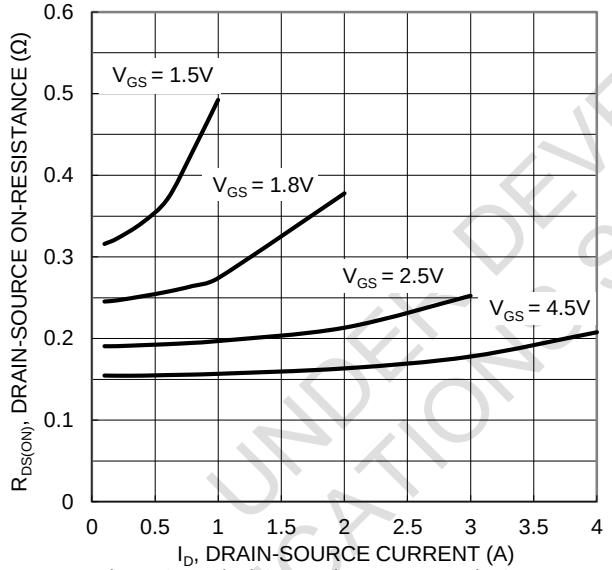

Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

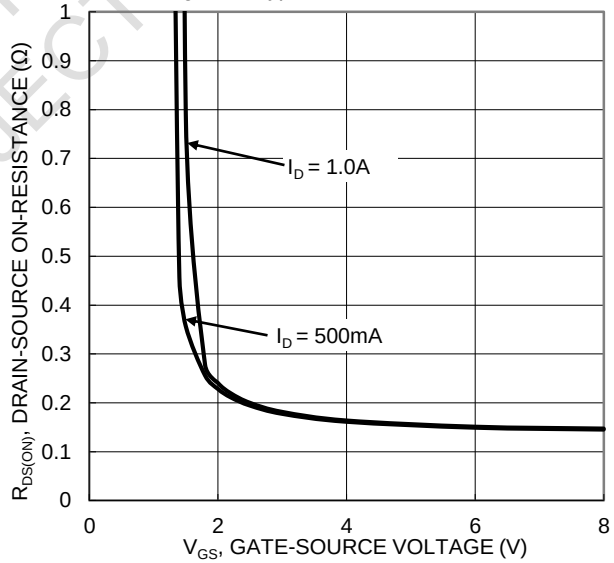

Figure 4. Typical Transfer Characteristic

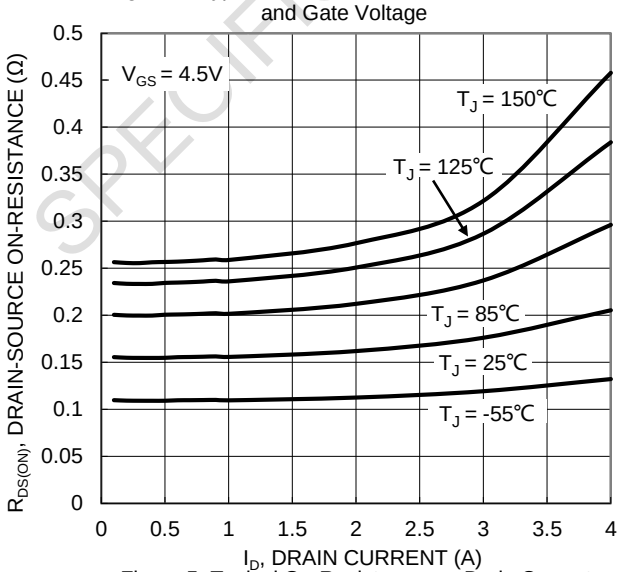

Figure 5. Typical On-Resistance vs. Drain Current and Temperature

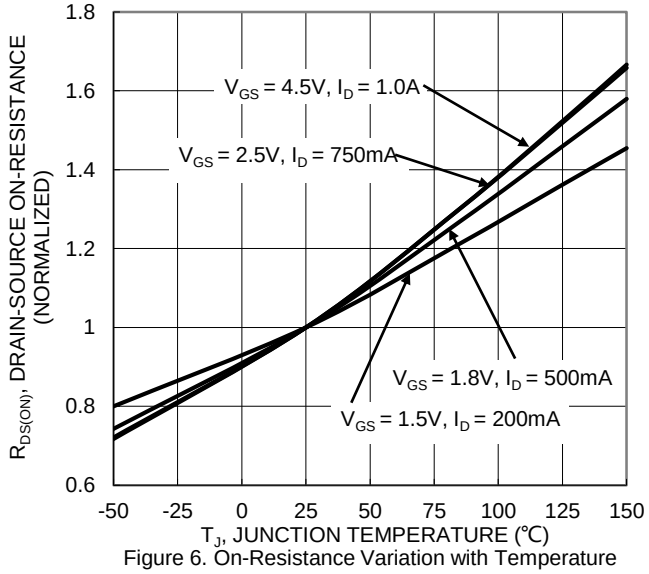

Figure 6. On-Resistance Variation with Temperature

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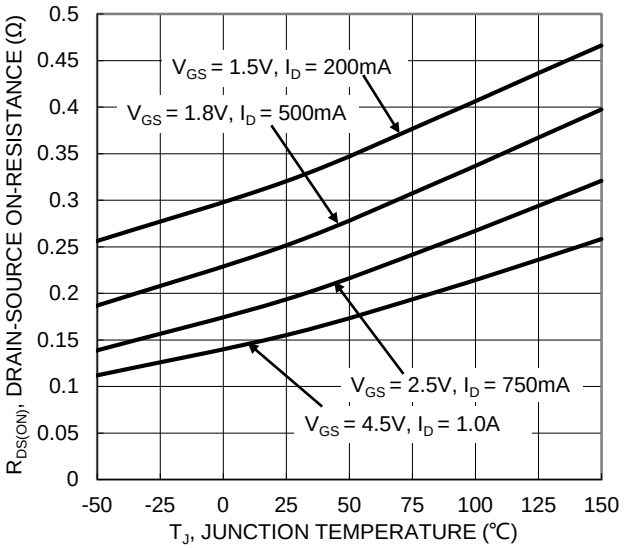

Figure 7. On-Resistance Variation with Temperature

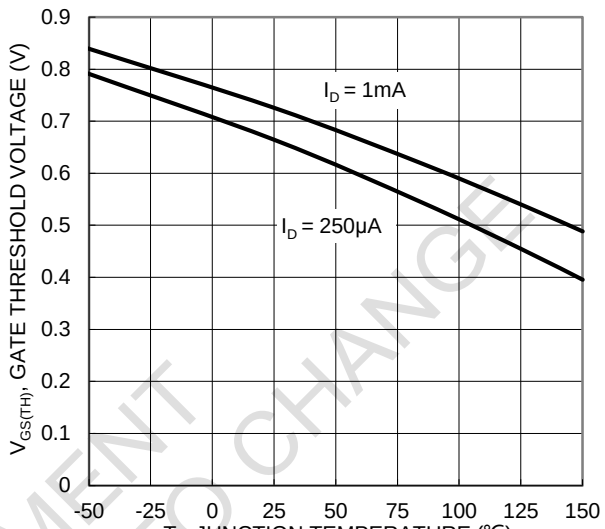

Figure 8. Gate Threshold Variation vs. Junction Temperature

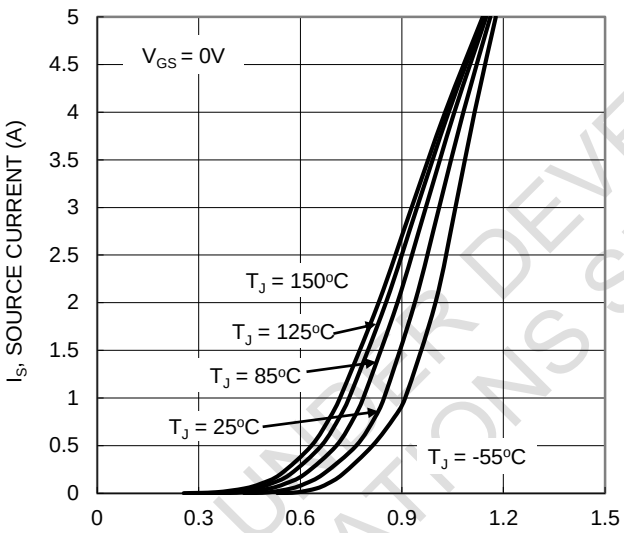

Figure 9. Diode Forward Voltage vs. Current

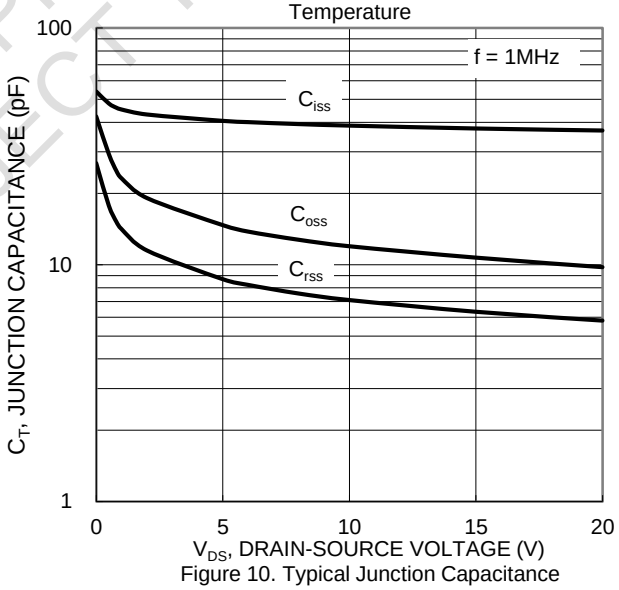

Figure 10. Typical Junction Capacitance

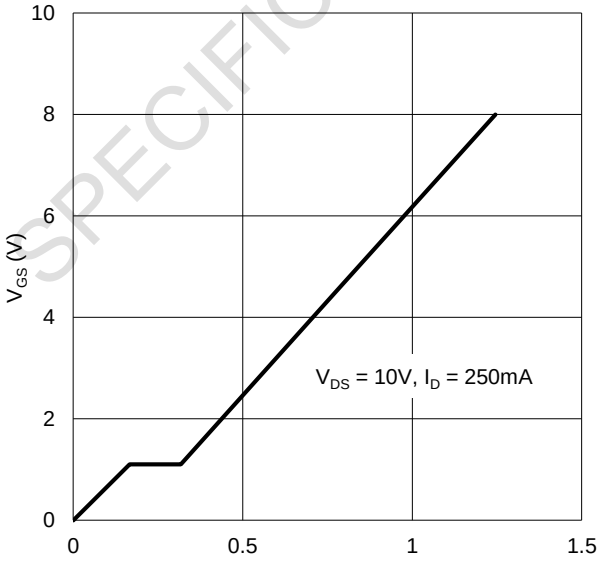

Figure 11. Gate Charge

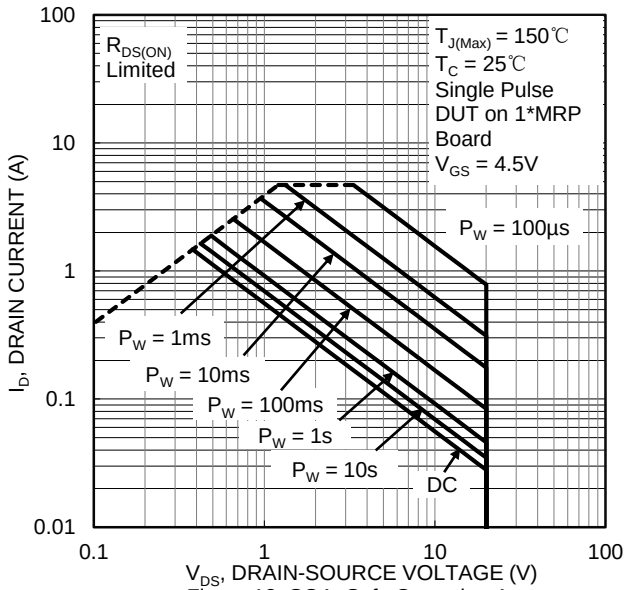

Figure 12. SOA, Safe Operation Area

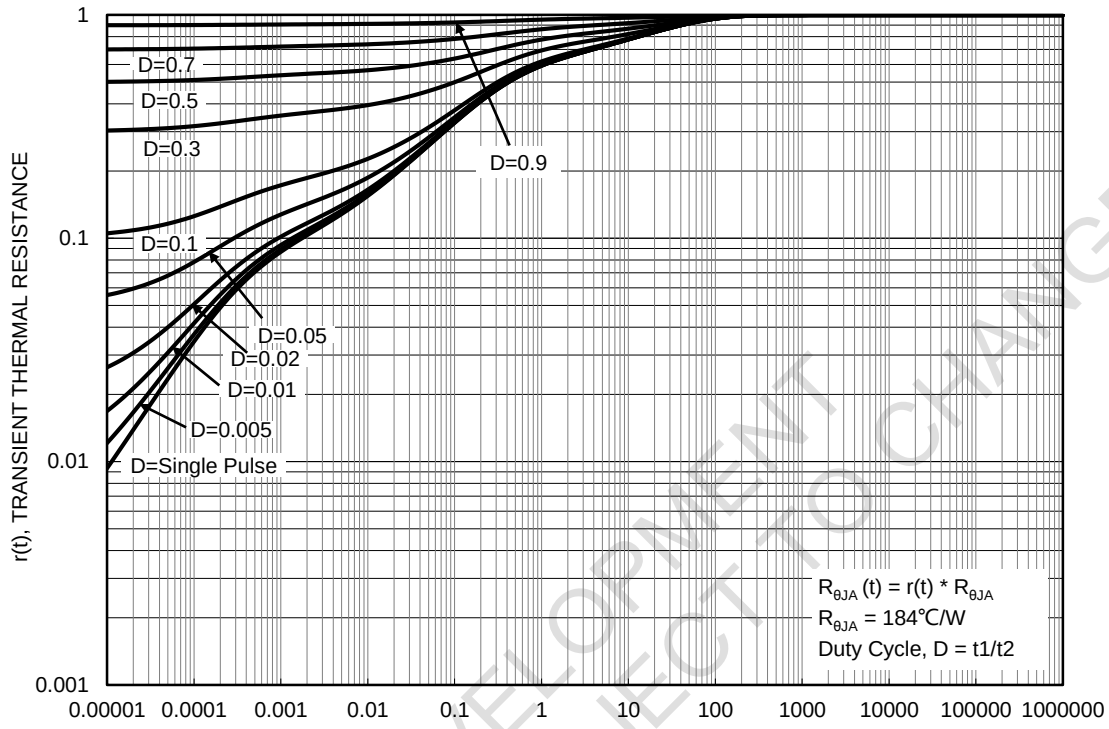

Figure 13. Transient Thermal Resistance

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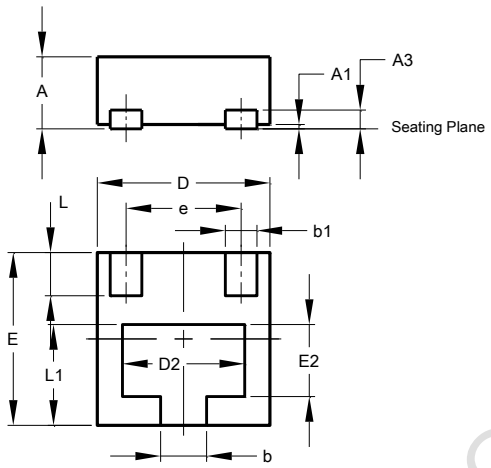
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN1212-3 (Type C)

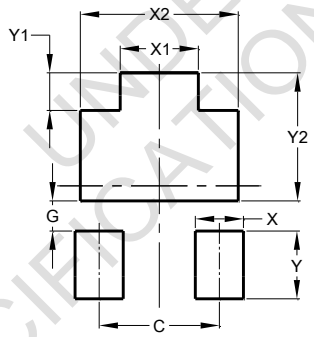


U-DFN1212-3 (Type C)			
Dim	**Min**	**Max**	**Typ**
A	0.47	0.53	0.50
A1	0	0.05	0.02
A3	-	-	0.13
b	0.27	0.37	0.32
b1	0.17	0.27	0.22
D	1.15	1.25	1.20
D2	0.75	0.95	0.85
e	-	-	0.80
E	1.15	1.25	1.20
E2	0.40	0.60	0.50
L	0.25	0.35	0.30
L1	0.65	0.75	0.70
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN1212-3 (Type C)



Dimensions	Value (in mm)
C	0.800
G	0.200
X	0.320
X1	0.520
X2	1.050
Y	0.450
Y1	0.250
Y2	0.850

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