

SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

SDLS113 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

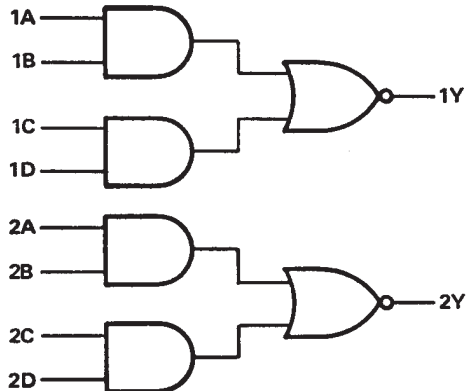
The '51 and 'S51 contain two independent 2-wide 2-input AND-OR-INVERT gates. They perform the Boolean function $Y = \overline{AB + CD}$.

The 'LS51 contains one 2-wide 3-input and one 2-wide 2-input AND-OR-INVERT gates. They perform the Boolean functions $1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$ and $2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$.

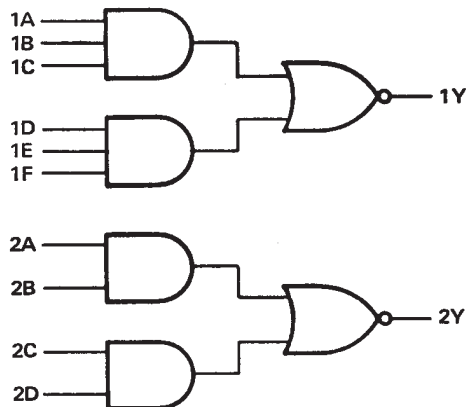
The SN5451, SN54LS51, and SN54S51 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7451, SN74LS51 and SN74S51 are characterized for operation from 0°C to 70°C .

logic diagrams

'51, 'S51

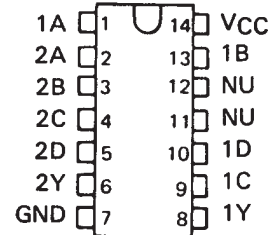


'LS51



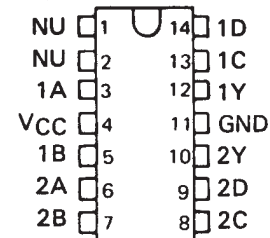
SN5451 . . . J PACKAGE
SN54S51 . . . J OR W PACKAGE
SN7451 . . . N PACKAGE
SN74S51 . . . D OR N PACKAGE

(TOP VIEW)



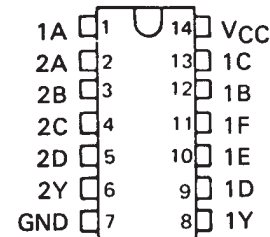
SN5451 . . . W PACKAGE

(TOP VIEW)



SN54LS51 . . . J OR W PACKAGE
SN74LS51 . . . D OR N PACKAGE

(TOP VIEW)



NC - No internal connection

NU - Make no external connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

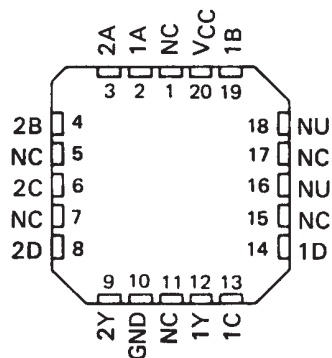
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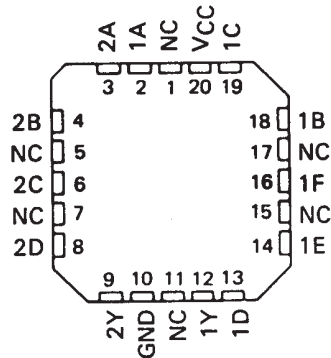
SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

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SN54S51 . . . FK PACKAGE
(TOP VIEW)

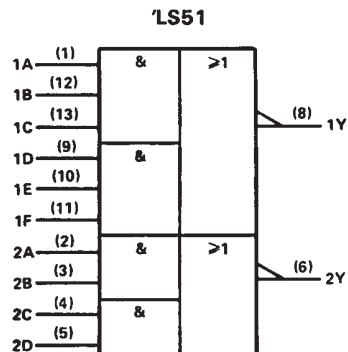
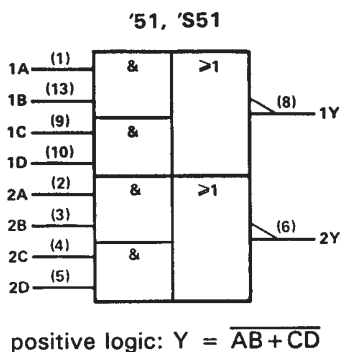


SN54LS51 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection
NU - Make no external connection

logic symbols†



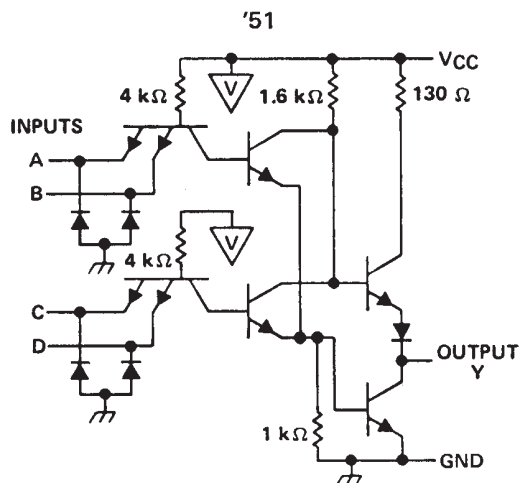
positive logic:

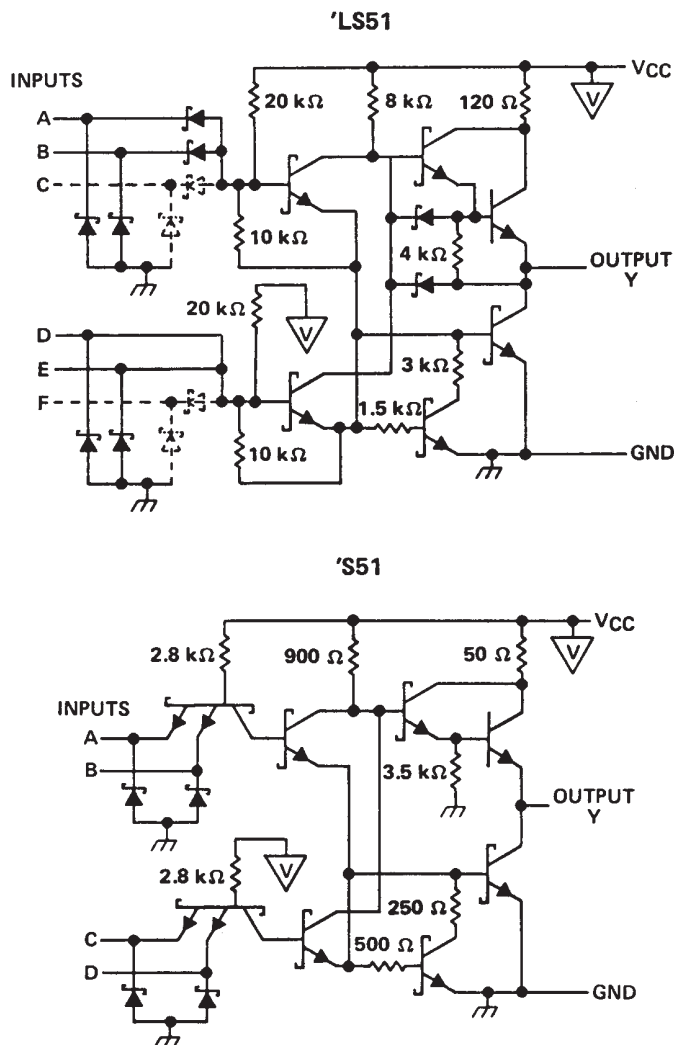
$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

$$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$$

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

schematics





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (See Note 1): '51, 'LS51, 'S51 | 7 V |
| Input voltage: '51, 'S51 | 5.5 V |
| 'LS51 | 7 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

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recommended operating conditions

| | SN5451 | | | SN7451 | | | UNIT |
|---|--------|-----|-------|--------|-----|-------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} High-level output current | | | − 0.4 | | | − 0.4 | mA |
| I _{OL} Low-level output current | | | 16 | | | 16 | mA |
| T _A Operating free-air temperature | − 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS † | SN5451 | | | SN7451 | | | UNIT |
|-------------------|--|--------|-------|-------|--------|-------|-------|------|
| | | MIN | TYP ‡ | MAX | MIN | TYP ‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = − 12 mA | | | − 1.5 | | | − 1.5 | V |
| V _{OH} | V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = − 0.4 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I _I | V _{CC} = MAX, V _I = 5.5 V | | | 1 | | | 1 | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.4 V | | | 40 | | | 40 | μA |
| I _{IL} | V _{CC} = MAX, V _I = 0.4 V | | | − 1.6 | | | − 1.6 | mA |
| I _{OS} § | V _{CC} = MAX | − 20 | | − 55 | − 18 | | − 55 | mA |
| I _{CCH} | V _{CC} = MAX, V _I = 0 V | | 4 | 8 | | 4 | 8 | mA |
| I _{CCL} | V _{CC} = MAX, See Note 2 | | 7.4 | 14 | | 7.4 | 14 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|--|-----|-----|-----|------|
| t _{PLH} | Any | Y | R _L = 400 Ω, C _L = 15 pF | | 13 | 22 | ns |
| t _{PHL} | | | | | 8 | 15 | |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

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recommended operating conditions

| | SN54LS51 | | | SN74LS51 | | | UNIT |
|--------------------------------------|----------|-----|-------|----------|-----|-------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} High-level output current | | | – 0.4 | | | – 0.4 | mA |
| I_{OL} Low-level output current | | | 4 | | | 8 | mA |
| T_A Operating free-air temperature | – 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS † | SN54LS51 | | | SN74LS51 | | | UNIT |
|------------|--|----------|-------|-------|----------|-------|-------|------|
| | | MIN | TYP ‡ | MAX | MIN | TYP ‡ | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | | | – 1.5 | | | – 1.5 | V |
| V_{OH} | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V_{OL} | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$ | 0.25 | 0.4 | | 0.25 | 0.4 | | V |
| | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$ | | | | 0.35 | 0.5 | | |
| I_I | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$ | | | 0.1 | | | 0.1 | mA |
| I_{IH} | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | | | 20 | | | 20 | µA |
| I_{IL} | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | | | – 0.4 | | | – 0.4 | mA |
| $I_{OS} §$ | $V_{CC} = \text{MAX}$ | – 20 | | – 100 | – 20 | | – 100 | mA |
| I_{CCH} | $V_{CC} = \text{MAX}, V_I = 0 \text{ V}$ | | 0.8 | 1.6 | | 0.8 | 1.6 | mA |
| I_{CCL} | $V_{CC} = \text{MAX}, \text{ See Note 2}$ | | 1.4 | 2.8 | | 1.4 | 2.8 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------------|-------------|--|-----|------|-----|------|
| t_{PLH} | Any | Y | $R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$ | | 12 | 20 | ns |
| t_{PHL} | | | | | 12.5 | 20 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

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recommended operating conditions

| | SN54S51 | | | SN74S51 | | | UNIT |
|--------------------------------------|---------|-----|-----|---------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} High-level output current | | | – 1 | | | – 1 | mA |
| I_{OL} Low-level output current | | | 20 | | | 20 | mA |
| T_A Operating free-air temperature | – 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS † | SN54S51 | | | SN74S51 | | | UNIT |
|------------|---|---------|-------|-------|---------|-------|-------|------|
| | | MIN | TYP ‡ | MAX | MIN | TYP ‡ | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | | | – 1.2 | | | – 1.2 | V |
| V_{OH} | $V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V_{OL} | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$ | | | 0.5 | | | 0.5 | V |
| I_I | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| I_{IH} | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | | | 50 | | | 50 | µA |
| I_{IL} | $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$ | | | – 2 | | | – 2 | mA |
| $I_{OS} §$ | $V_{CC} = \text{MAX}$ | – 40 | | – 100 | – 40 | | – 100 | mA |
| I_{CCH} | $V_{CC} = \text{MAX}, V_I = 0 \text{ V}$ | | 8.2 | 17.8 | | 8.2 | 17.8 | mA |
| I_{CCL} | $V_{CC} = \text{MAX}, \text{ See Note 2}$ | | 13.6 | 22 | | 13.6 | 22 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------------|-------------|---|-----|-----|-----|------|
| t_{PLH} | Any | Y | $R_L = 280 \Omega, C_L = 15 \text{ pF}$ | | 3.5 | 5.5 | ns |
| t_{PHL} | | | | | 3.5 | 5.5 | ns |
| t_{PLH} | | | $R_L = 280 \Omega, C_L = 50 \text{ pF}$ | | 5 | | ns |
| t_{PHL} | | | | | 5.5 | | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/00502BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 00502BCA | Samples |
| JM38510/07401BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 07401BCA | Samples |
| JM38510/07401BDA | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 07401BDA | Samples |
| JM38510/30401BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 30401BCA | Samples |
| M38510/00502BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 00502BCA | Samples |
| M38510/07401BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 07401BCA | Samples |
| M38510/07401BDA | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 07401BDA | Samples |
| M38510/30401BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 30401BCA | Samples |
| SN5451J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN5451J | Samples |
| SN54LS51J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS51J | Samples |
| SN54S51J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54S51J | Samples |
| SN74LS51D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS51 | Samples |
| SN74LS51DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS51 | Samples |
| SN74LS51N | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS51N | Samples |
| SN74LS51NSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS51 | Samples |
| SN74S51D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S51 | Samples |
| SN74S51N | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S51N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SNJ5451J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ5451J | Samples |
| SNJ5451W | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ5451W | Samples |
| SNJ54LS51J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS51J | Samples |
| SNJ54LS51W | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS51W | Samples |
| SNJ54S51FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S 51FK | Samples |
| SNJ54S51J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S51J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS51, SN54S51, SN74LS51, SN74S51 :

- Catalog : [SN74LS51](#), [SN74S51](#)
- Military : [SN54LS51](#), [SN54S51](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS51DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS51NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



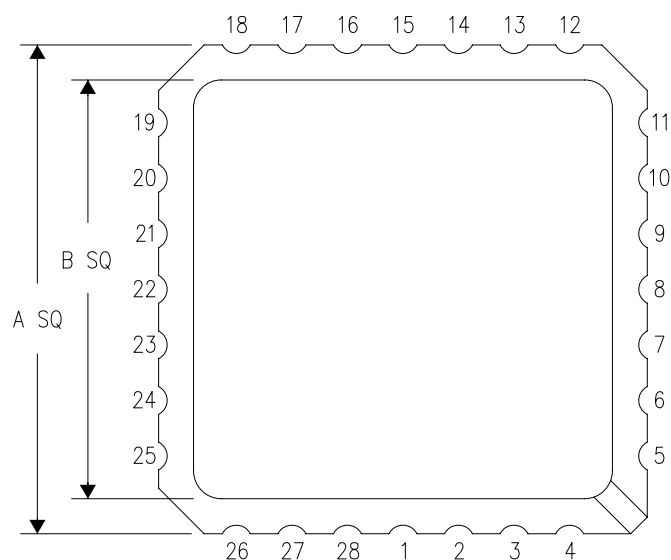
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS51DR | SOIC | D | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| SN74LS51NSR | SO | NS | 14 | 2000 | 853.0 | 449.0 | 35.0 |

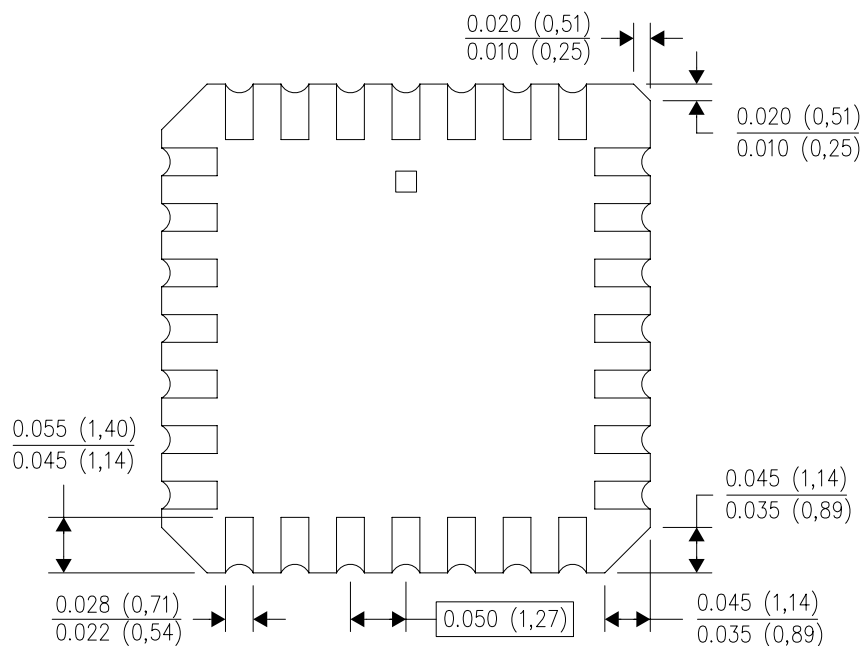
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



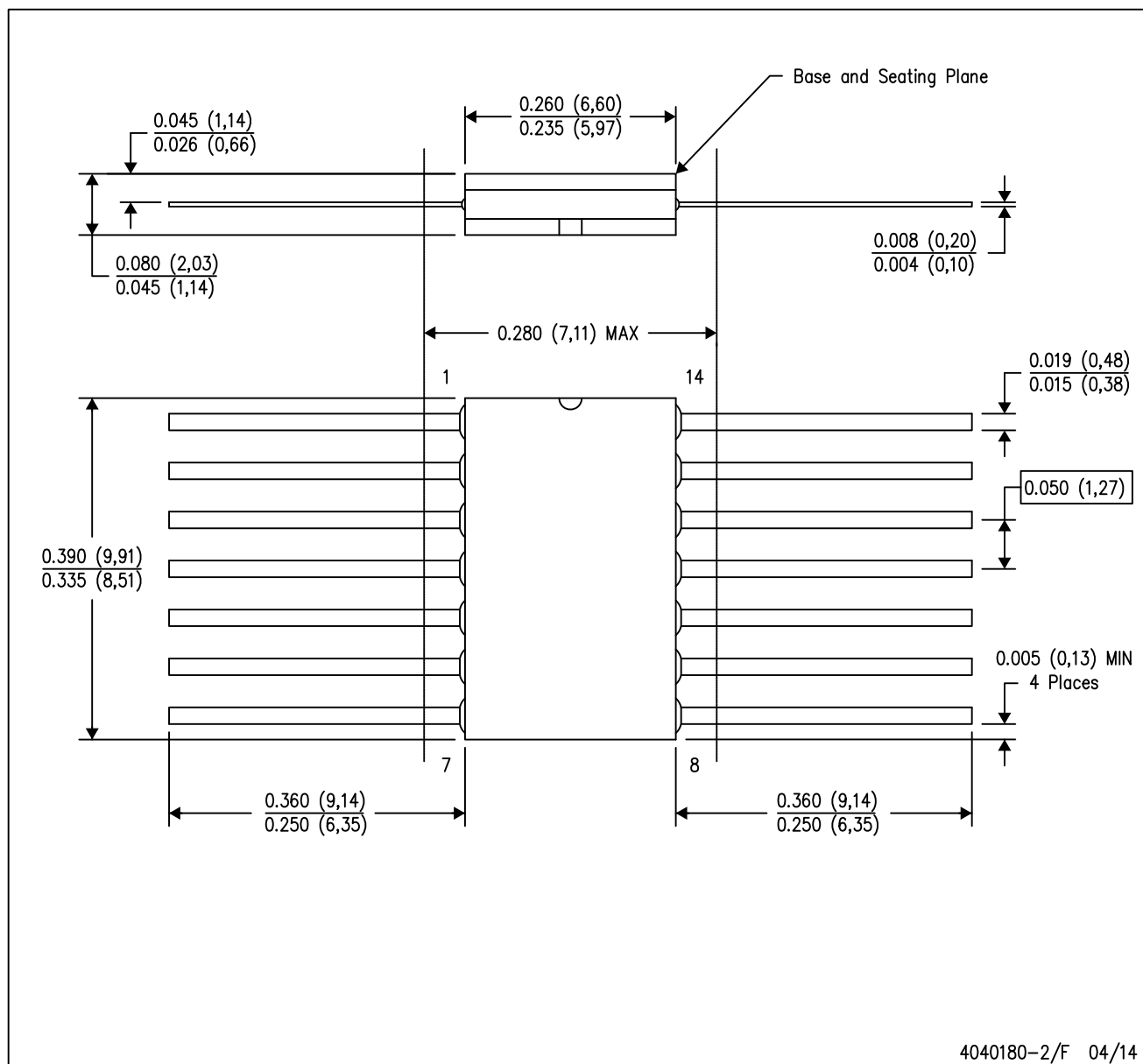
| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---------------|-------|-------|-------|-------|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

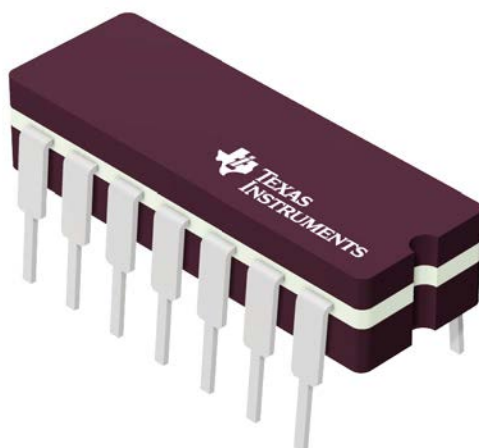
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL STD 1835 GDFP1-F14

J 14

GENERIC PACKAGE VIEW

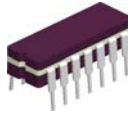
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

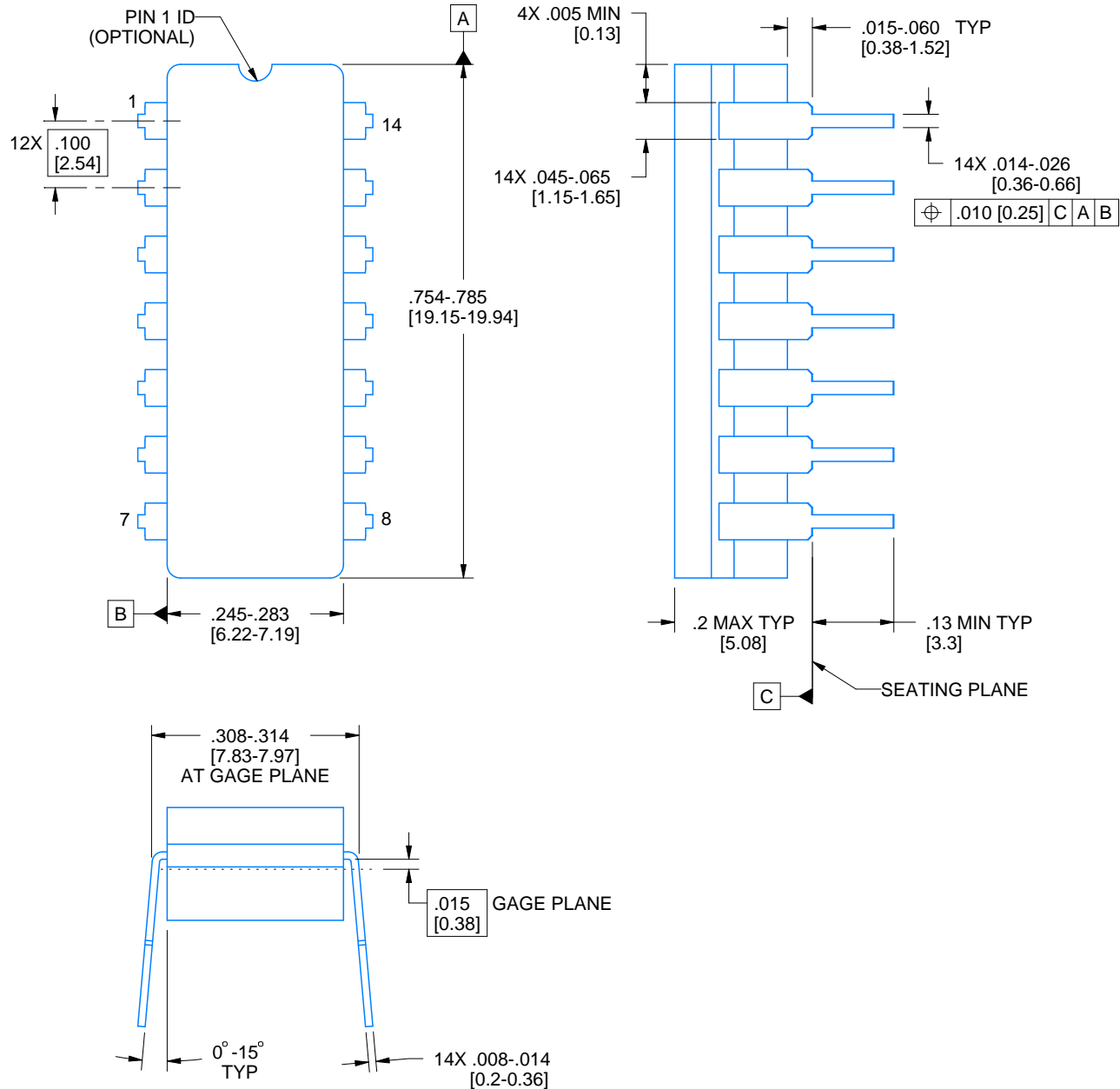


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



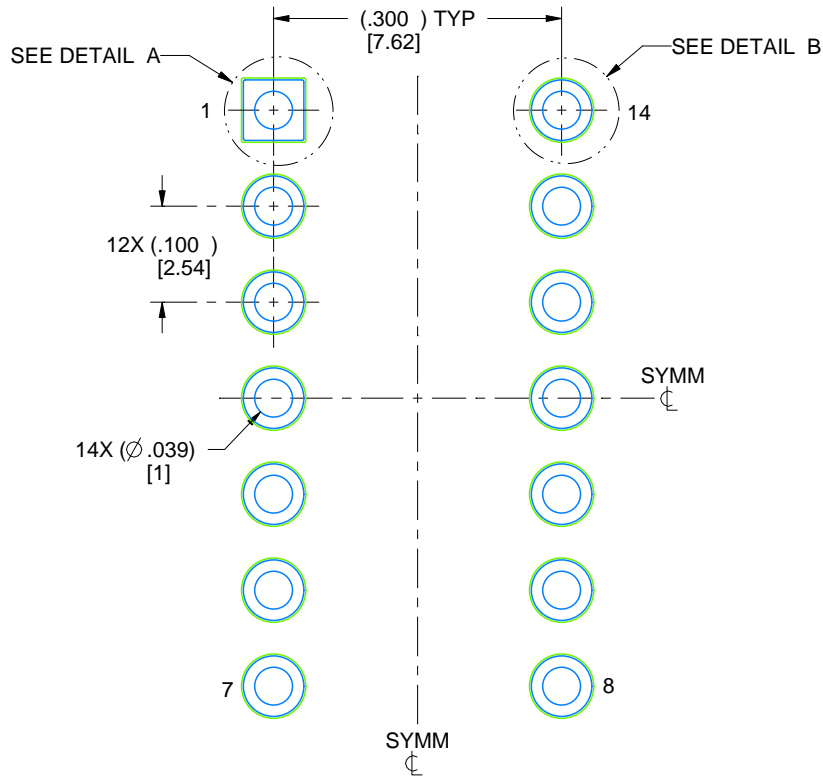
**TEXAS
INSTRUMENTS**
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EXAMPLE BOARD LAYOUT

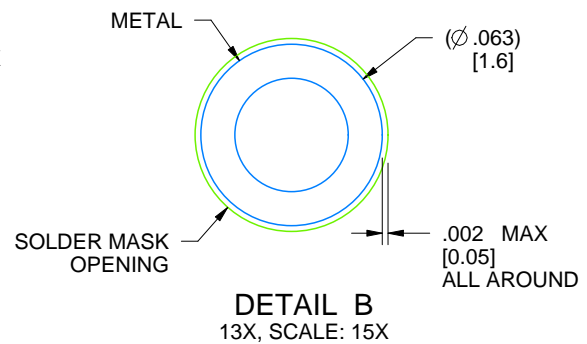
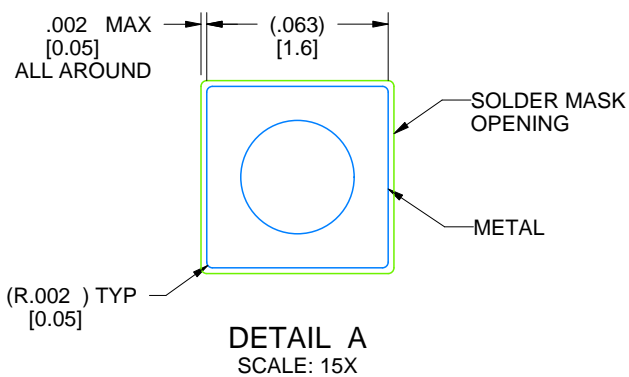
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



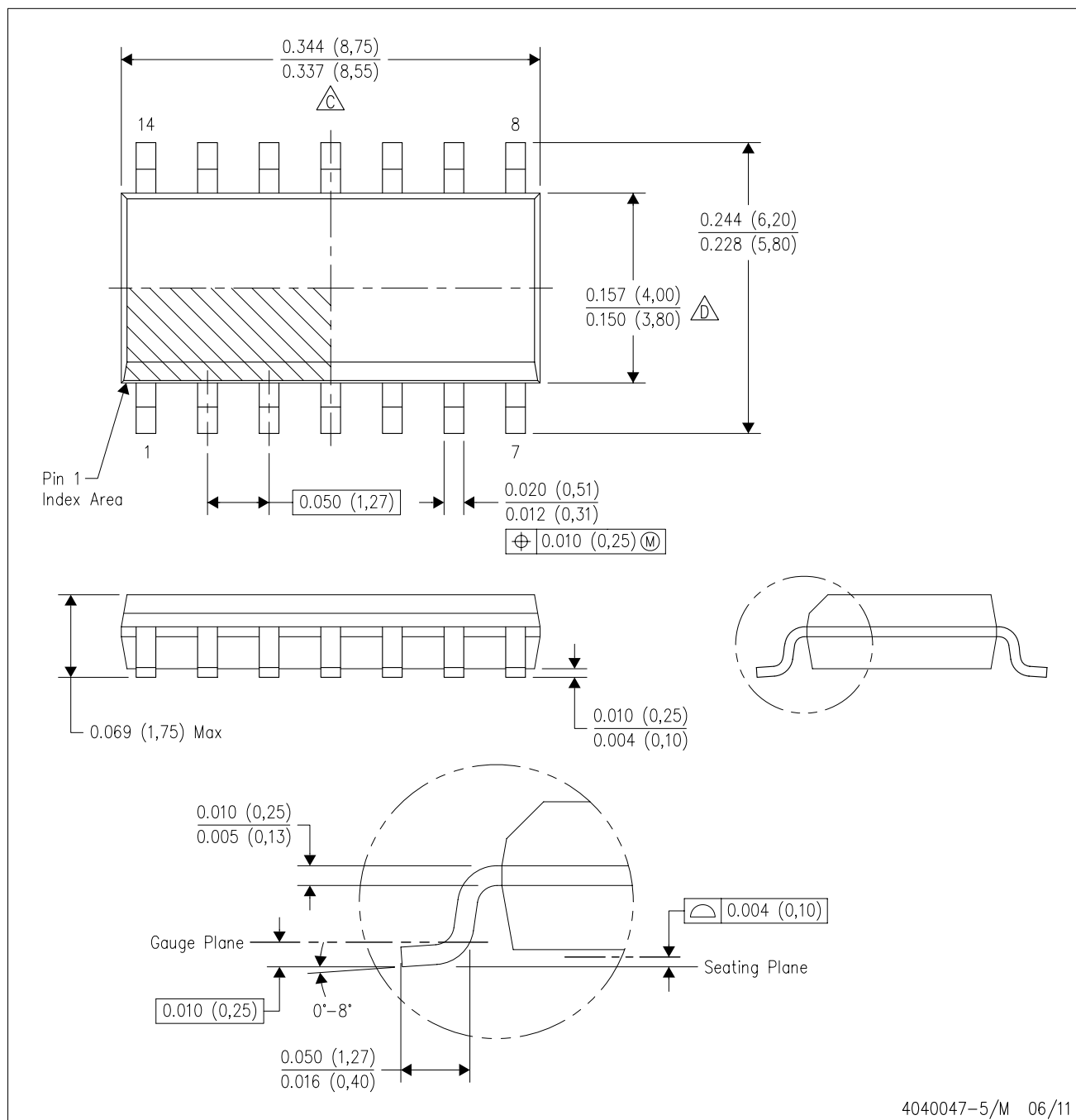
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



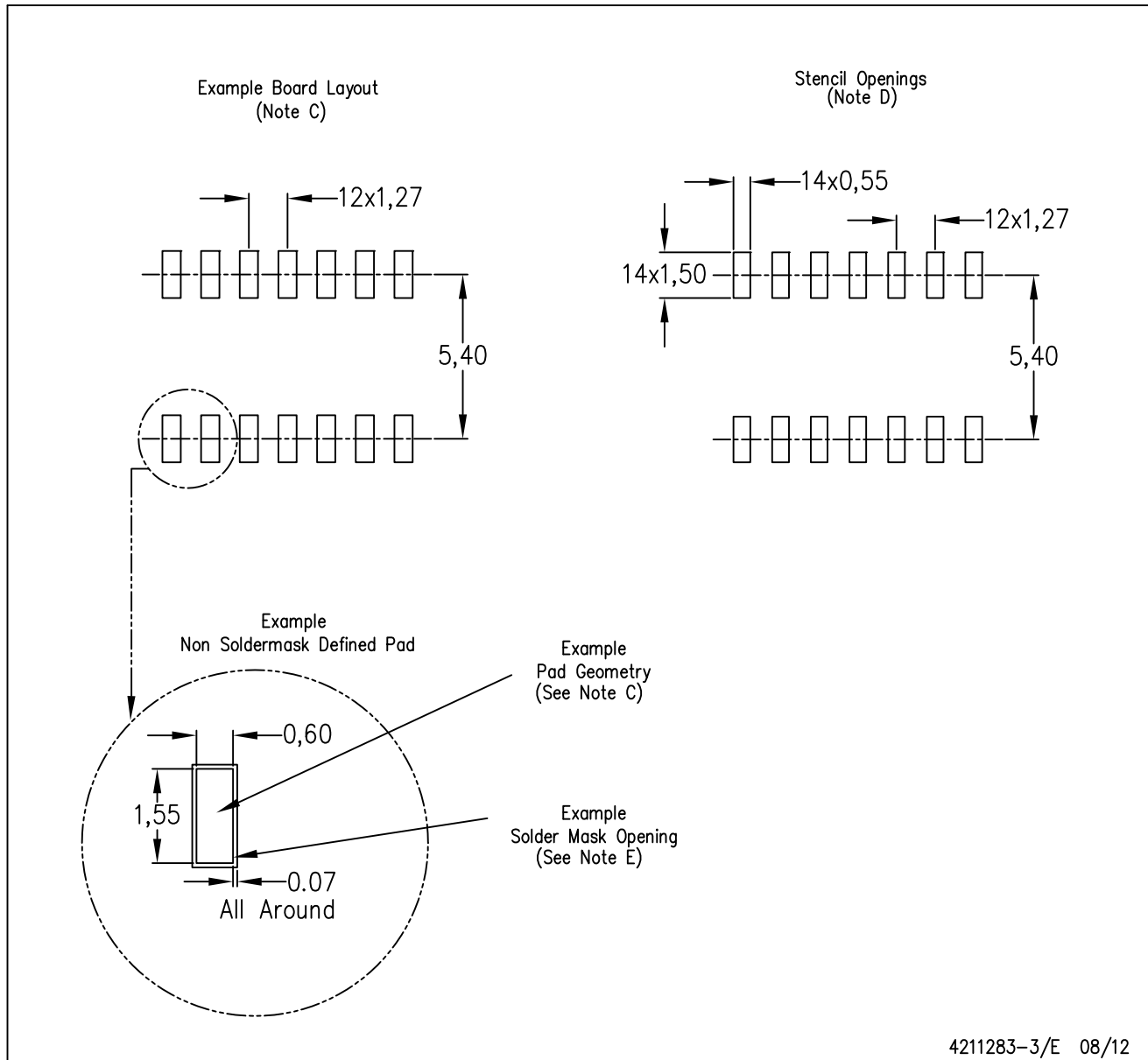
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

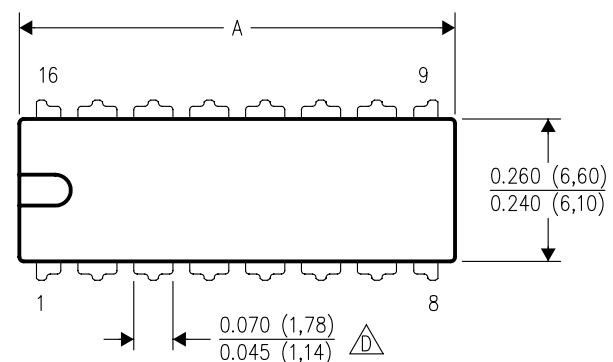


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

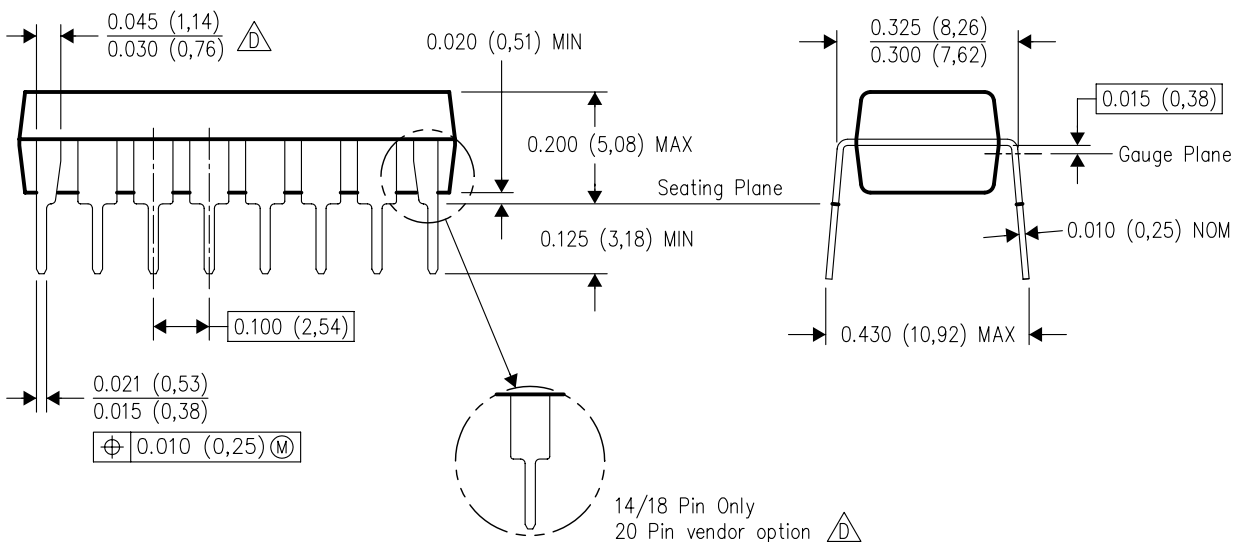
N (R-PDIP-T**)

16 PINS SHOWN



PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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