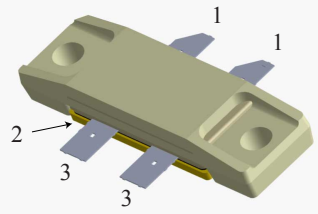
STAC9200

Datasheet

200 W, 32 V HF to 1.3 GHz LDMOS transistor in a STAC package



STAC780-4B

Pin connection	
Pin	**Connection**
1	Drain
2	Source (bottom side)
3	Gate

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
STAC9200	860 MHz	32 V	200 W	16 dB	60 %

- Improved ruggedness: $V_{(BR)DSS}$ > 80 V
- Load mismatch 65:1 all phases at 200 W, 32 V, 860 MHz, PW 1ms, DC = 10%
- P_{OUT} = 200 W min. (230 W typ.) with 16 dB gain at 860 MHz
- In compliance with the 2002/95/EC European directive
- ST air-cavity STAC packaging technology

Description

The STAC9200 is a common source N-channel enhancement-mode lateral field-effect RF power transistor designed for broadband applications in the HF to 1300 MHz frequency range. The STAC9200 benefits from the latest generation of efficient STAC package technology.

Product status link
STAC9200

Product summary	
Order code	STAC9200
Marking	STAC9200
Package	STAC780-4B
Packing	Box

1 Electrical data

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain source voltage (T_{CASE} = 25 °C)	80	V
V_{GS}	Gate-source voltage (T_{CASE} = 25 °C)	±20	V
T_J	Maximum operating junction temperature	200	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction-case thermal resistance	0.525	°C/W

Table 3. ESD protection

Symbol	Test Methodology	Class
HBM	Human Body Model (per JESD22-A114)	2

2 Electrical characteristics

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain - Source Breakdown voltage	V_{GS} = 0 V, I_{DS} = 10 mA	80			V
I_{DSS}	Zero gate voltage drain Leakage Current	V_{GS} = 0 V, V_{DS} = 28 V			1	µA
I_{GSS}	Gate - Source leakage current	V_{GS} = 15 V, V_{DS} = 0 V			1	µA
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 10 V, I_D = 250 mA	2.0		4.0	V
$V_{DS(ON)}$	Drain - Source on voltage	V_{GS} = 10 V, I_D = 3 A			0.8	V
G_{FS}	Forward transconductance	V_{DS} = 10 V, I_D = 3 A	2.5			S
C_{ISS}	Input capacitance	V_{DS} = 32 V, f = 1 MHz		113		pF
C_{OSS}	Ouput capacitance			57		pF
C_{RSS}	Reverse transfer capacitance			1.2		pF

Table 5. Dynamic (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	P_{IN} = 5 W	200	230	-	W
η_D	Drain efficiency	P_{IN} = 5 W	60	68	-	%
G_{ps}	Power gain	P_{OUT} = 200 W		18	-	dB

1. *F = 860 MHz, V_{DD} = 32 V, I_{DQ} = 100 mA.*

3 Impedance

Figure 1. Current conventions

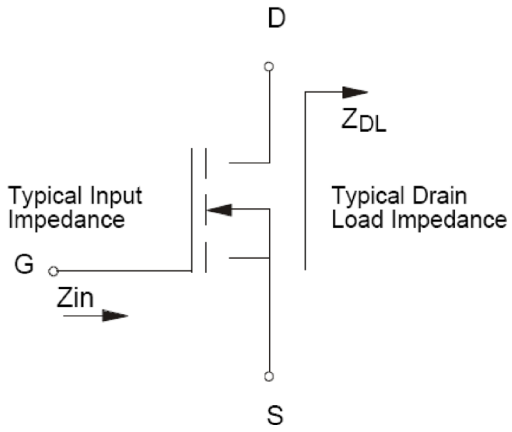


Table 6. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL}(Ω)
200	TBD	7.63 + j 2.92
280	TBD	7.02 + j 3.82
360	TBD	6.34 + j 4.52
440	TBD	5.66 + j 5.05
520	TBD	5.01 + j 5.43
600	TBD	4.42 + j 5.70
700	TBD	TBD
800	TBD	TBD
860	2.04 + j 5.33	2.33 + j 3.02
900	TBD	TBD
1000	TBD	TBD

Note: Measured gate-to-gate and drain-to-drain, respectively, balanced configuration.

4 Typical performance

Figure 2. **Output power and efficiency versus input power**

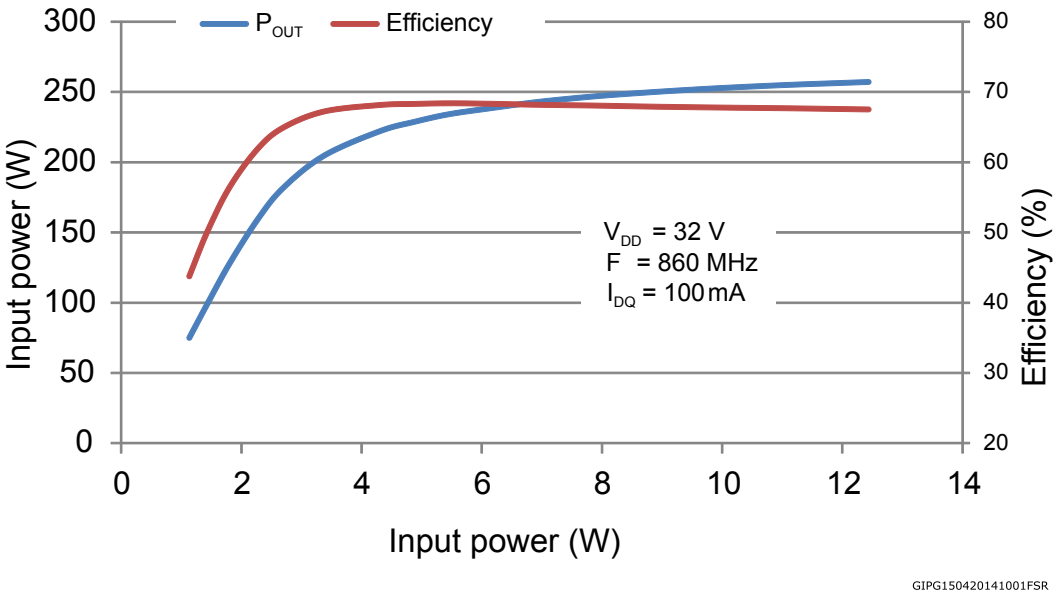
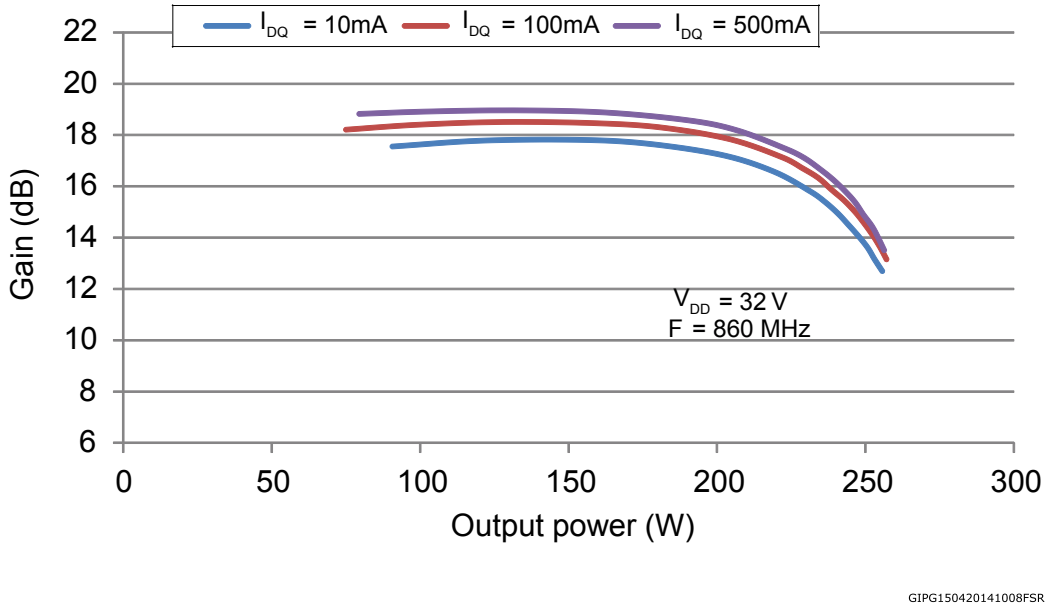


Figure 3. **Gain vs. output power and bias current**



5 Electrical schematic and BOM

Figure 4. **Electrical schematic**

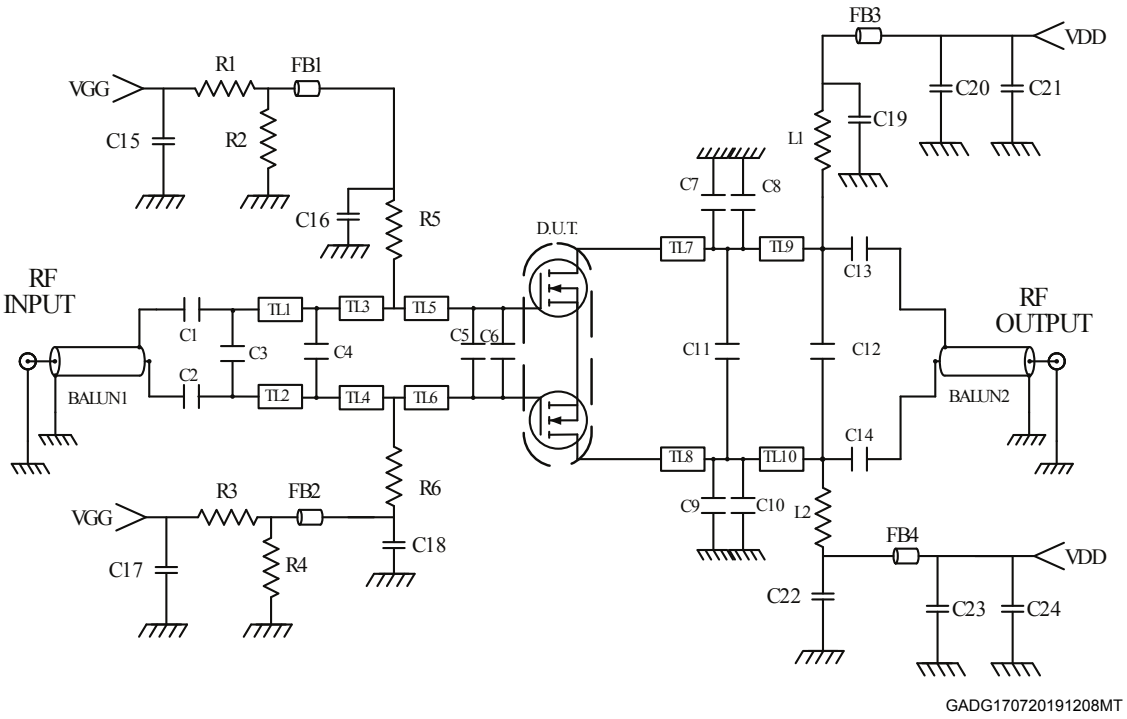
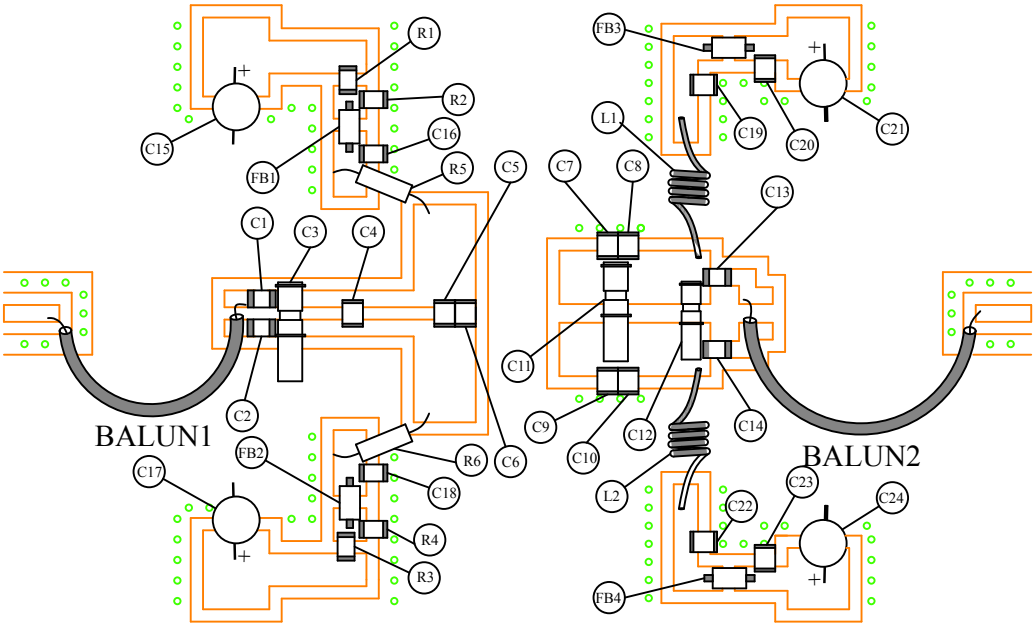


Table 7. Component list

Item	Qty	Part number	Vendor	Description
C1, C2, C13 ,C14, C16, C18, C19, C22	8	ATC100B510FW1500X	ATC	51 pF ATC 100B surface mount ceramic chip capacitor
C3, C11	2	27291PC	Johanson	0.8-8 pF Giga trim variable capacitor
C4	1	ATC100B0R6BW1500XT	ATC	0.6 pF ATC 100B surface mount ceramic chip capacitor
C5	1	ATC100B6R2BW1500XT	ATC	6.2 pF ATC 100B surface mount ceramic chip capacitor
C6	1	ATC100B150BW1500XT	ATC	15 pF ATC 100B surface mount ceramic chip capacitor
C7, C9	2	ATC100B5R1BW1500XT	ATC	5.1 pF ATC 100B surface mount ceramic chip capacitor
C8, C10	2	ATC100B4R7BW1500XT	ATC	4.7 pF ATC 100B surface mount ceramic chip capacitor
C12	1		Johanson	0.6-4.5 pF Giga trim variable capacitor
C15, C17	2	SEK101M063ST		100 µF, 63 V electrolytic capacitor
C20, C23	2	ATC200B393KW50X	ATC	39.000 pF ATC 200B surface mount ceramic chip capacitor
C21, C24	2	UPW1H222MHD		2200 µF, 50 V aluminum electrolytic capacitor
B1, B2	2	EZ141	Huber-Suhner	Balun, 50 Ω Sucoform, OD 0.141, 2.12 LG coaxial cable or equivalent
L1, L2	2		Belden	Inductor, 4 turns air-wound #18AWG ID = 0.13 in
R1, R3	2	CR1206-8W-911JB	Venkel	0.91 kΩ surface mount chip resistor
R2, R4	2	CR1206-8W-914JB	Venkel	910 kΩ surface mount chip resistor
R5, R6	2	RCO7GF510J	Allen Bradley	51 Ω 1/4W carbon composition resistor
FB1, FB2, FB3, FB4	4	2743021447	Fair-Rite Corp	Surface mount emi shield bead
TL1, TL2				L= 0.414 in W = 0.082 in
TL3, TL4				L = 0.297 in W = 0.082 in
TL5, TL6				L = 0.302 in W = 0.500 in
TL7, TL8				L = 0.385 in W = 0.260 in
TL9, TL10				L = 0.350 in W = 0.260 in
Board 3X5	1		Rogers Corp	0.030 THK , Er = 2.5, 2 Oz Cu both sides

6 Circuit layout

Figure 5. **Circuit layout**



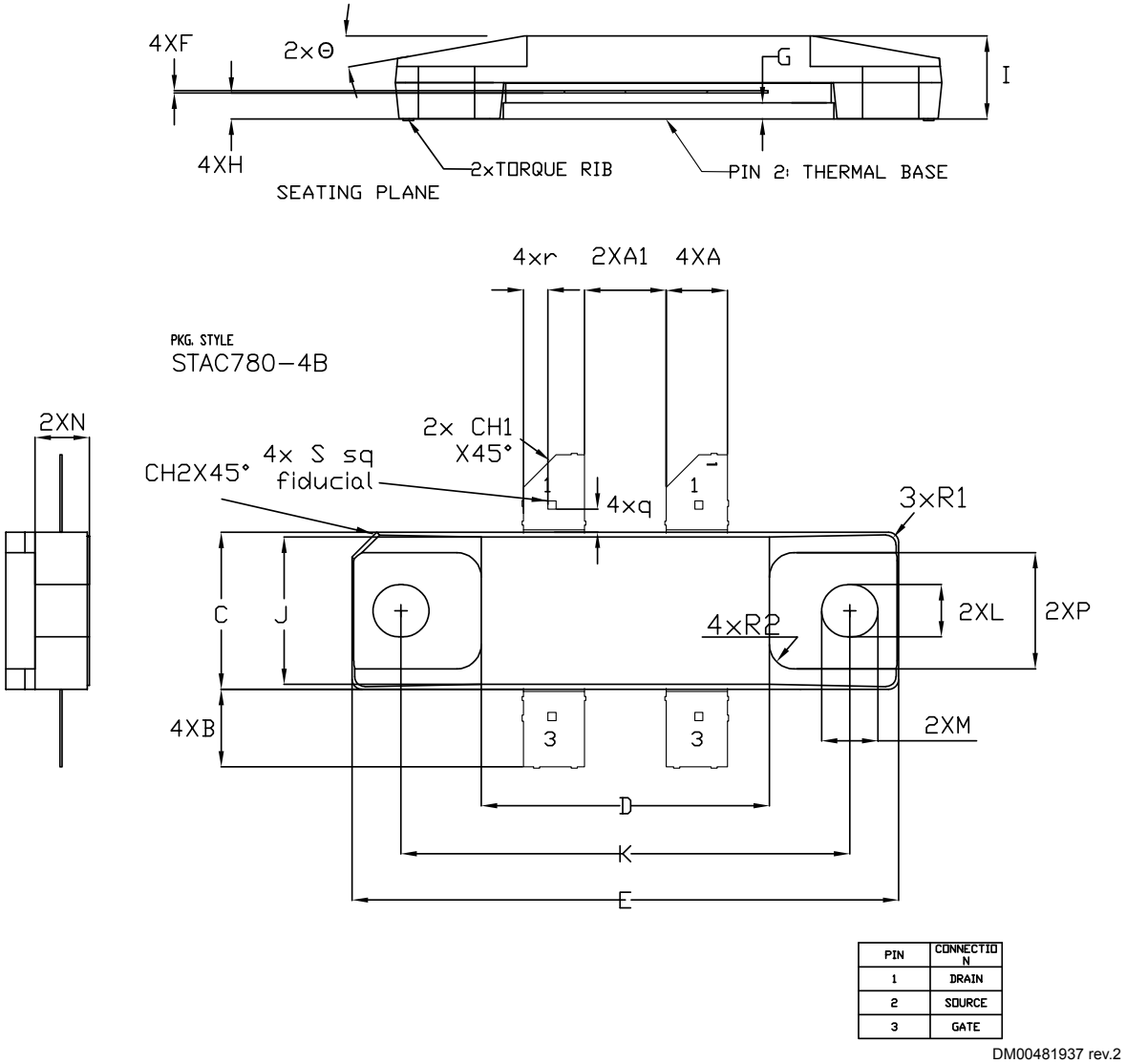
GIPG150420141026FSR

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 STAC780-4B package information

Figure 6. STAC780-4B package outline



DM00481937 rev.2

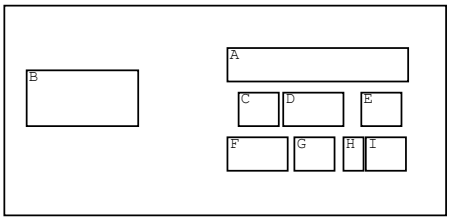
Table 8. **STAC780-4B mechanical data**

Symbol	Milimeters		
	Min	Typ	Max
A	3.76		3.86
A1	5.03		5.13
B	4.57		5.08
C	9.65		9.91
D	17.78		18.08
E	33.88		34.19
F	0.13		0.18
G	0.97		1.14
H	1.52		1.70
I	4.83		5.33
J	9.52		9.78
K	27.69		28.19
L	3.20	3.25	3.30
M	3.43	3.51	3.58
M	3.30	3.38	3.45
p	7.14	7.21	7.29
q		1.45	
R1		0.64	
R2		1.52	
r		1.52	
s		0.51	
Θ		10°	
CH1		2.03	
CH2		1.52	

7.2 Marking information

Figure 7. **Marking information**

PACKAGE FACE : TOP



LEGEND

Marking Composition Field

A - MARKING AREA
B - ST LOGO
C - Assy Plant
(PP)
D - BE Sequence
(LLL)
E - Diffusion Traceability Plant
(WX)
F - COUNTRY OF ORIGIN
(MAX CHAR ALLOWED = 3)
G - Test & Finishing Plant
(TF)
H - Assy Year
(Y)
I - Assy Week
(WW)

Revision history

Table 9. **Document revision history**

Date	Version	Changes
21-Oct-2013	1	Initial release.
22-Apr-2014	2	Updated features in cover page, Table 4: Dynamic and Table 5: Impedance data. Added Section 4: Typical performance, Section 5: Electrical schematic and BOM and Section 6: Circuit layout.
10-Nov-2015	3	Added Section 1.2: Thermal data. Minor text changes.
20-Mar-2020	4	Updated package information. Added Table 3.

Contents

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