**TEXAS INSTRUMENTS**

# 具有三态取消选定输出 SN74LVC1G18 2 选 1 同相多路信号分离器

## 1 特性

- 工作温度范围为 –40°C 至 +125°C
- 支持 5V $V_{CC}$ 运行
- 输入电压高达 5.5V
- 支持向下转换到 $V_{CC}$
- 电压为 3.3V 时，$t_{pd}$ 最大值为 3.4ns
- 低功耗，$I_{CC}$ 最大值为 10µA
- 电压为 3.3V 时，输出驱动为 ±24mA
- 在 $V_{CC}$ = 3.3V、$T_A$ = 25°C 时，$V_{OLP}$（输出接地反弹）
  典型值小于 0.8V
- 在 $V_{CC}$ = 3.3V，$T_A$ = 25°C 时，$V_{OHV}$（输出 $V_{OH}$ 下冲）
  典型值大于 2V
- $I_{off}$ 支持带电插入、局部关断模式和后驱动保护
- 闩锁性能超过 100mA，
  符合 JESD 78 II 类规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器模型 (A115-A)
  - 1000V 充电器件模型 (C101)

## 2 应用

- 数据中心交换机
- 基带单元 (BBU)
- Wi-Fi 接入点
- 笔记本电脑
- 有源天线系统 (AAS)
- 电器
- 工业监控器
- 咖啡机
- 有线扬声器
- 扫地机器人
- 专业音频接口

## 3 说明

此同相多路信号分离器专为 1.65V 至 5.5V $V_{CC}$ 运行而设计。

SN74LVC1G18 器件是一款具有三态输出的 2 选 1 同相多路信号分离器。此器件在输入端 A 上缓冲数据，然后根据选定输入端的状态是低还是高，将数据分别传递至输出端 Y0 或 Y1。
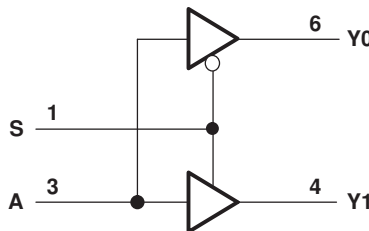
NanoFree™封装技术是 IC 封装概念的一项重大突破，它将硅晶片用作封装。

该器件完全 适用于 $I_{off}$ 为了部分断电的应用。$I_{off}$ 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。

### 器件信息[(1)]

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| SN74LVC1G18DBVR | SOT-23 (6) | 2.90mm x 2.80mm |
| SN74LVC1G18DCKR | SC70 (6) | 2.00mm × 1.10mm |
| SN74LVC1G18DRYR | SON (6) | 1.45mm x 1.00mm |
| SN74LVC1G18DSFR | SON (6) | 1.00mm × 1.00mm |
| SN74LVC1G18YZPR | DSBGA (6) | 1.39mm × 0.89mm |

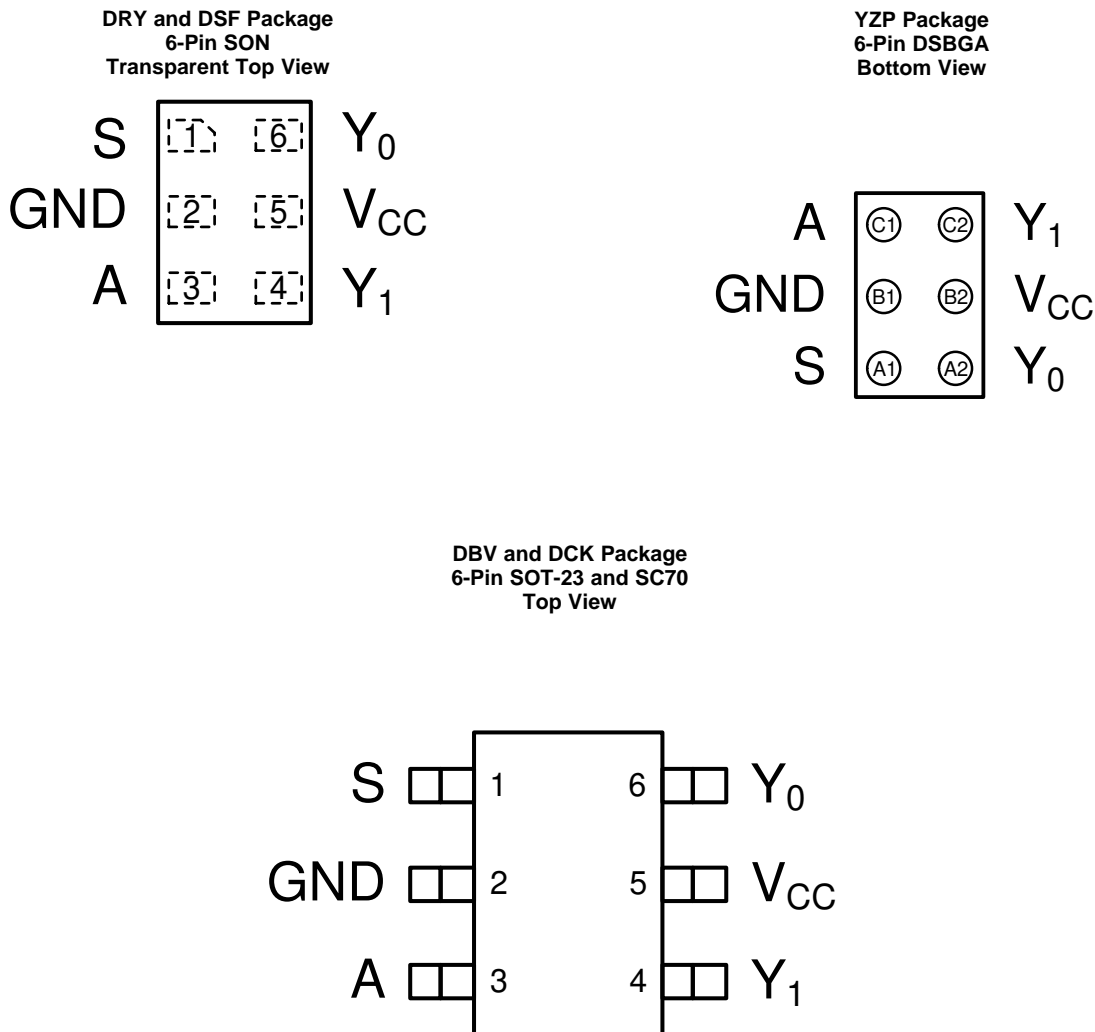(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图

## 目录

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision K (July 2012) to Revision L**                   **Page**

- 将文档更新为新的 TI 数据表格式。 ................................................................................................................. 1
- 已删除 订购信息表。 ...................................................................................................................................... 1
- 更新了 $I_{off}$ 特性中添加了"INA212-Q1：1000V/V".................................................................................... 1
- 已添加 音频播放器. .......................................................................................................................................... 1
- 已添加 添加了器件信息表 ................................................................................................................................. 1
- Added Operating junction temperature................................................................................................................ 5
- Added Handling Ratings table............................................................................................................................. 5
- Added Thermal Information table. ...................................................................................................................... 6

## 5 Pin Configuration and Functions

**DRY and DSF Package**
**6-Pin SON**
**Transparent Top View**

```
 S    [1]  [6]   Y0
GND   [2]  [5]   VCC
 A    [3]  [4]   Y1
```

**YZP Package**
**6-Pin DSBGA**
**Bottom View**

```
 A    (C1)  (C2)   Y1
GND   (B1)  (B2)   VCC
 S    (A1)  (A2)   Y0
```

**DBV and DCK Package**
**6-Pin SOT-23 and SC70**
**Top View**

```
 S  ▭  1    6  ▭  Y0
GND ▭  2    5  ▭  VCC
 A  ▭  3    4  ▭  Y1
```

Not to scale. See the mechanical drawings at the end of the data sheet for package dimensions.

### Pin Functions

| NAME | DBV, DCK, DRY, DSF | YZP | I/O | DESCRIPTION |
|---|---|---|---|---|
| S | 1 | A1 | Input | Active output selection (LOW = Y0, HIGH = Y1) |
| GND | 2 | B1 | — | Ground |
| A | 3 | C1 | Input | Input A |
| $Y_1$ | 4 | C2 | Output | Output $Y_1$ |
| $V_{CC}$ | 5 | B2 | — | Positive supply |
| $Y_0$ | 6 | A2 | Output | Output $Y_0$ |

**Logic Diagram (Positive Logic)**
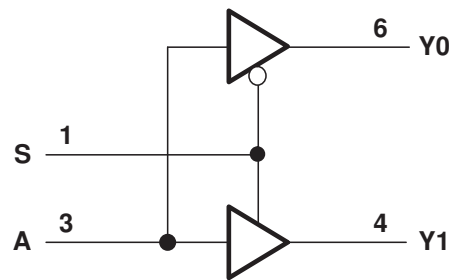
# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

|          |                                                                              |           | MIN  | MAX             | UNIT |
|----------|------------------------------------------------------------------------------|-----------|------|-----------------|------|
| $V_{CC}$ | Supply voltage range                                                         |           | −0.5 | 6.5             | V    |
| $V_I$    | Input voltage range [2]                                                      |           | −0.5 | 6.5             | V    |
| $V_O$    | Voltage range applied to any output in the high-impedance or power-off state [3] |       | −0.5 | 6.5             | V    |
| $V_O$    | Voltage range applied to any output in the high or low state [2][1]          |           | −0.5 | $V_{CC}$ + 0.5  | V    |
| $I_{IK}$ | Input clamp current                                                          | $V_I < 0$ |      | −50             | mA   |
| $I_{OK}$ | Output clamp current                                                         | $V_O < 0$ |      | −50             | mA   |
| $I_O$    | Continuous output current                                                    |           |      | ±50             | mA   |
|          | Continuous current through $V_{CC}$ or GND                                   |           |      | ±100            | mA   |
| $T_J$    | Operating junction temperature                                               |           |      | 150             | °C   |
| $T_{stg}$| Storage temperature                                                          |           | −65  | 150             | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 6.2 ESD Ratings

|             |                           |                                                                   | VALUE | UNIT |
|-------------|---------------------------|-------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge   | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]            | 2000  | V    |
|             |                           | Charged device model (CDM), per JEDEC specification JESD22-C101 [2] | 1000  |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.7 × $V_{CC}$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.3 × $V_{CC}$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | −4 | mA |
| | | $V_{CC}$ = 2.3 V | | −8 | |
| | | $V_{CC}$ = 3 V | | −16 | |
| | | | | −24 | |
| | | $V_{CC}$ = 4.5 V | | −32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 10 | |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 5 | |
| $T_A$ | Operating free-air temperature | | −40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74LVC1G18 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | DBV | DCK | DRY | DSF | YZP | |
| | | 6 PINS | 6 PINS | 6 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 236.1 | 278.7 | 306.7 | 300.3 | 123.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 174.0 | 217.8 | 207.2 | 183.5 | 1.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 111.5 | 124.6 | 181.1 | 170.7 | 38.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 93.5 | 105.2 | 49.9 | 24.2 | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 111.2 | 124.1 | 180.3 | 170.2 | 38.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | -40 to 85°C | | | -40 to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP[1] | MAX | MIN | TYP[1] | MAX | |
| $V_{OH}$ | $I_{OH}$ = −100 μA | | 1.65 V to 5.5 V | $V_{CC} -$ 0.1 | | | $V_{CC} -$ 0.1 | | | V |
| | $I_{OH}$ = −4 mA | | 1.65 V | 1.2 | | | 1.2 | | | |
| | $I_{OH}$ = −8 mA | | 2.3 V | 1.9 | | | 1.9 | | | |
| | $I_{OH}$ = −16 mA | | 3 V | 2.4 | | | 2.4 | | | |
| | $I_{OH}$ = −24 mA | | | 2.3 | | | 2.3 | | | |
| | $I_{OH}$ = −32 mA | | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 μA | | 1.65 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | | | 0.45 | |
| | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.3 | | | 0.3 | |
| | $I_{OL}$ = 16 mA | | 3 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | | | | 0.55 | | | 0.55 | |
| | $I_{OL}$ = 32 mA | | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | | 0 to 5.5 V | | | ±5 | | | ±5 | μA |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±10 | | | ±10 | μA |
| $I_{OZ}$ | $V_O$ = 0 to 5.5 V | | 3.6 V | | | 10 | | | 10 | μA |
| $I_{CC}$ | $V_I$ = 5.5 V or GND, $I_O$ = 0 | | 1.65 V to 5.5 V | | | 10 | | | 10 | μA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ − 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V | | | 500 | | | 500 | μA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 4 | | | 4 | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 6 | | | 6 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 6.6 Switching Characteristics, –40 to 85°C

$T_A$ = –40 to 85°C, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see *Parameter Measurement Information*)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CONDITION | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | 2.3 | 8.4 | 1.1 | 4.2 | 1.1 | 3.4 | 0.8 | 2.7 | ns |
| | | | $C_L$ = 30 pF or 50 pF | 3.5 | 9.3 | 1.7 | 5 | 1.5 | 4.2 | 0.7 | 3.2 | ns |
| $t_{en}$ | S | Y | $C_L$ = 30 pF or 50 pF | 3.6 | 10.2 | 1.7 | 5.6 | 1.5 | 4.6 | 0.9 | 3.4 | ns |
| $t_{dis}$ | S | Y | $C_L$ = 30 pF or 50 pF | 1.9 | 12.7 | 1 | 5.3 | 1.1 | 4.9 | 0.5 | 3.3 | ns |

## 6.7 Switching Characteristics, –40 to 125°C

over recommended operating free-air temperature range, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see *Parameter Measurement Information*)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CONDITION | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 30 pF or 50 pF | 3.5 | 9.8 | 1.7 | 5.5 | 1.5 | 4.7 | 0.7 | 3.7 | ns |
| $t_{en}$ | S | Y | $C_L$ = 30 pF or 50 pF | 3.6 | 11.2 | 1.7 | 6.6 | 1.5 | 6.1 | 0.9 | 4.9 | ns |
| $t_{dis}$ | S | Y | $C_L$ = 30 pF or 50 pF | 1.9 | 13.7 | 1 | 6.3 | 1.1 | 6.4 | 0.5 | 4.8 | ns |

## 6.8   Operating Characteristics

$T_A = 25°C$

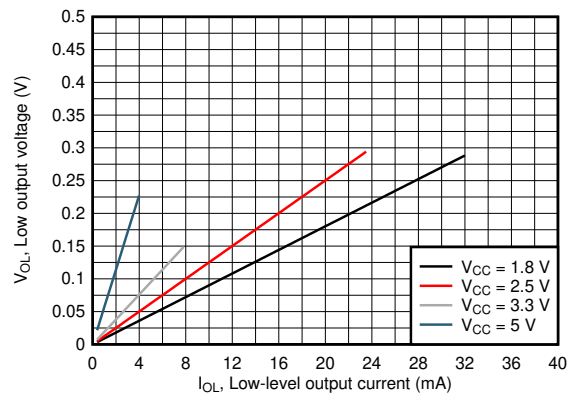| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 17 | 17 | 18 | 21 | pF |

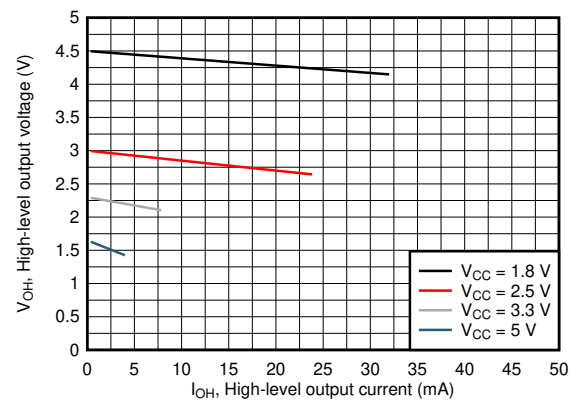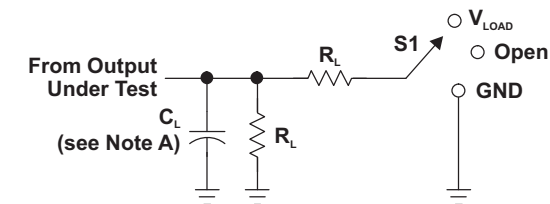## 6.9   Typical Characteristics

$T_A = 25°C$; Simulated data



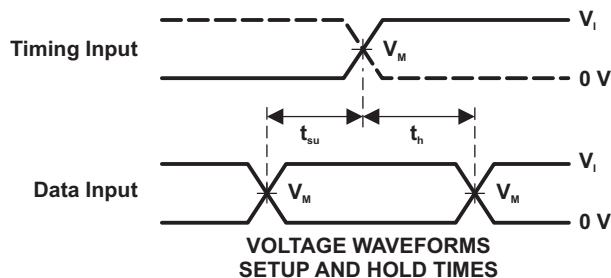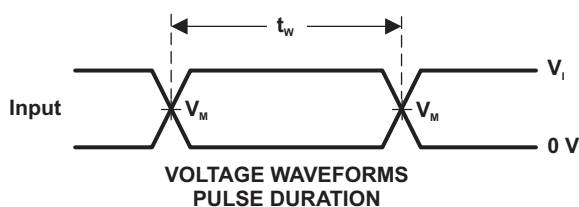**Figure 1. Typical low-level output voltage at common supply values and currents**



**Figure 2. Typical high-level output voltage at common supply values and currents**

# 7 Parameter Measurement Information



**LOAD CIRCUIT**

| TEST | S1 |
|------|-----|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 15 pF | 1 MΩ | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.3 V |



**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES:  A. $C_L$ includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
   D. The outputs are measured one at a time, with one transition per measurement.
   E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
   F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
   G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
   H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

## Parameter Measurement Information (continued)

**LOAD CIRCUIT**

| TEST | S1 |
|------|-----|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|----------|--------|-----|-------|------------|-------|-------|------------|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |

**VOLTAGE WAVEFORMS
PULSE DURATION**

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   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
   D. The outputs are measured one at a time, with one transition per measurement.
   E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
   F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
   G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
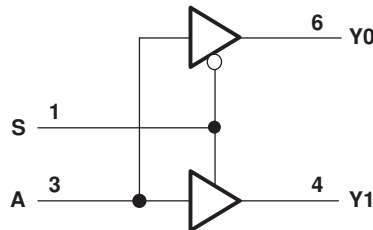   H. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

This device contains one independent 1-of-2 noninverting demultiplexer with high-impedance outputs when disabled.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Balanced CMOS 3-State Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

3-State outputs can be placed into a high-impedance state. In this state, the output will neither source nor sink current, and leakage current is defined by the $I_{OZ}$ specification in the *Electrical Characteristics*. A pull-up or pull-down resistor can be used to ensure that the output remains HIGH or LOW, respectively, during the high-impedance state.

### 8.3.2 Partial Power Down ($I_{off}$)

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off}$ in the *Electrical Characteristics*.

### 8.3.3 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* , and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

### 8.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions* .

### 8.3.5 Clamp Diode Structure

The inputs and outputs to this device have negative clamping diodes only as depicted in Figure 5.

**Feature Description (continued)**

> **CAUTION**
>
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
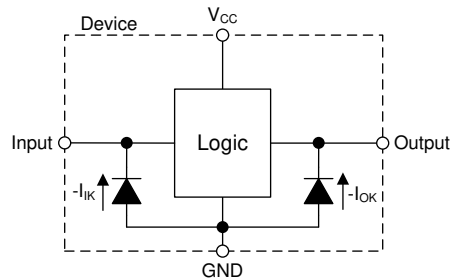


**Figure 5. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**Table 1. Function Table**

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| **S** | **A** | **Y0** | **Y1** |
| L | L | L | Z |
| L | H | H | Z |
| H | L | Z | L |
| H | H | Z | H |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC1G18 can be used to select between controlling two analog switches. In this use case, pull-down resistors are connected to both outputs of the SN74LVC1G18 to ensure that a valid state is available for the inputs to the switches at all times. This defaults the switches into the "off" state to prevent unwanted data transmission.

## 9.2 Typical Application
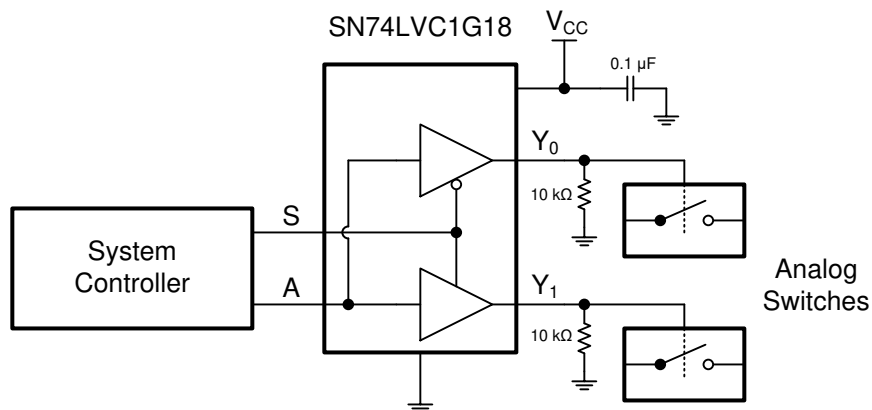


**Figure 6. Typical application block diagram**

### 9.2.1 Design Requirements

- Each analog switch must be controlled by the system controller, but only when the other switch is disabled.
- When the input S is low, the $Y_0$ output is selected and the $Y_1$ output is in the high impedance state
- When the input S is high, the $Y_1$ output is selected and the $Y_0$ output is in the high impedance state
- When the input A is high, the selected analog switch must be closed
- When the input A is low, the selected analog switch must be open

#### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions* . The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC1G18 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or $V_{CC}$ listed in the *Absolute Maximum Ratings* .

The SN74LVC1G18 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF.

## Typical Application (continued)

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and C$_{pd}$ Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

---

### CAUTION

The maximum junction temperature, T$_J$(max) listed in the *Absolute Maximum Ratings* , is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings* . These limits are provided to prevent damage to the device.

---

### 9.2.1.2 Input Considerations

Unused inputs must be terminated to either V$_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74LVC1G18, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74LVC1G18 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions* .

Refer to the *Feature Description* for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V$_{OH}$ specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V$_{OL}$ specification in the *Electrical Characteristics*. The plots in the *Typical Characteristics* provide a relationship between output voltage and current for this device.

Unused outputs can be left floating.

Refer to *Feature Description* for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V$_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V$_{CC}$ and GND pins. An example layout is shown in the *Layout*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC1G18 to the receiving device.
3. Ensure the resistive load at the output is larger than (V$_{CC}$ / 25 mA) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*

# Typical Application (continued)
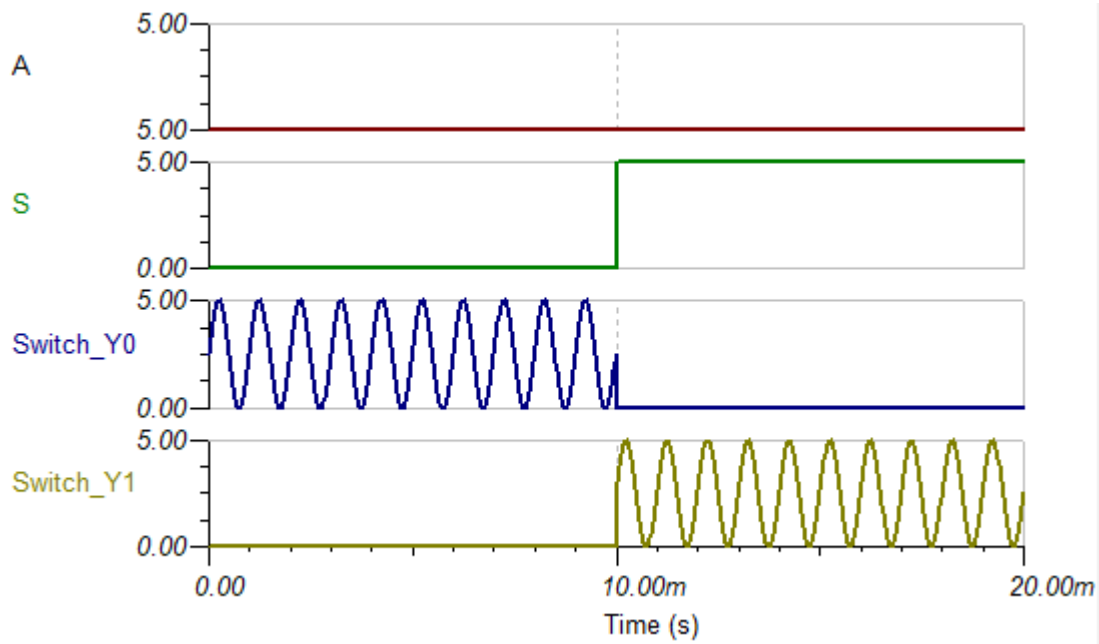
## 9.2.3 Application Curves



**Figure 7. Simulated application transient response**

## 10   Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* . Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in Figure 8.

## 11   Layout

### 11.1   Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.
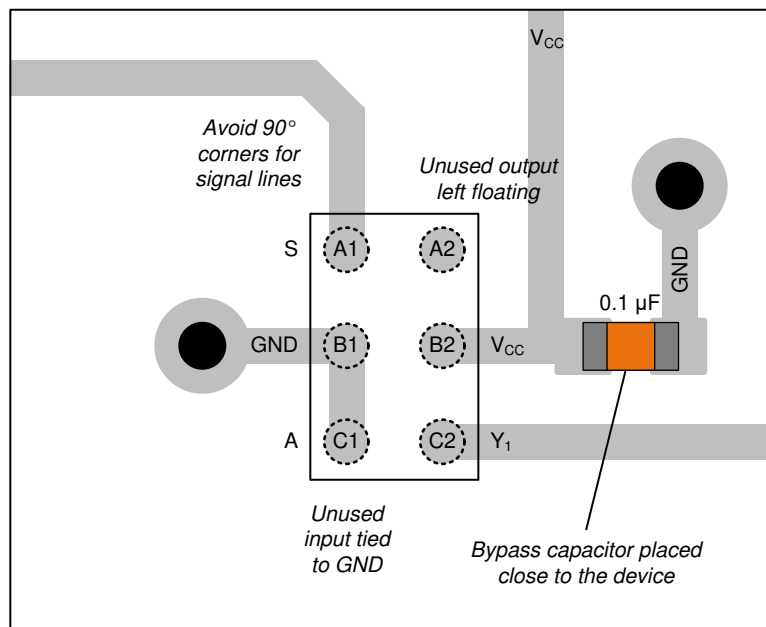
### 11.2   Layout Example



**Figure 8.  Example layout for the SN74LVC1G18**

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档：
- *《慢速或浮点 CMOS 输入的影响》*
- *《CMOS 功耗与 $C_{pd}$ 计算》*
- *《了解和解读标准逻辑器件数据表》*

### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

NanoFree, E2E are trademarks of Texas Instruments.

### 12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## 重要声明和免责声明

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G18DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C185, C18R) | Samples |
| SN74LVC1G18DBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C185, C18R) | Samples |
| SN74LVC1G18DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | (CJ5, CJF, CJJ, CJ K, CJR) | Samples |
| SN74LVC1G18DCKRE4 | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CJ5 | Samples |
| SN74LVC1G18DCKRG4 | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CJ5 | Samples |
| SN74LVC1G18DRYR | ACTIVE | SON | DRY | 6 | 5000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CJ | Samples |
| SN74LVC1G18DSFR | ACTIVE | SON | DSF | 6 | 5000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CJ | Samples |
| SN74LVC1G18YZPR | ACTIVE | DSBGA | YZP | 6 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CJN | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|---|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G18DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G18DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G18DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G18DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G18DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G18DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G18DCKRG4 | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G18DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G18DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G18YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1G18DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G18DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G18DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G18DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G18DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G18DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G18DCKRG4 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G18DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G18DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G18YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS
INSTRUMENTS

B ← 1.05 / 0.95 → A

PIN 1 INDEX AREA

1.5 / 1.4

0.6 MAX

C

SEATING PLANE

0.05 / 0.00

⌒ 0.08 C

3X 0.6

SYMM ₵

(0.05) TYP

3

4X 0.5

2X 1

4

SYMM ₵

1

6

0.4 / 0.3

PIN 1 ID (OPTIONAL)

6X 0.25 / 0.15

⊕ 0.1 Ⓜ C A B
  0.05 Ⓜ C

5X 0.35 / 0.25

(0.127) TYP

4222894/A   01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

**TEXAS INSTRUMENTS**

www.ti.com

SYMM

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)
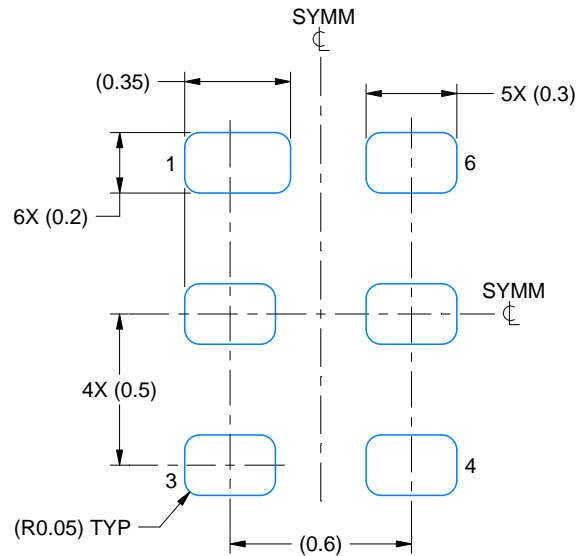
**LAND PATTERN EXAMPLE**
1:1 RATIO WITH PKG SOLDER PADS
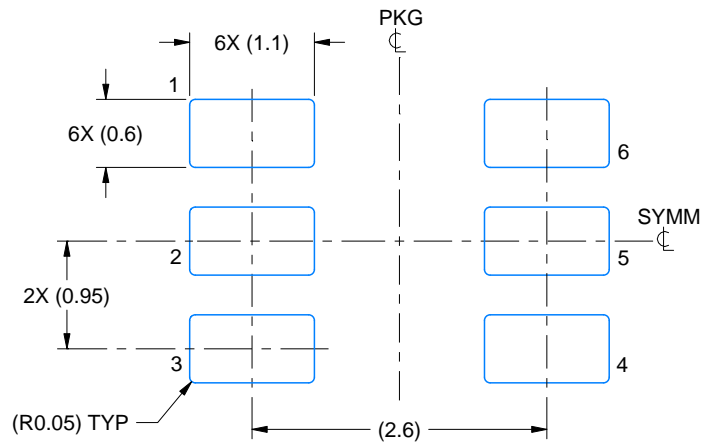EXPOSED METAL SHOWN
SCALE:40X

0.05 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED**

0.05 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED
(PREFERRED)**

**SOLDER MASK DETAILS**

4222894/A   01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).
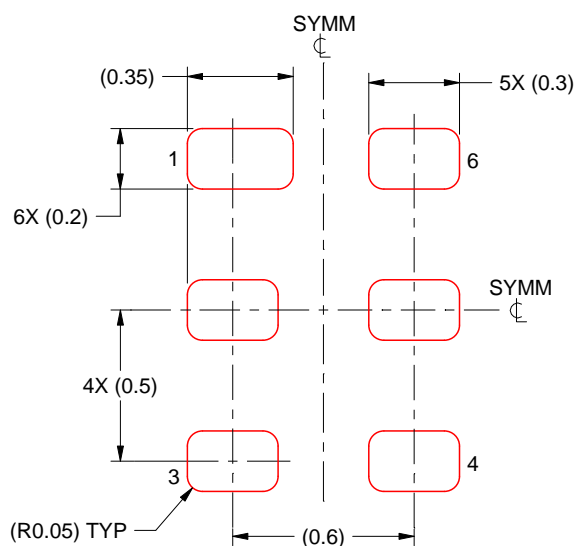
SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A   01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

## PACKAGE OUTLINE

**DBV0006A**

**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



3.0 / 2.6

1.75 / 1.45

PIN 1 INDEX AREA

2X 0.95

1.9

6X 0.50 / 0.25

⊕ 0.2 Ⓜ C A B

B

A

3.05 / 2.75

C

◯ 0.1 C

1.45 MAX

(1.1)

0.15 / 0.00 TYP

0.25 GAGE PLANE

0.22 / 0.08 TYP

8° / 0° TYP

0.6 / 0.3 TYP

SEATING PLANE

4214840/B  03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
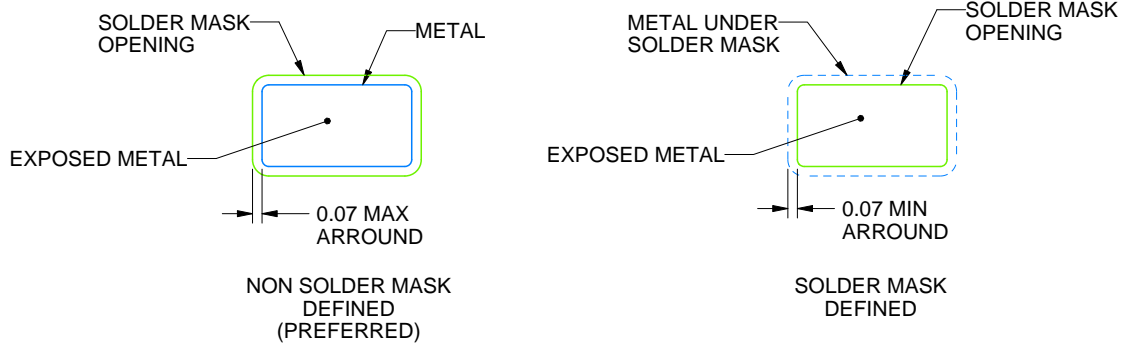5. Refernce JEDEC MO-178.

TEXAS INSTRUMENTS
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PKG ℄

6X (1.1)

1

6X (0.6)

2

SYMM ℄

6

5

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214840/B   03/2018

NOTES: (continued)
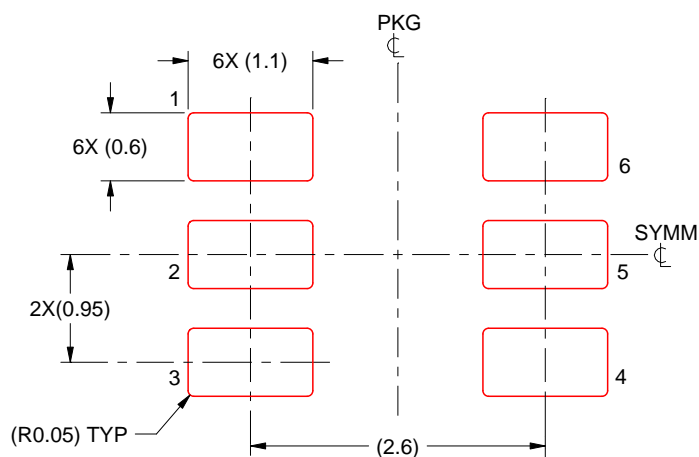
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

6X (1.1)

1

6X (0.6)

2

2X(0.95)

3
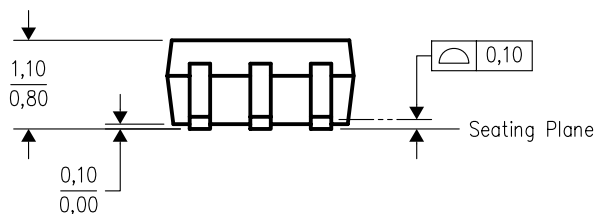
(R0.05) TYP

(2.6)

SYMM

6

5

4

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B   03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
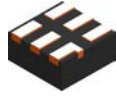
DCK (R-PDSO-G6)  PLASTIC SMALL-OUTLINE PACKAGE



2,15 / 1,85

2,40 / 1,80

1,40 / 1,10

Pin 1 Index Area

0,65

1,30

6X 0,30 / 0,15

⊕ 0,10 Ⓜ

0,22 / 0,08

Gauge Plane
Seating Plane

0,15

0°-8°

0,46 / 0,26

1,10 / 0,80

△ 0,10

Seating Plane

0,10 / 0,00

4093553-4/G  01/2007

NOTES:  A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 D. Falls within JEDEC MO-203 variation AB.

TEXAS INSTRUMENTS
www.ti.com

DCK (R–PDSO–G6)                    PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

4x0,65

2x1,30

4x0,65

2x1,30

0,4

Solder Mask Opening

1,0    0,9

Pad Geometry

0,05

0,50

4210356–3/C  07/11

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
        D.  Publication IPC–7351 is recommended for alternate designs.
        E.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
            contact their board assembly site for stencil design recommendations.  Example stencil design based on a 50% volumetric
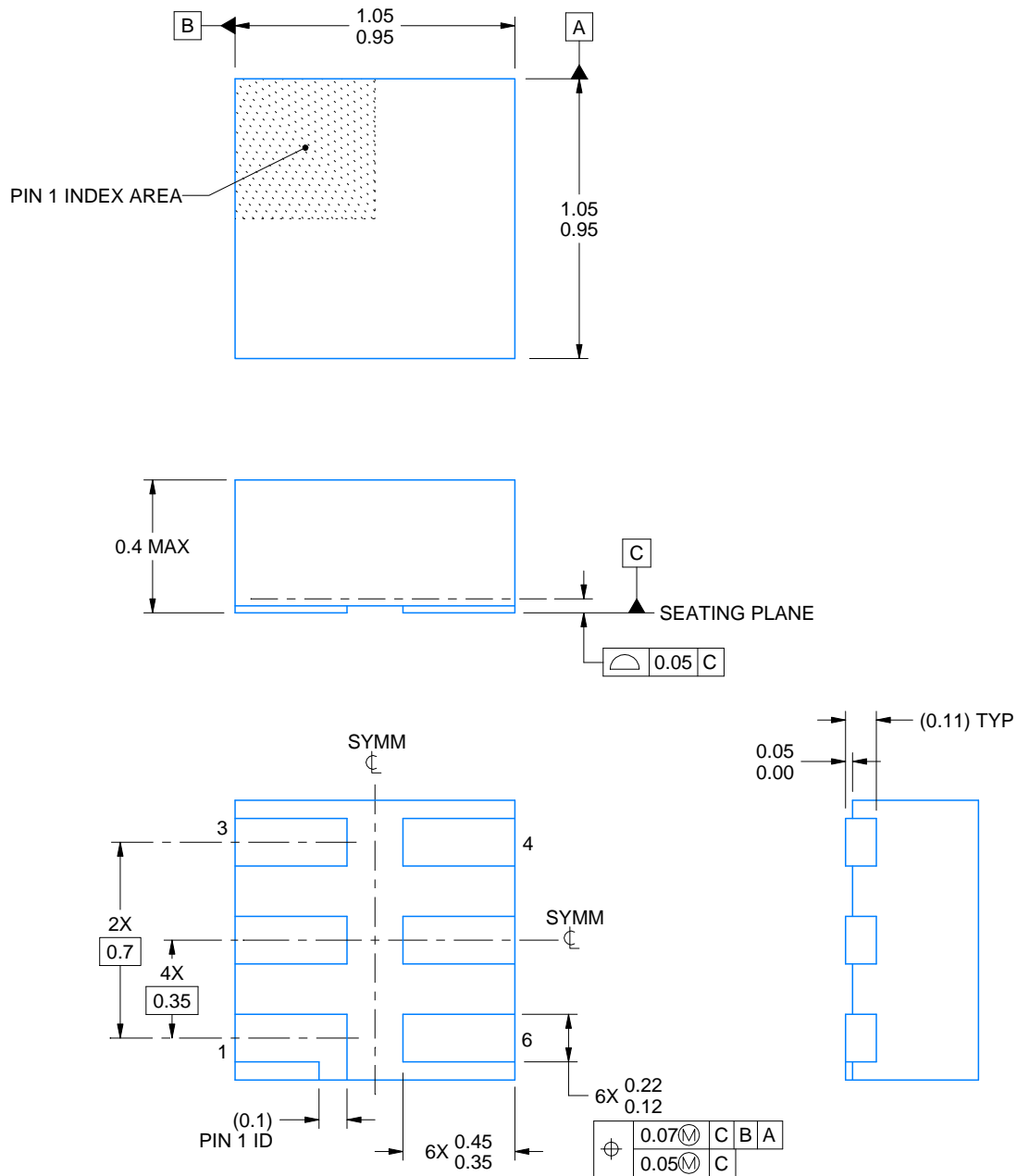            metal load solder paste.  Refer to IPC–7525 for other stencil recommendations.

B

1.05
0.95

A

PIN 1 INDEX AREA

1.05
0.95

0.4 MAX

C

SEATING PLANE

△ 0.05 C

SYMM

(0.11) TYP

0.05
0.00

3

4

2X
0.7

SYMM

4X
0.35

1

6

(0.1)
PIN 1 ID

6X 0.45
0.35

6X 0.22
0.12

⊕ | 0.07Ⓜ | C | B | A
0.05Ⓜ | C
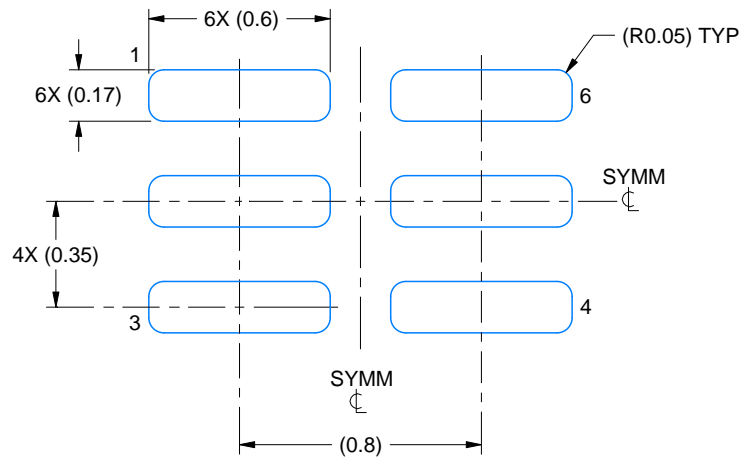
4220597/A   06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

6X (0.6)

1

6X (0.17)

(R0.05) TYP

6

SYMM
₵

4X (0.35)

3

4

SYMM
₵

(0.8)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE:40X

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED**

0.07 MIN
ALL AROUND

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**
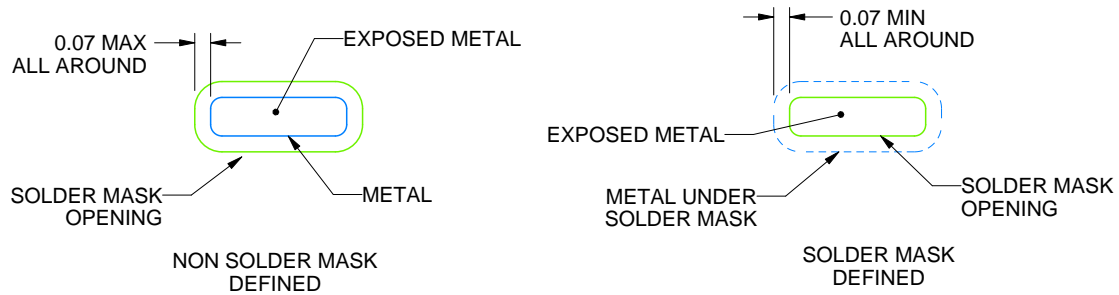
**SOLDER MASK DETAILS**

4220597/A   06/2017

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

TEXAS
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6X (0.6)

1

6X (0.17)

(R0.05) TYP

6

SYMM
℄

4X (0.35)

3

4

SYMM
℄

(0.8)
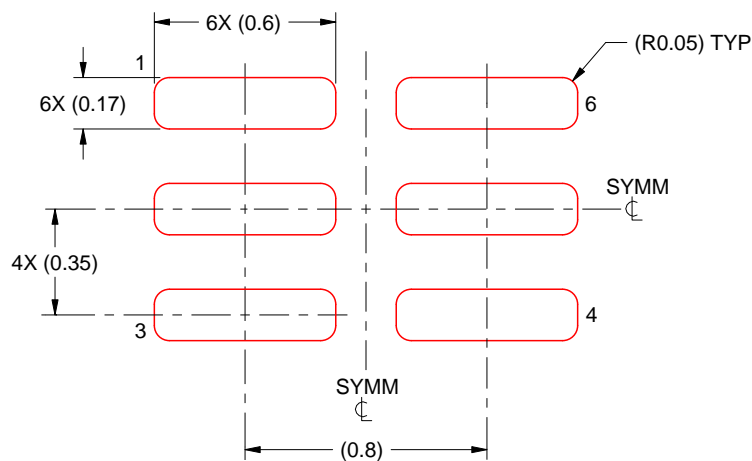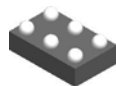
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A   06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

B |← E →| A

BALL A1
CORNER

D

0.5 MAX

C

SEATING PLANE

0.19
0.15

BALL TYP

⌒ 0.05 C

0.5 TYP

C

SYMM
₵

B

1
TYP

0.5
TYP

A

D: Max = 1.418 mm, Min =1.357 mm

E: Max = 0.918 mm, Min =0.857 mm

1          2

6X ⌀ 0.25
0.21

SYMM
₵

⊕ 0.015Ⓢ C AⓈ BⓈ

4219524/A   06/2014

NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

6X (∅ 0.225)

(0.5) TYP

(0.5) TYP

1    2

A

B    SYMM ℄

C

SYMM ℄

**LAND PATTERN EXAMPLE**
SCALE:40X

(∅ 0.225)
METAL

0.05 MAX

SOLDER MASK
OPENING

**NON-SOLDER MASK
DEFINED
(PREFERRED)**

0.05 MIN

METAL
UNDER
MASK

(∅ 0.225)
SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**

**SOLDER MASK DETAILS**
NOT TO SCALE

4219524/A   06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

(0.5) TYP

6X (□ 0.25)

1    2    (R0.05) TYP

A

(0.5)
TYP

B    SYMM ₵

METAL
TYP

C

SYMM
₵

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A   06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# 重要声明和免责声明