STP16N60M2, STU16N60M2

N-channel 600 V, 0.28 Ω typ., 12 A MDmesh™ M2 Power MOSFET in TO-220 and IPAK packages

Datasheet - production data

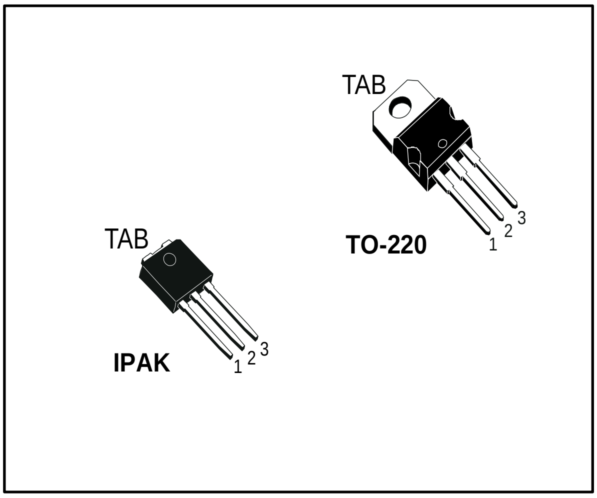
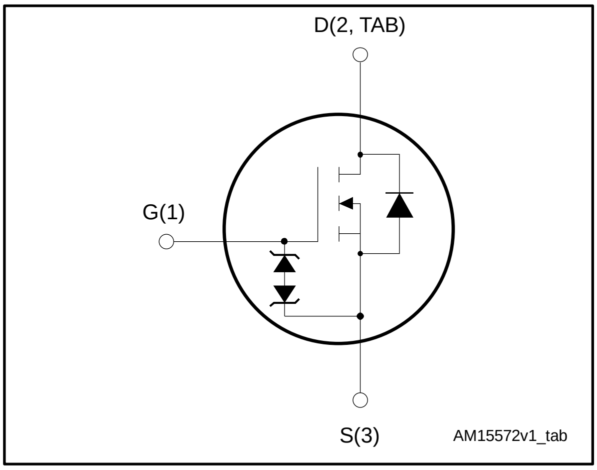


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP16N60M2	600 V	0.32 Ω	12 A
STU16N60M2			

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP16N60M2	16N60M2	TO-220	Tube
STU16N60M2		IPAK	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	12	A
I_D	Drain current (continuous) at T_C= 100 °C	7.6	A
I_{DM}(1)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3).	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

Notes:

(1) Pulse width limited by safe operating area.

(2) I_{SD} ≤ 12 A, di/dt ≤ 400 A/µs; $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

(3) V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value		Unit
		TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max.	1.14		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max.	62.5	100	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	2.9	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	130	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		0.28	0.32	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	700	-	pF
C_{oss}	Output capacitance		-	38	-	pF
C_{rss}	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	140	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.3	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 12 A, V_{GS} = 10 V (see *Figure 17: "Gate charge test circuit"*)	-	19	-	nC
Q_{gs}	Gate-source charge		-	3.3	-	nC
Q_{gd}	Gate-drain charge		-	9.5	-	nC

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16: "Switching times test circuit for resistive load"* and *Figure 21: "Switching time waveform"*)	-	10.5	-	ns
t_r	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	58	-	ns
t_f	Fall time		-	18.5	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM} (1)	Source-drain current (pulsed)		-		48	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 12 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	316		ns
Q_{rr}	Reverse recovery charge		-	3.25		µC
I_{RRM}	Reverse recovery current		-	20.5		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	454		ns
Q_{rr}	Reverse recovery charge		-	4.8		µC
I_{RRM}	Reverse recovery current		-	21		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: TO-220 safe operating area

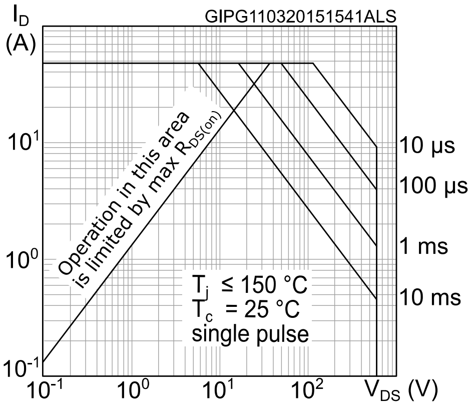


Figure 3: TO-220 thermal impedance

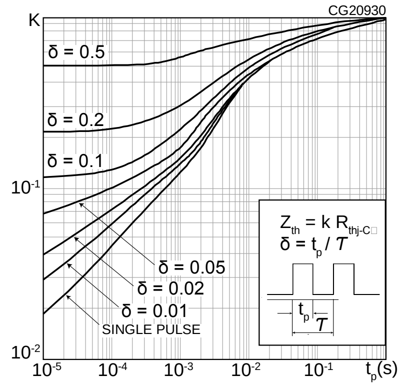


Figure 4: IPAK safe operating area

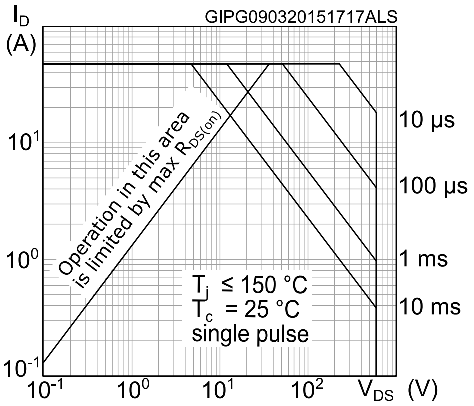


Figure 5: IPAK thermal impedance

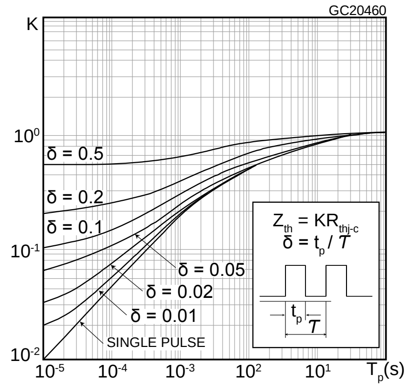


Figure 6: Output characteristics

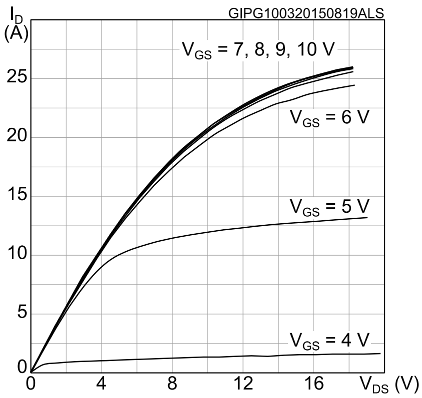


Figure 7: Transfer characteristics

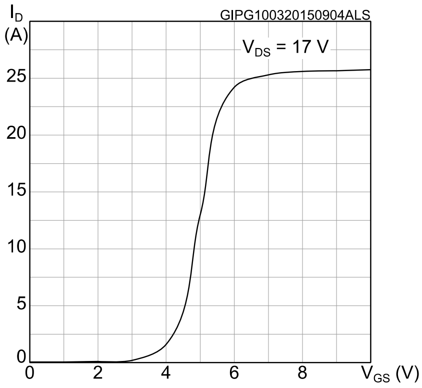


Figure 8: Normalized gate threshold voltage vs. temperature

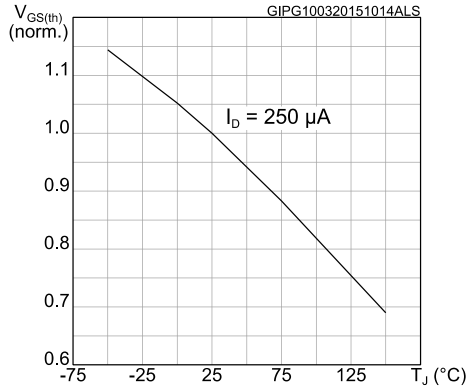


Figure 9: Normalized V(BR)DSS vs. temperature

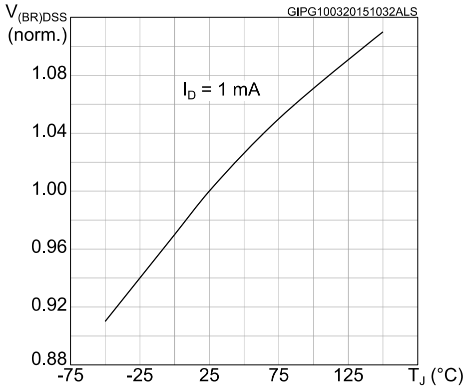


Figure 10: Static drain-source on-resistance

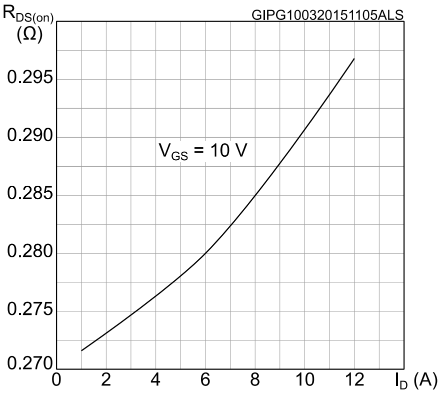


Figure 11: Normalized on-resistance vs. temperature

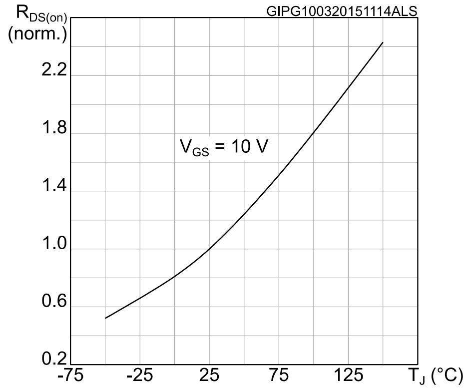


Figure 12: Gate charge vs. gate-source voltage

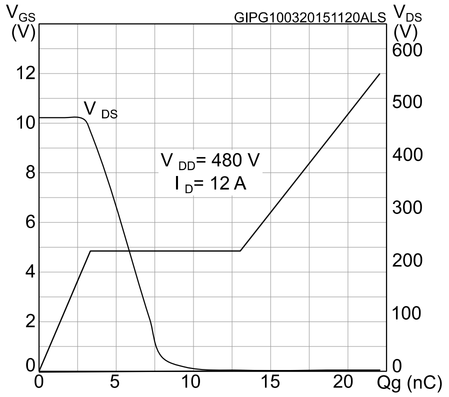


Figure 13: Capacitance variations

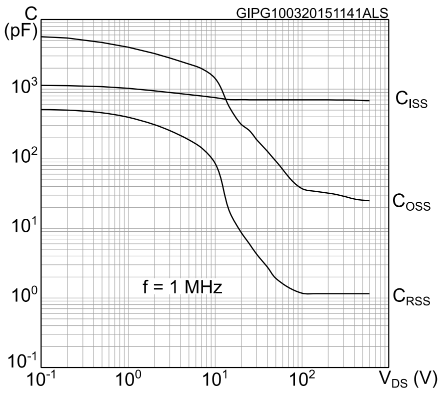


Figure 14: Output capacitance stored energy

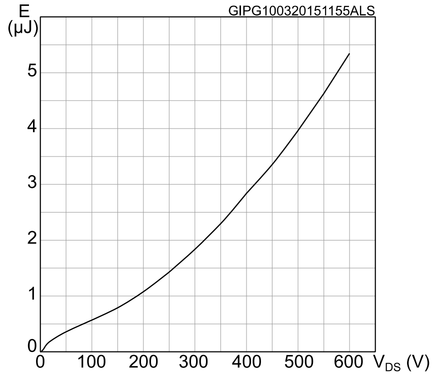
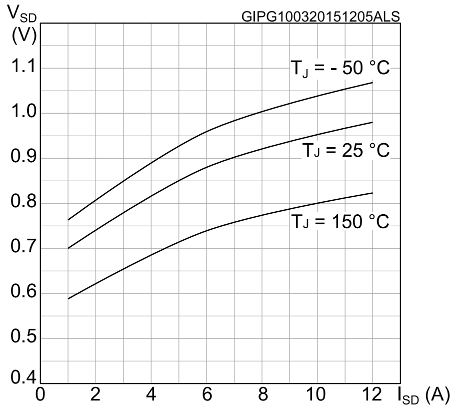


Figure 15: Source- drain diode forward characteristics



3 Test circuits

Figure 16: Switching times test circuit for resistive load

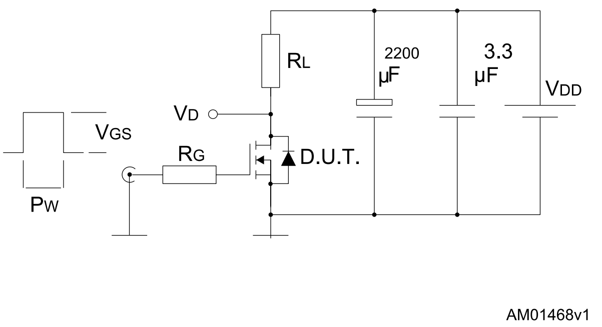


Figure 17: Gate charge test circuit

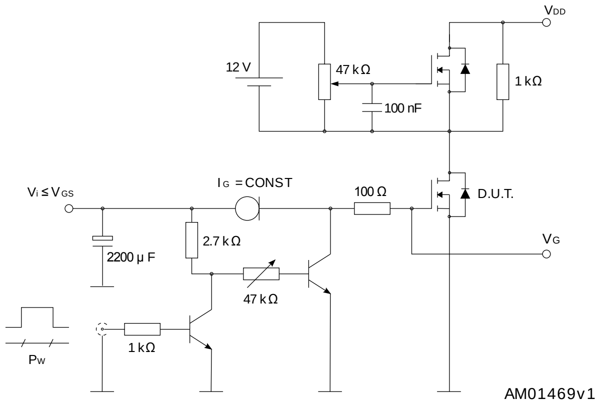


Figure 18: Test circuit for inductive load switching and diode recovery times

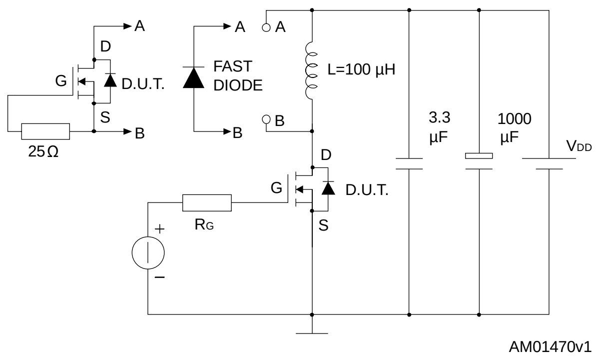


Figure 19: Unclamped inductive load test circuit

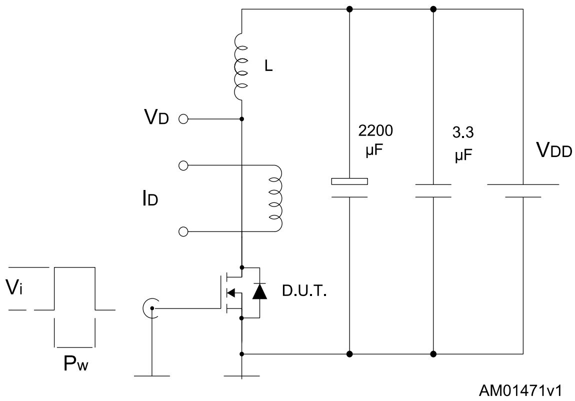


Figure 20: Unclamped inductive waveform

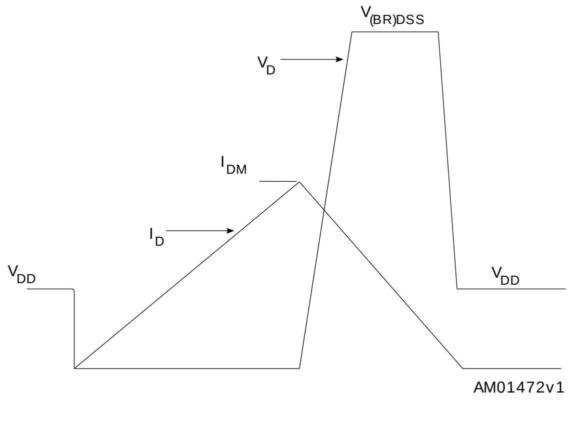
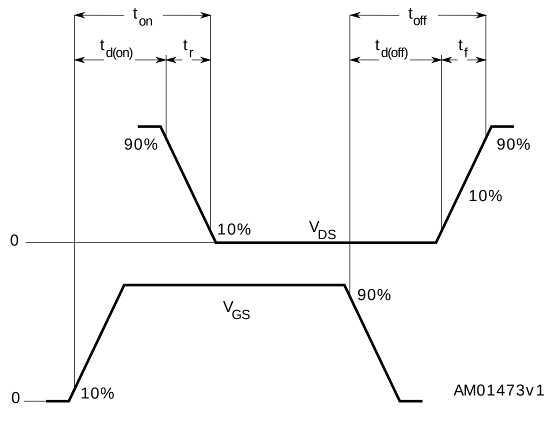


Figure 21: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 22: TO-220 type A package outline

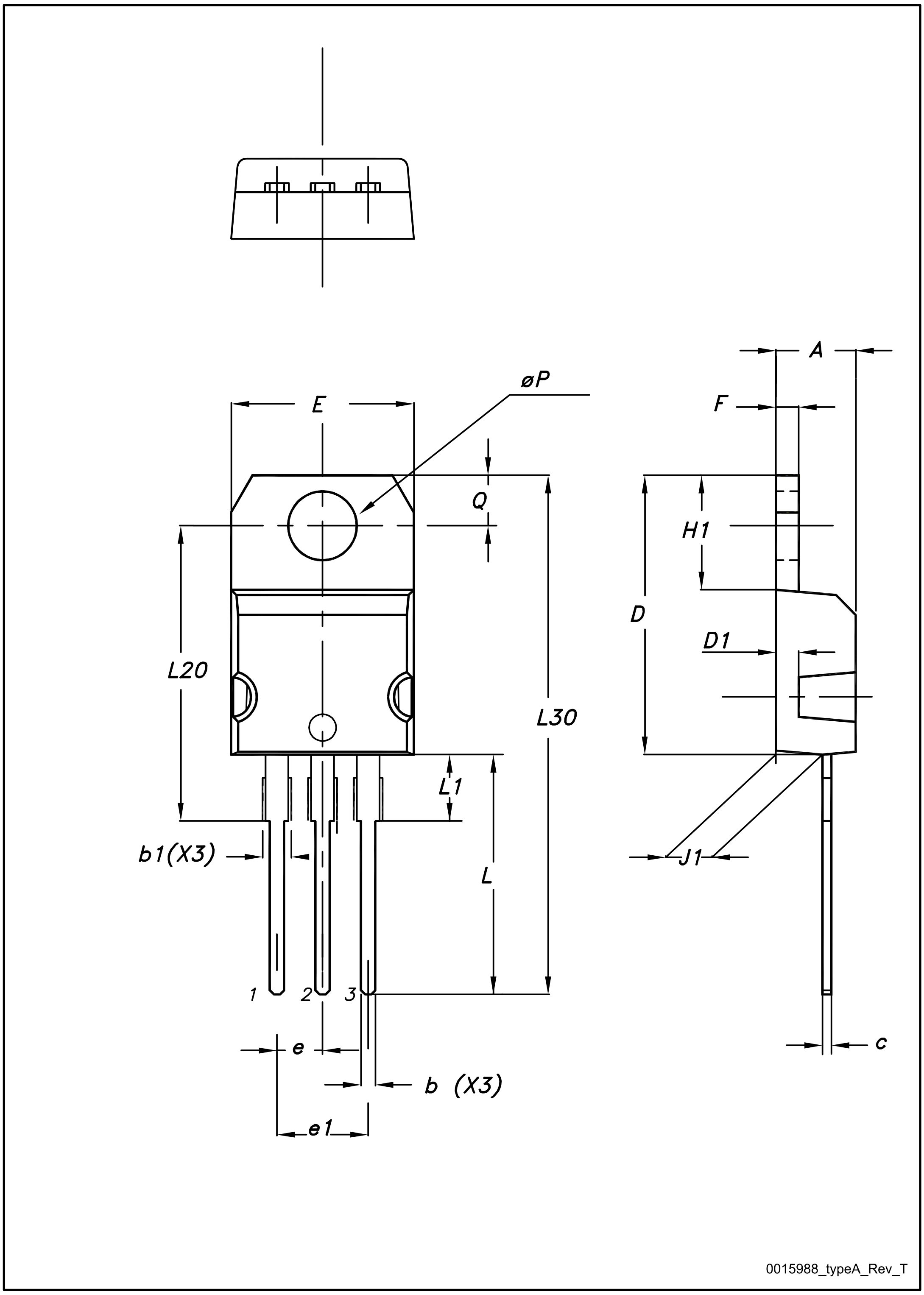


Table 9: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.2 IPAK (TO-251) Type A package information

Figure 23: IPAK (TO-251) type A drawing

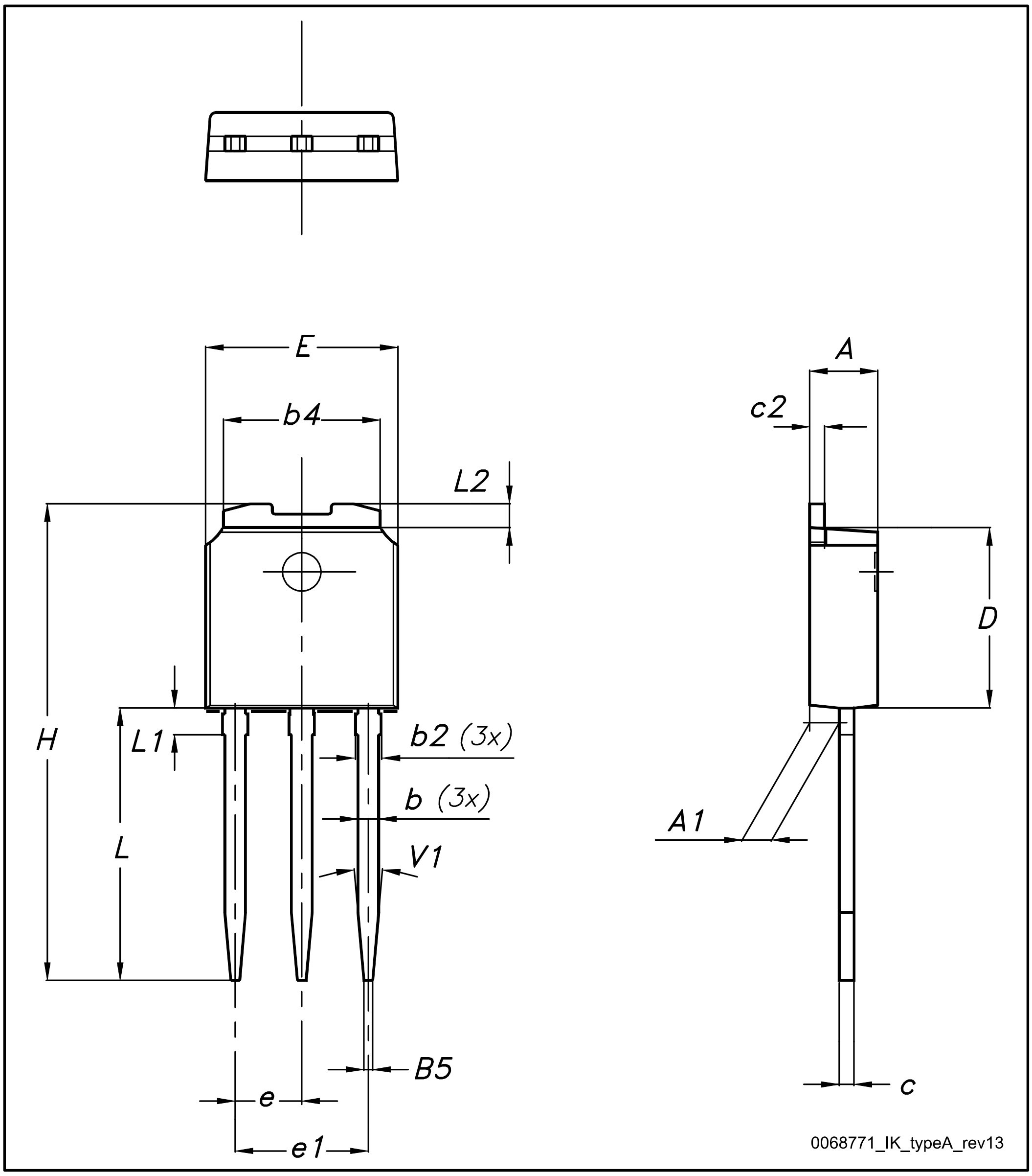


Table 10: IPAK (TO-251) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
11-Mar-2015	1	Initial release.