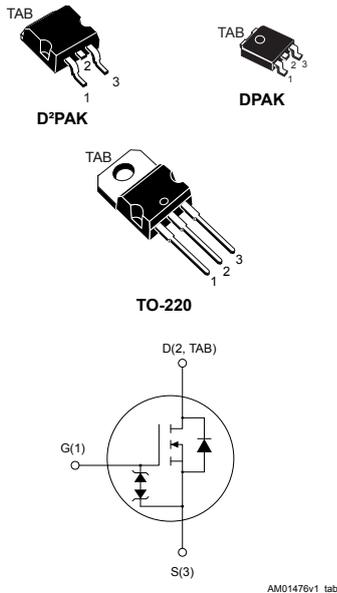


N-channel 600 V, 0.55 Ω typ., 7.5 A MDmesh M2 Power MOSFET in a D²PAK, DPAK and TO-220 packages



Features

Order codes	V_{DS} @ T_J max.	$R_{DS(on)}$ max.	I_D	Package
STB10N60M2	650 V	0.60 Ω	7.5 A	D ² PAK
STD10N60M2				DPAK
STP10N60M2				TO-220

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the MDmesh M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters.



Product status links

[STB10N60M2](#)
[STD10N60M2](#)
[STP10N60M2](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	7.5	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4.9	
$I_{DM}^{(1)}$	Drain current (pulsed)	30	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	85	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse limited by safe operating area.
2. $I_{SD} \leq 7.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	DPAK	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	1.47			$^\circ\text{C}/\text{W}$
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	30	50		$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient			62.5	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	1.5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	110	mJ

1. Pulse width limited by T_J max.
2. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$		0.55	0.60	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	400	-	pF
C_{oss}	Output capacitance		-	22	-	pF
C_{rSS}	Reverse transfer capacitance		-	0.84	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	83	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	6.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 7.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 16. Test circuit for gate charge behavior)	-	13.5	-	nC
Q_{gs}	Gate-source charge		-	2.1	-	nC
Q_{gd}	Gate-drain charge		-	7.2	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 3.75\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	8.8	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	32.5	-	ns
t_f	Fall time		-	13.2	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		30	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 7.5\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 7.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	270		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	2		μC
I_{RRM}	Reverse recovery current	(see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	14.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 7.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	376		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	2.8		μC
I_{RRM}	Reverse recovery current	(see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	15		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

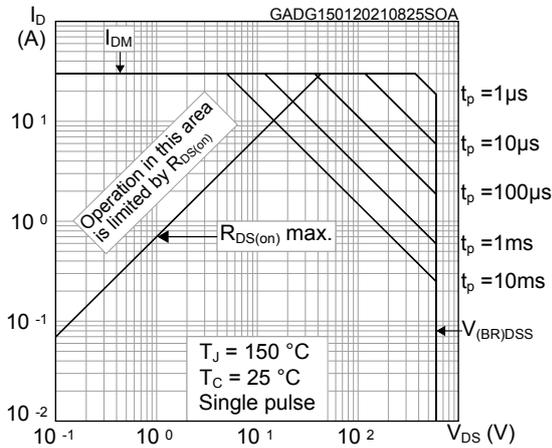
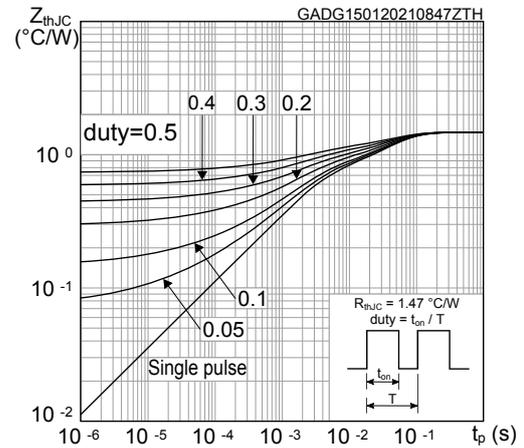
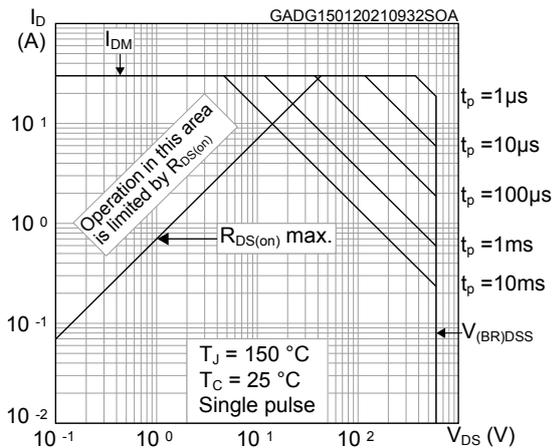
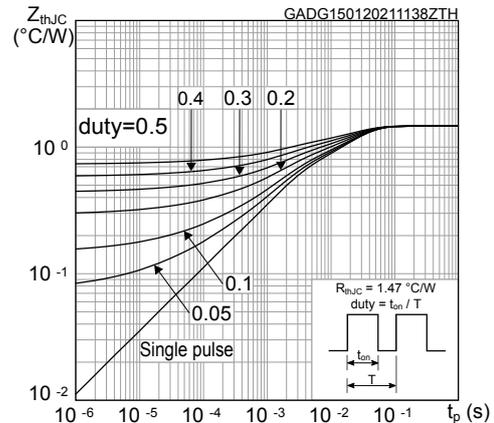
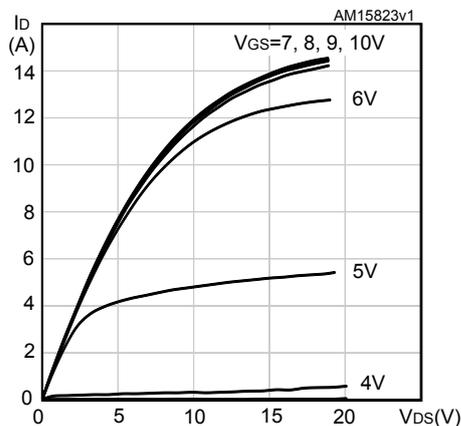
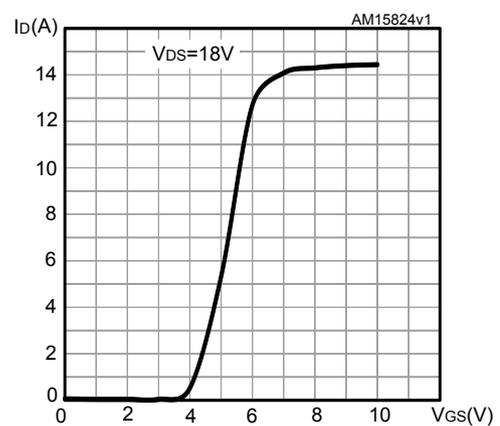
2.1 Electrical characteristics (curves)
Figure 1. Safe operating area for D²PAK and TO-220

Figure 2. Maximum transient thermal impedance for D²PAK and TO-220

Figure 3. Safe operating area for DPAK

Figure 4. Maximum transient thermal impedance for DPAK

Figure 5. Output characteristics

Figure 6. Transfer characteristics


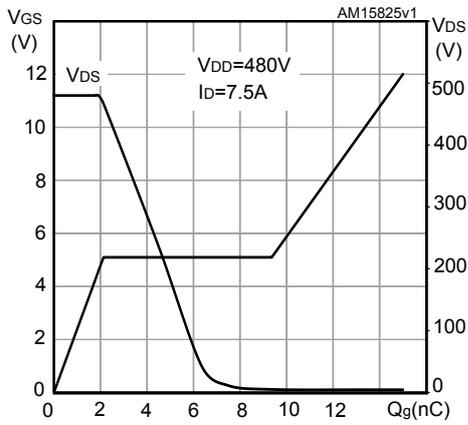
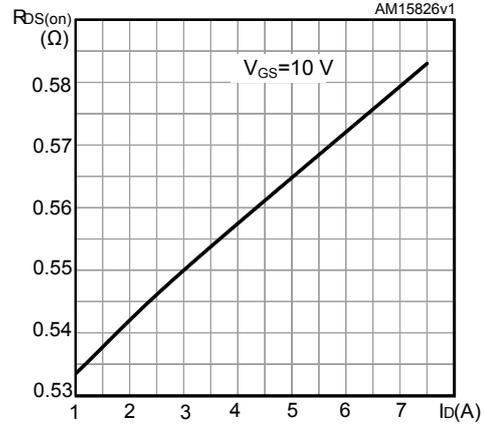
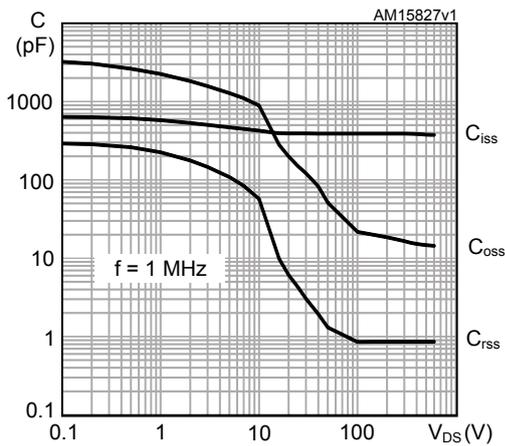
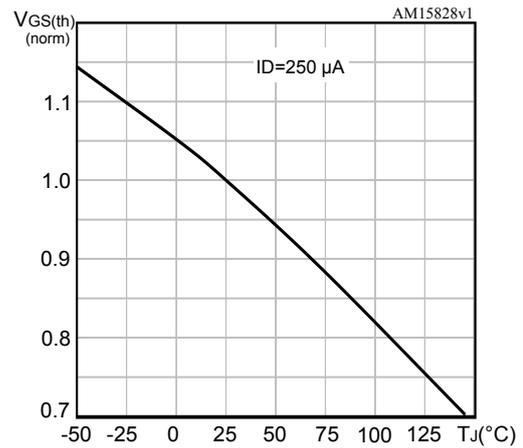
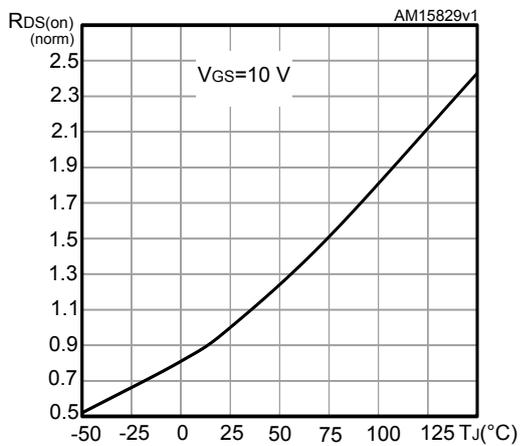
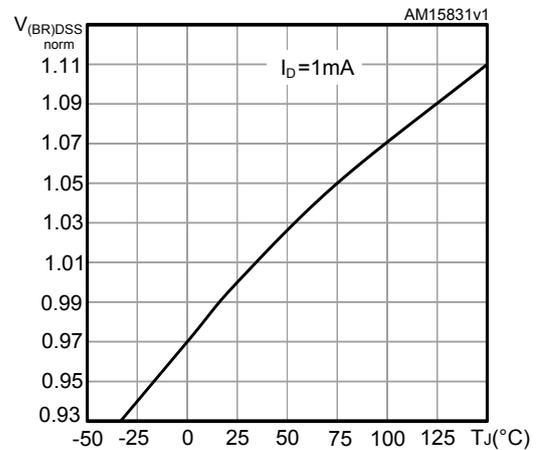
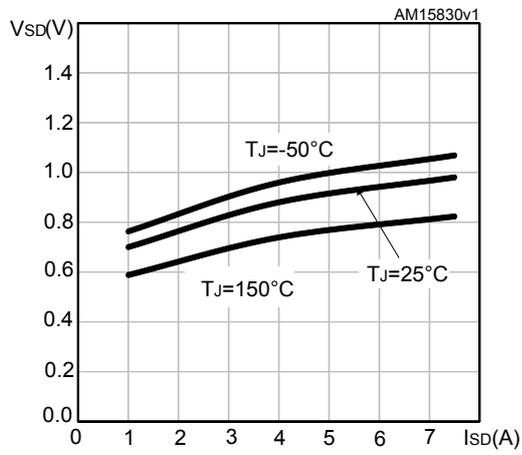
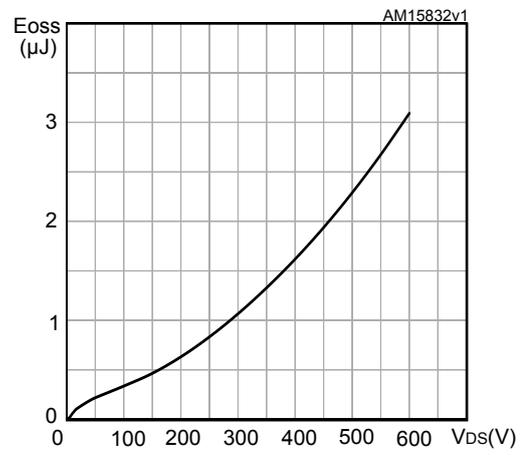
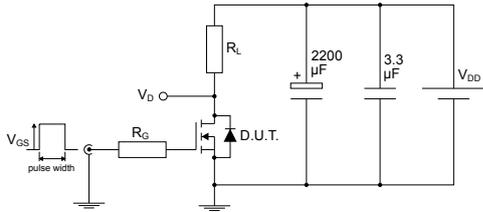
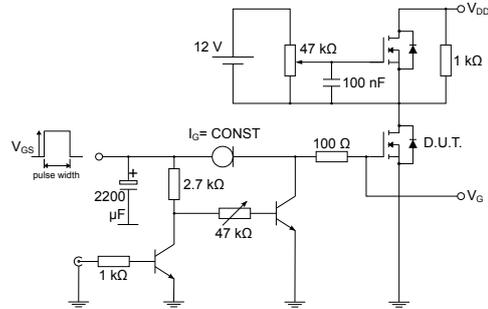
Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on-resistance

Figure 9. Capacitance variations

Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature

Figure 12. Normalized V(BR)DSS vs temperature


Figure 13. Source-drain diode forward characteristics

Figure 14. Output capacitance stored energy


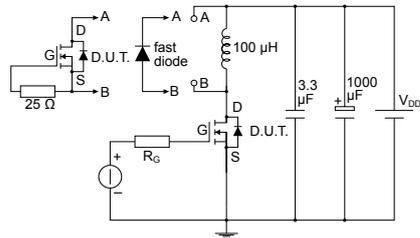
3 Test circuits

Figure 15. Test circuit for resistive load switching times


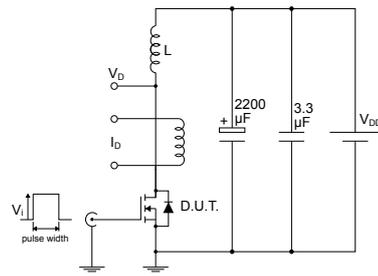
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Figure 16. Test circuit for gate charge behavior


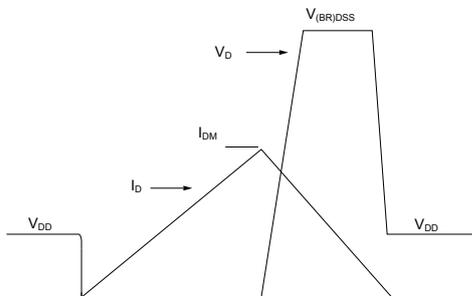
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Figure 17. Test circuit for inductive load switching and diode recovery times


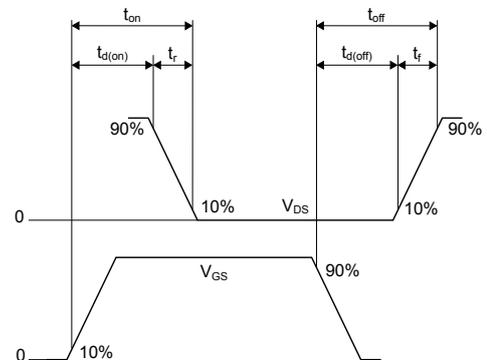
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Figure 18. Unclamped inductive load test circuit


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Figure 19. Unclamped inductive waveform


AM01472v1

Figure 20. Switching time waveform


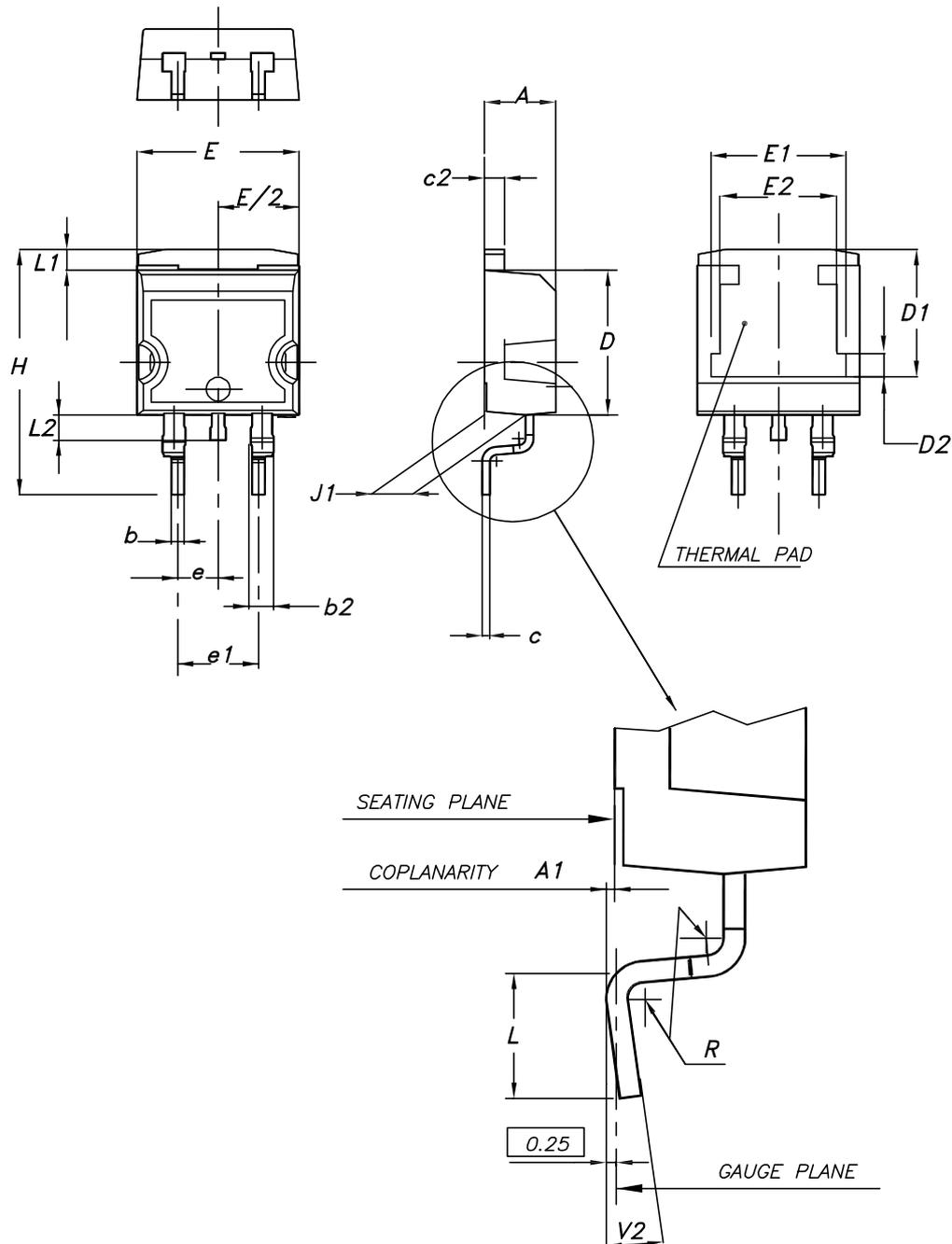
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 21. D²PAK (TO-263) type A package outline

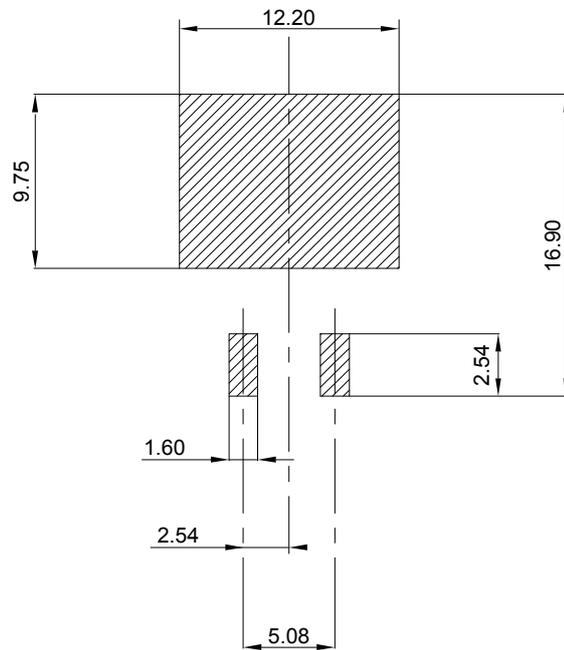


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Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

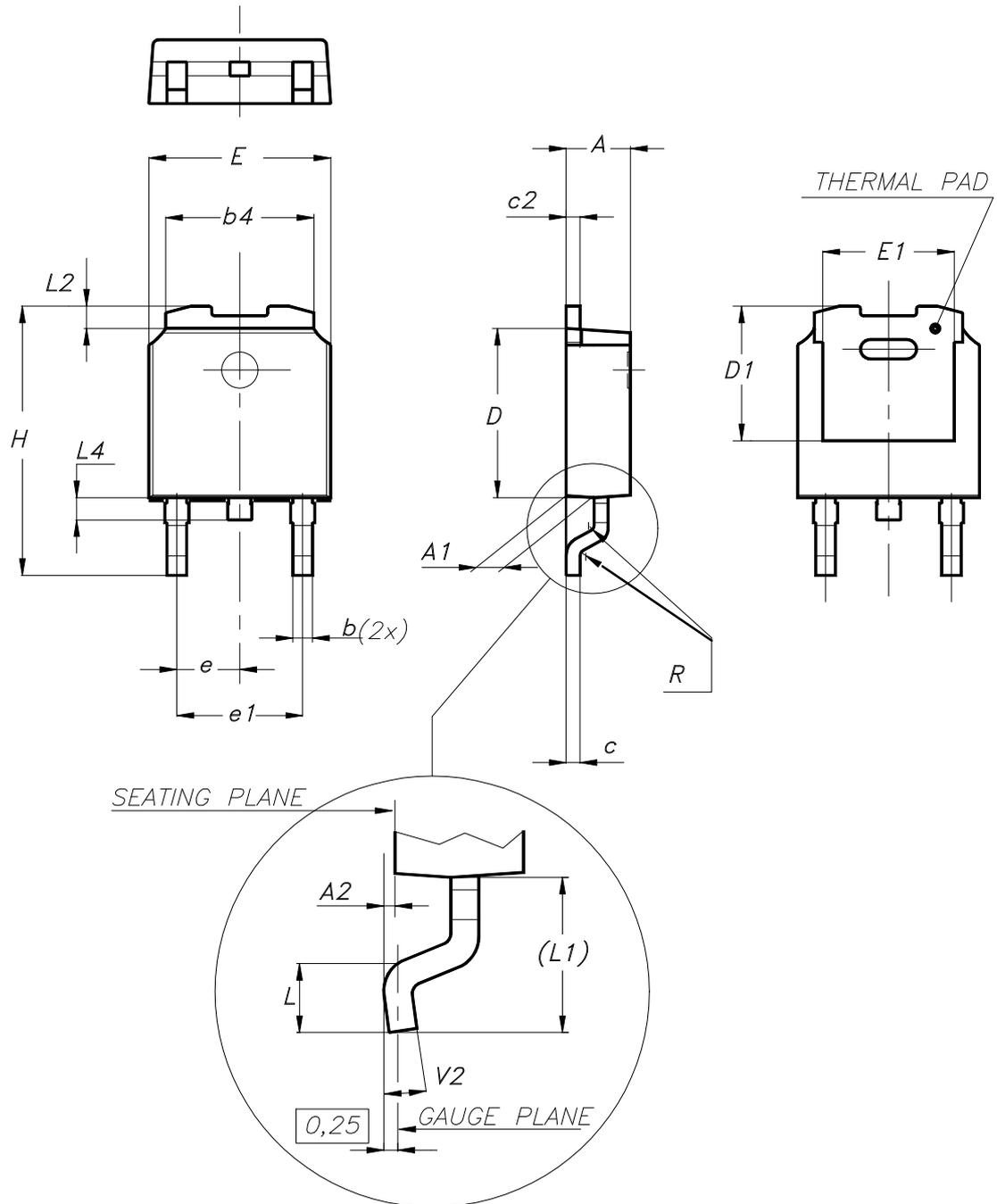
Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint_26

4.2 DPAK (TO-252) type A package information

Figure 23. DPAK (TO-252) type A package outline



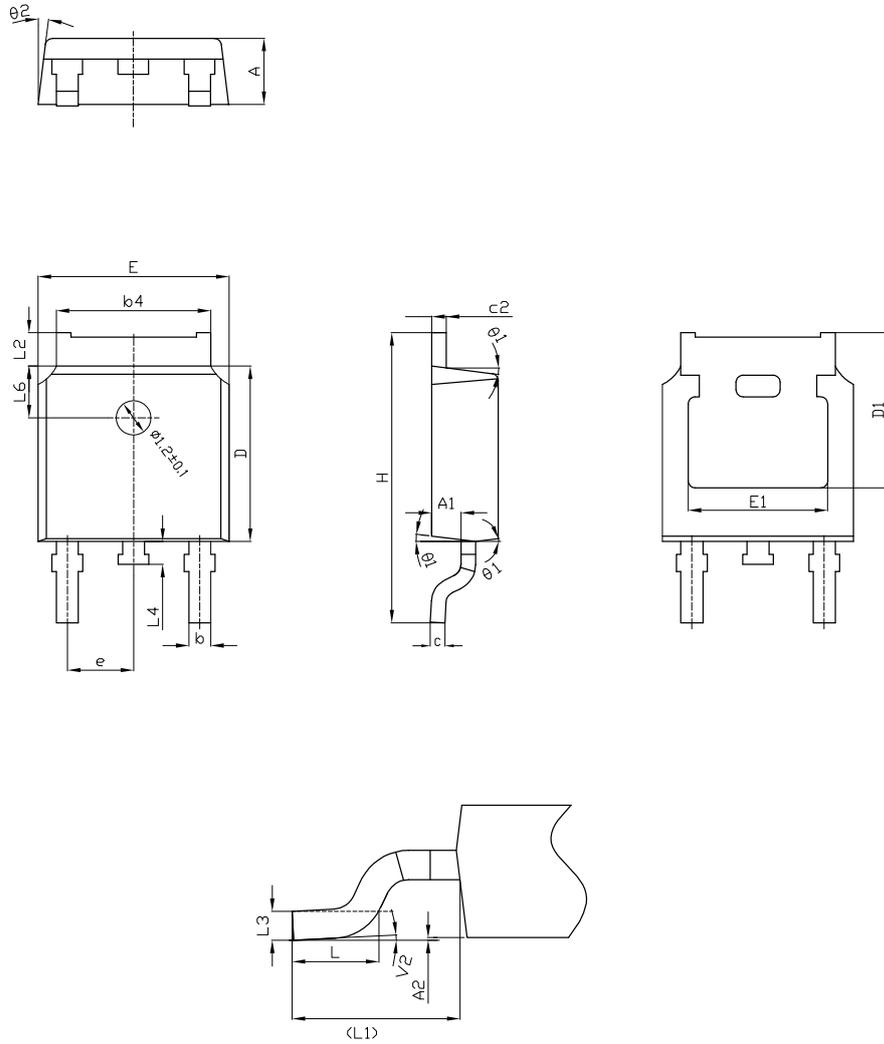
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Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.3 DPAK (TO-252) type C package information

Figure 24. DPAK (TO-252) type C package outline



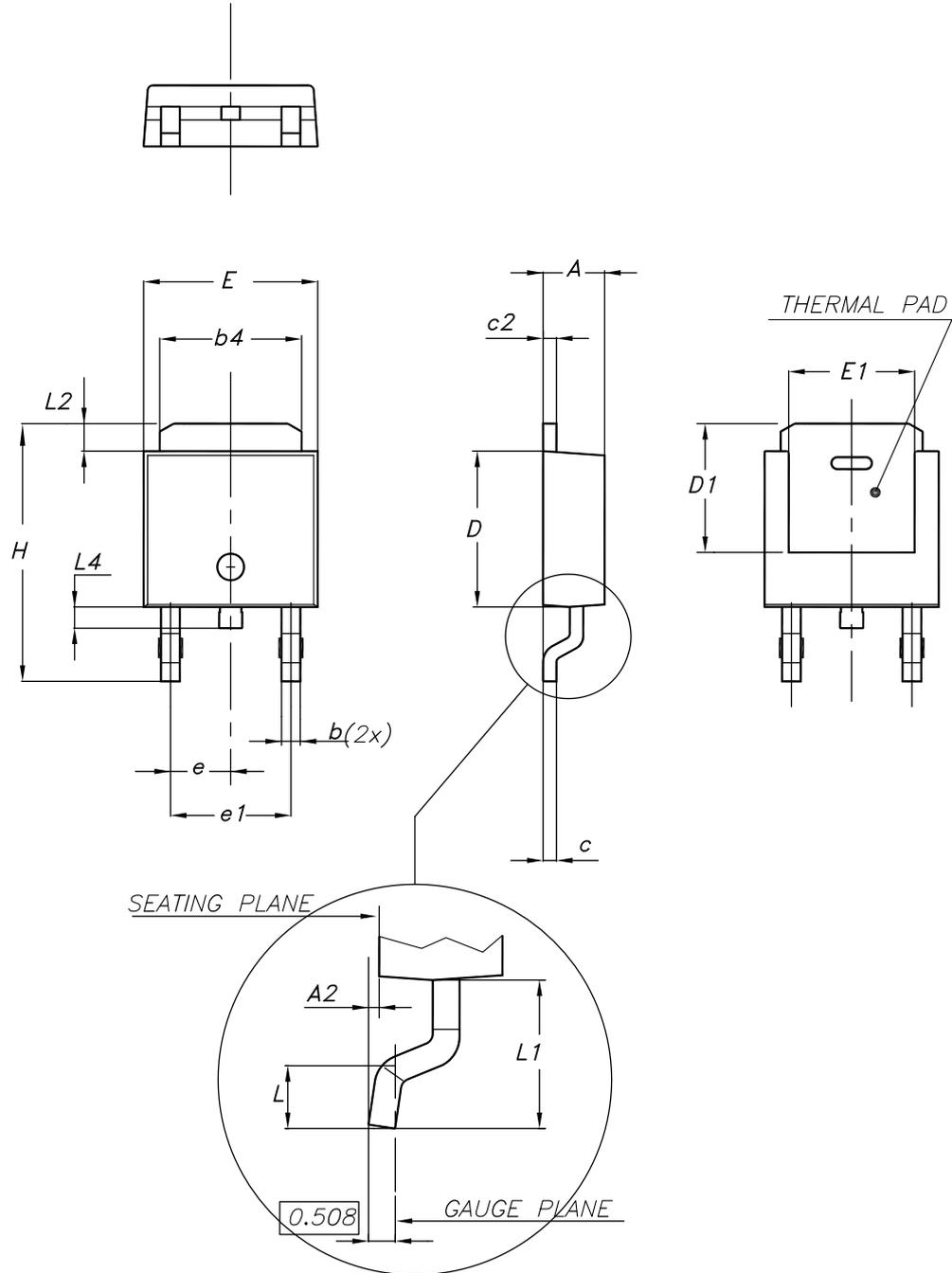
0068772_C_30

Table 10. DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

4.4 DPAK (TO-252) type E package information

Figure 25. DPAK (TO-252) type E package outline

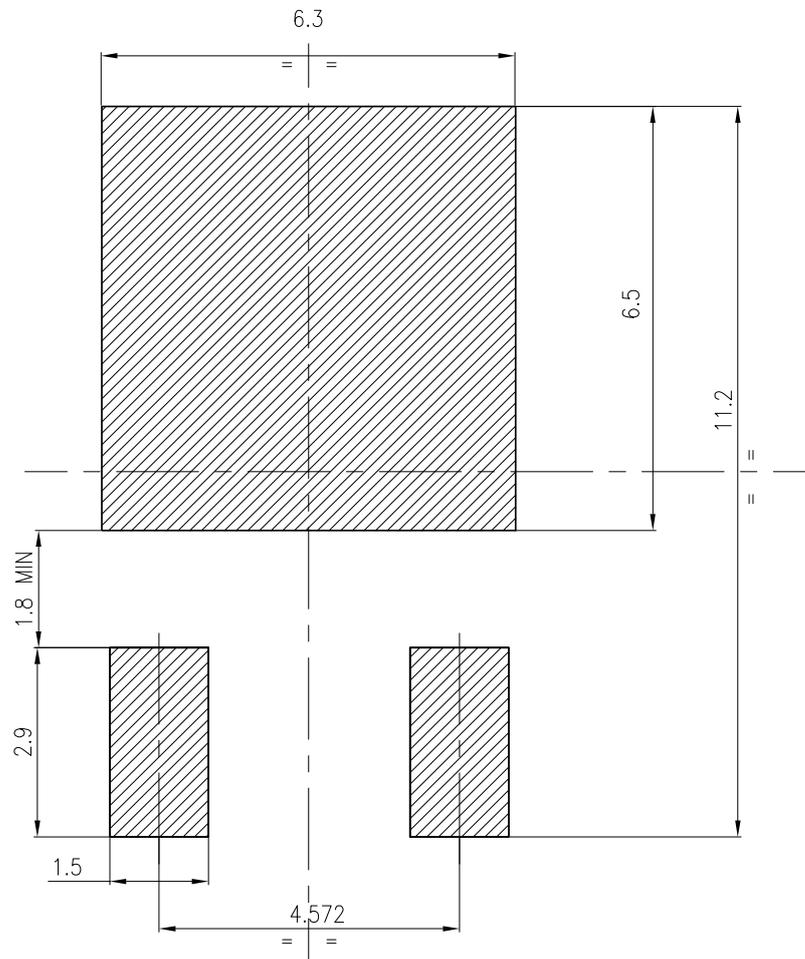


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Table 11. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

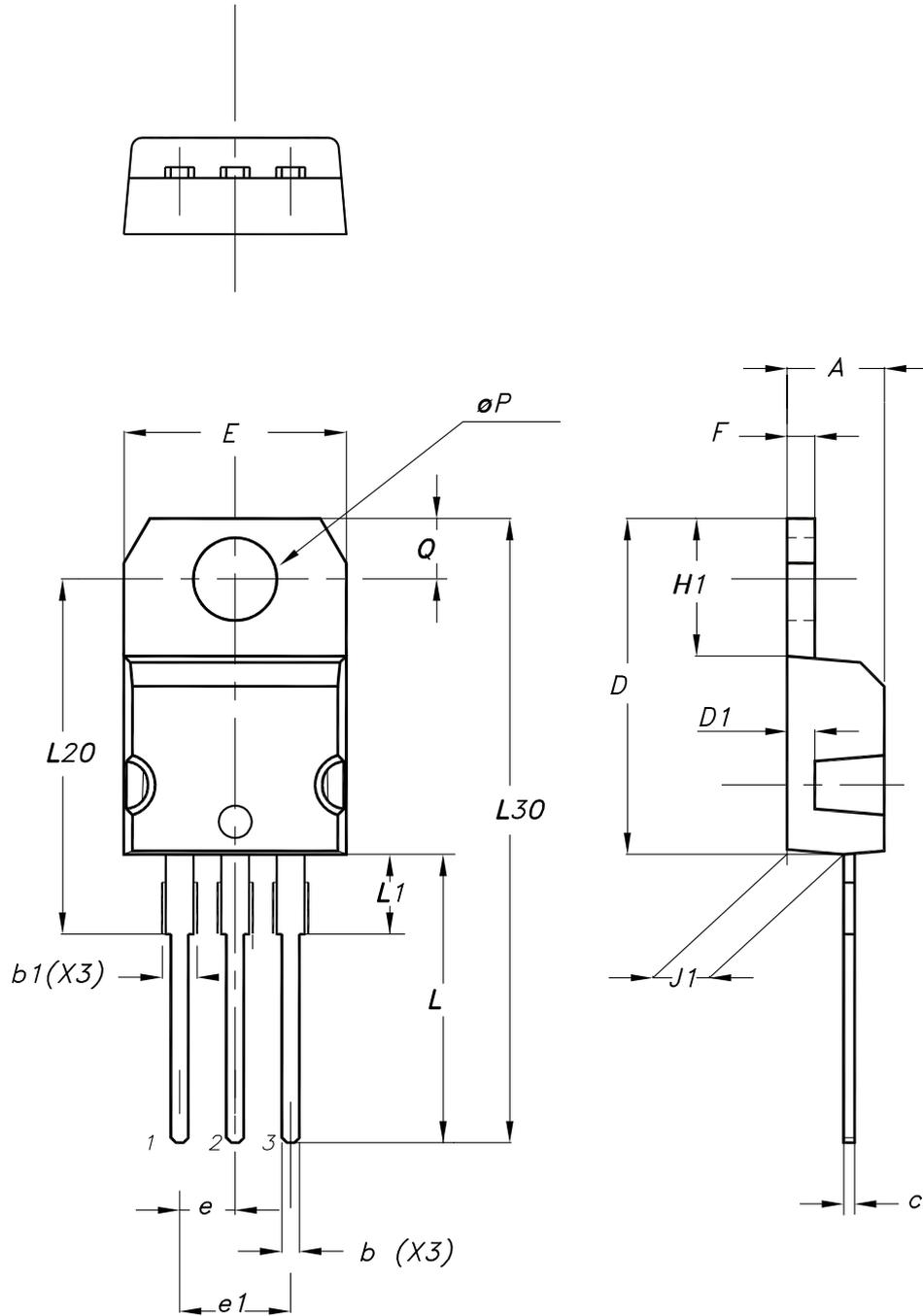
Figure 26. DPAK (TO-252) recommended footprint (dimensions are in mm)



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4.5 TO-220 type A package information

Figure 27. TO-220 type A package outline



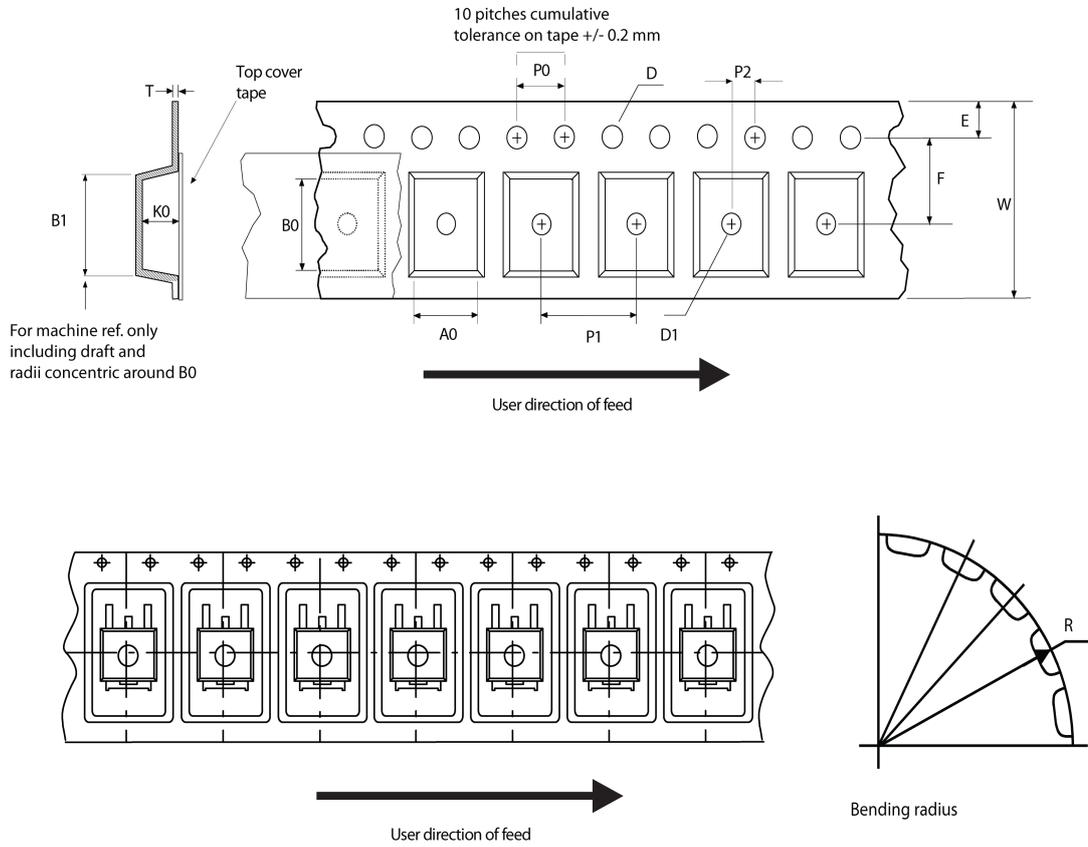
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Table 12. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

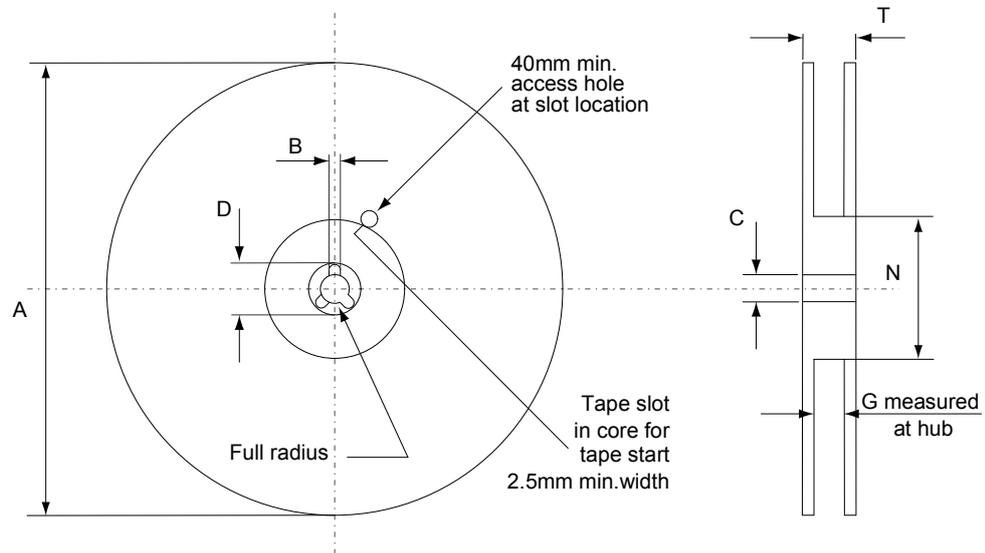
4.6 D²PAK and DPAK packing information

Figure 28. Tape outline



AM08852v1

Figure 29. Reel outline



AM06038v1

Table 13. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 14. DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Order codes

Table 15. Device summary

Order code	Marking	Package	Packing
STB10N60M2	10N60M2	D ² PAK	Tape and reel
STD10N60M2		DPAK	
STP10N60M2		TO-220	Tube

Revision history

Table 16. Document revision history

Date	Version	Changes
29-May-2013	1	First release.
06-Dec-2013	2	<ul style="list-style-type: none"> – Added: D²PAK package – Modified: title and $R_{DS(on)}$ values in cover page – Modified: $R_{DS(on)}$ values in <i>Table 5</i> – Modified: R_G value in <i>Table 6</i> – Modified: <i>Figure 9</i> and I_D value in <i>Figure 12</i> – Added: <i>Table 9, 13, Figure 22</i> and <i>23</i> – Updated: <i>Table 10, 11, Figure 24, 25</i> and <i>26</i> Minor text changes.
08-Mar-2017	3	Updated the title and the description in cover page. Updated <i>Table 4: "Avalanche characteristics"</i> . Updated <i>Section 4.2: "DPAK (TO-252) type A package information"</i> . Added <i>Section 4.4: "DPAK (TO-252) type E package information"</i> , and <i>Section 4.7: "IPAK (TO-251) type C package information"</i> . Minor text changes.
19-Jan-2021	4	The part number STU10N60M2 have been removed and the document has been updated accordingly. Updated <i>Figure 1. Safe operating area for D²PAK and TO-220</i> , <i>Figure 2. Maximum transient thermal impedance for D²PAK and TO-220</i> , <i>Figure 3. Safe operating area for DPAK and Figure 4. Maximum transient thermal impedance for DPAK</i> . Minor text changes.

Contents

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3	Test circuits	8
4	Package information	9
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