STL36N55M5

N-channel 550 V, 0.066 Ω typ., 22.5 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet — production data

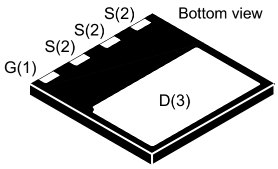
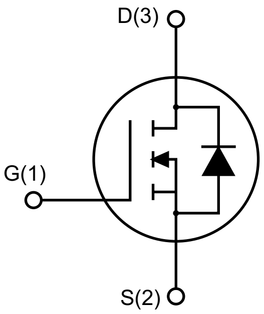


Figure 1. Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STL36N55M5	600 V	0.090 Ω	22.5 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input
- capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL36N55M5	36N55M5	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	550	V
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	22.5	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	17	A
I_{DM} (1),(2)	Drain current (pulsed)	90	A
I_D(3)	Drain current (continuous) at T_{amb} = 25 °C	3.7	A
I_D(3)	Drain current (continuous) at T_{amb} = 100 °C	2.2	A
P_{TOT} (3)	Total dissipation at T_{amb} = 25 °C	2.8	W
P_{TOT} (1)	Total dissipation at T_C = 25 °C	150	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\ max}$)	7	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	510	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj-case}$ and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch², 2 oz Cu.
4. $I_{SD} \leq$ 22.5 A, di/dt $\leq$ 400 A/µs, $V_{Peak} < V_{(BR)DSS}$, V_{DD} = 340 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	°C/W
$R_{thj-amb}$(1)	Thermal resistance junction-ambient max	45	°C/W

1. When mounted on FR-4 board of inch², 2 oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	550			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 550 V			1	µA
		V_{DS} = 550 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 16.5 A		0.066	0.090	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	2670	-	pF
C_{oss}	Output capacitance		-	75	-	pF
C_{rss}	Reverse transfer capacitance		-	6.6	-	pF
$C_{o(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 440 V	-	71	-	pF
$C_{o(tr)}$ (2)	Equivalent output capacitance time related		-	192	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.85	-	Ω
Q_g	Total gate charge	V_{DD} = 440 V, I_D = 16.5 A, V_{GS} = 10 V (see *Figure 16*)	-	62	-	nC
Q_{gs}	Gate-source charge		-	15	-	nC
Q_{gd}	Gate-drain charge		-	27	-	nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(V)}$	Voltage delay time	V_{DD} = 400 V, I_D = 22 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 20*)	-	56	-	ns
$t_{r(V)}$	Voltage rise time		-	13	-	ns
$t_{f(i)}$	Current fall time		-	13	-	ns
$t_{c(off)}$	Crossing time		-	17	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		22.5	A
I_{SDM}(1),(2)	Source-drain current (pulsed)		-		90	A
V_{SD} (3)	Forward on voltage	I_{SD} = 22.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 22.5 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 17*)	-	292		ns
Q_{rr}	Reverse recovery charge		-	4.2		µC
I_{RRM}	Reverse recovery current		-	29		A
t_{rr}	Reverse recovery time	I_{SD} = 22.5 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 17*)	-	364		ns
Q_{rr}	Reverse recovery charge		-	6		µC
I_{RRM}	Reverse recovery current		-	33		A

1. The value is rated according to $R_{thj\text{-}case}$ and limited by package.
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

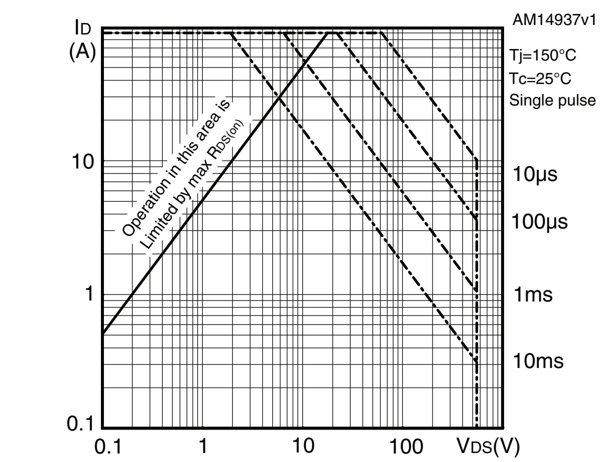


Figure 3. Thermal impedance

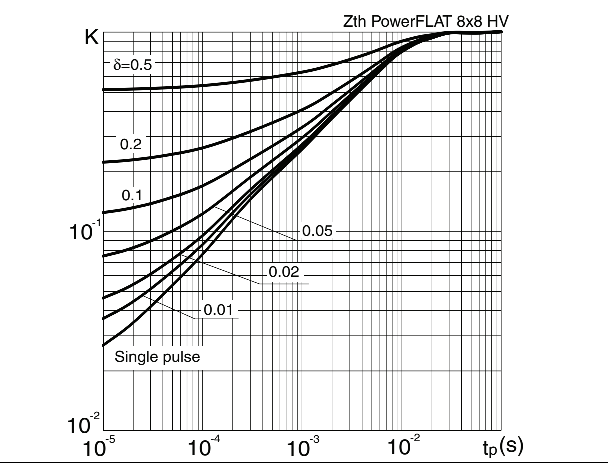


Figure 4. Output characteristics

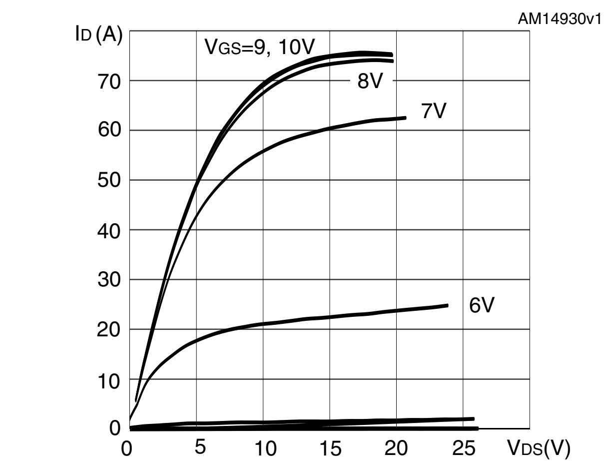


Figure 5. Transfer characteristics

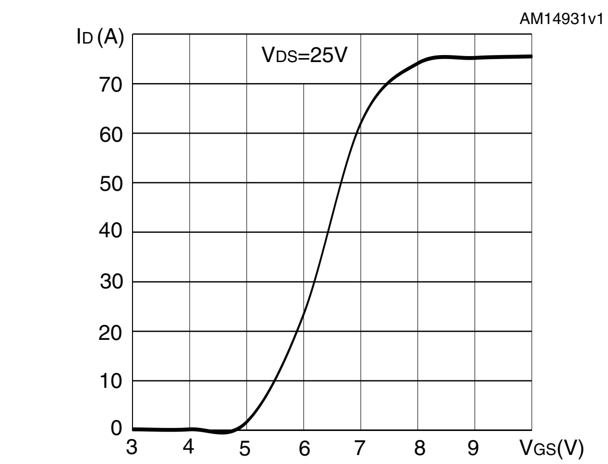


Figure 6. Gate charge vs gate-source voltage

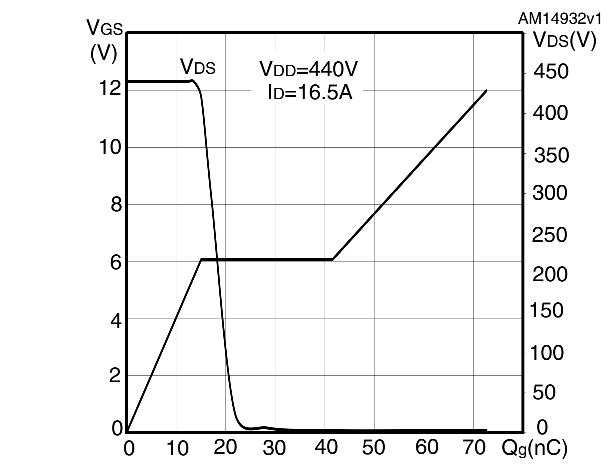


Figure 7. Static drain-source on-resistance

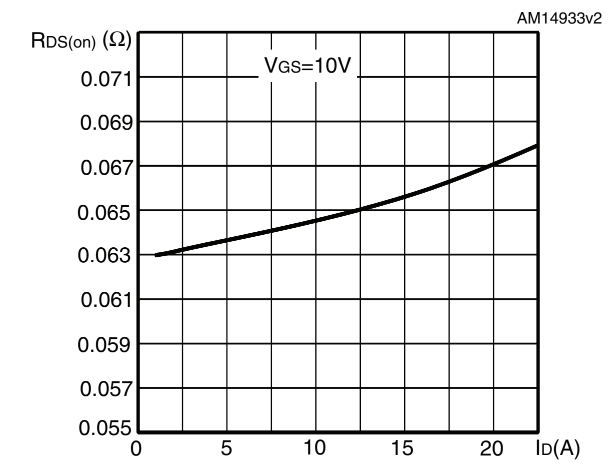


Figure 8. Capacitance variations

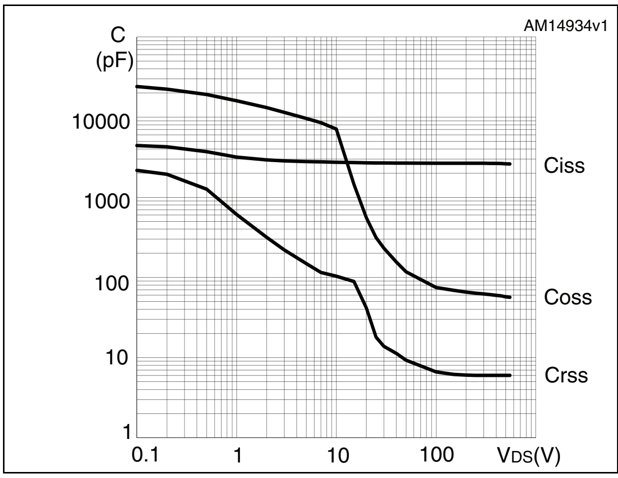


Figure 9. Output capacitance stored energy

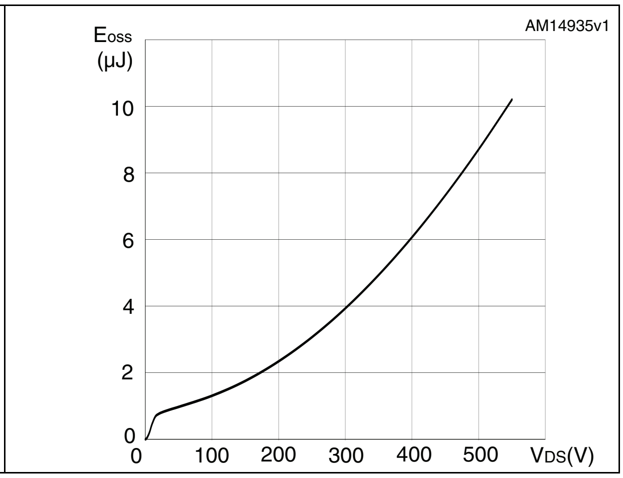


Figure 10. Normalized gate threshold voltage vs temperature

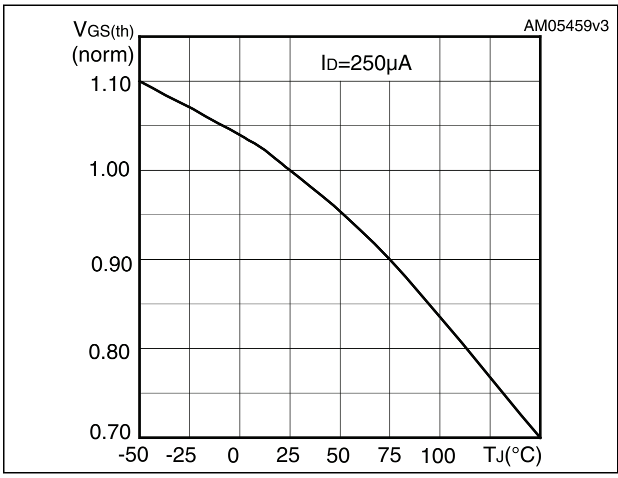


Figure 11. Normalized on-resistance vs temperature

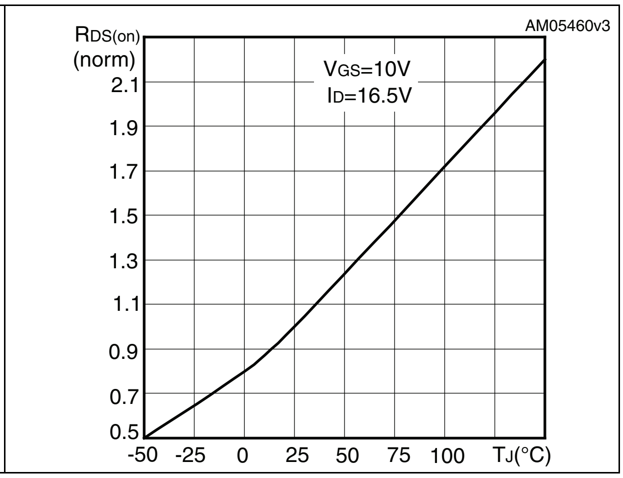


Figure 12. Source-drain diode forward characteristics

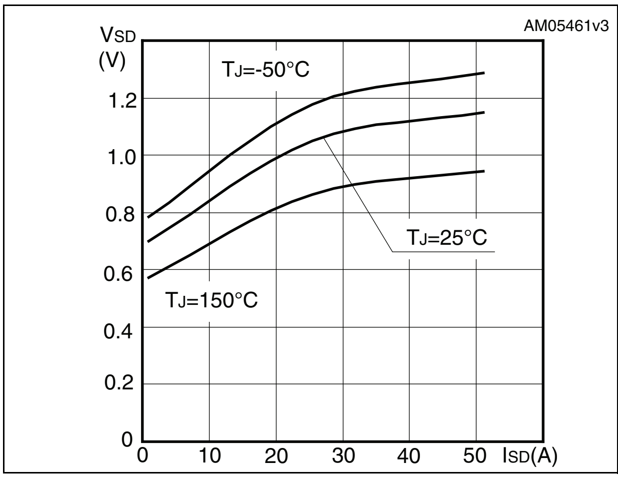


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

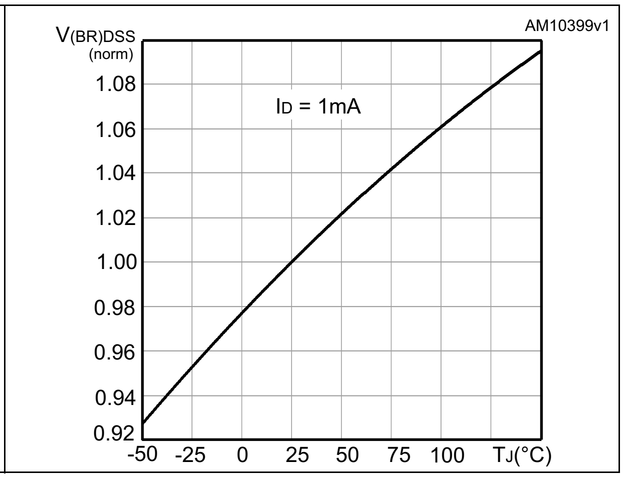
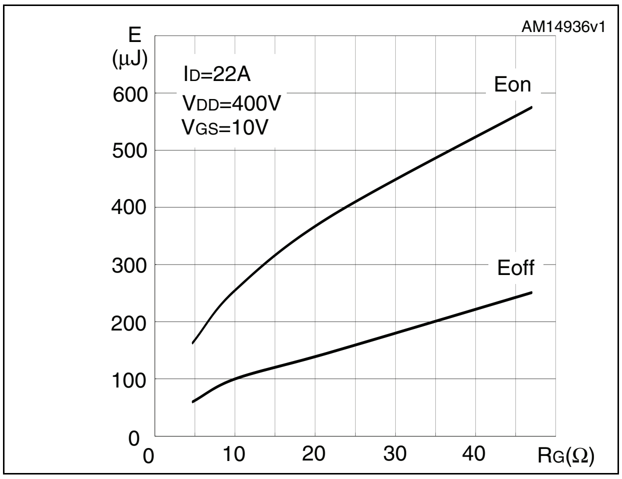


Figure 14. Switching losses vs gate resistance (1)



1. Eon including reverse recovery of a SiC diode.

3 Test circuits

Figure 15. Switching times test circuit for resistive load

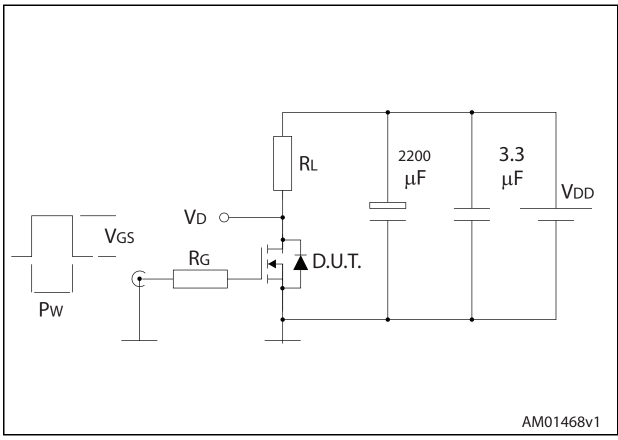


Figure 16. Gate charge test circuit

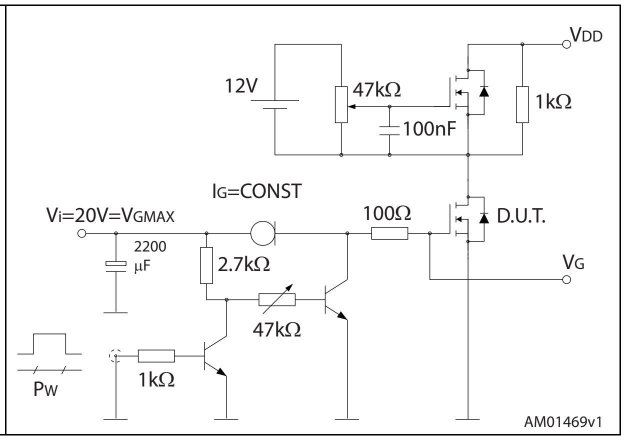


Figure 17. Test circuit for inductive load switching and diode recovery times

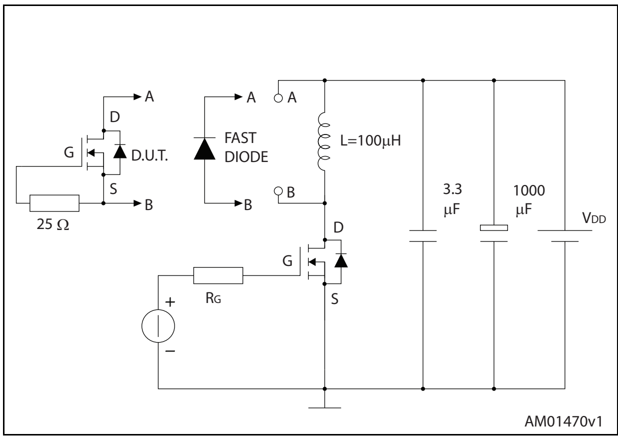


Figure 18. Unclamped inductive load test circuit

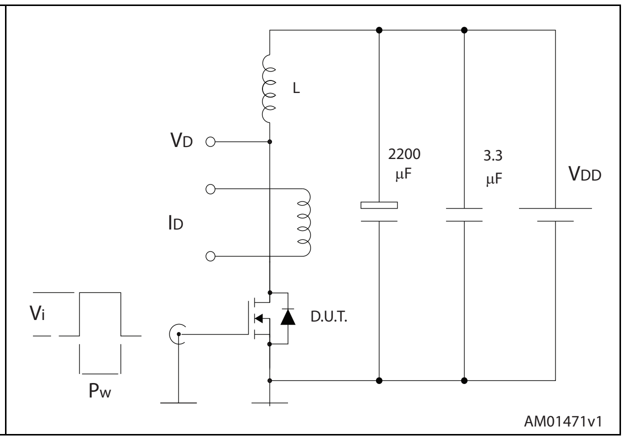


Figure 19. Unclamped inductive waveform

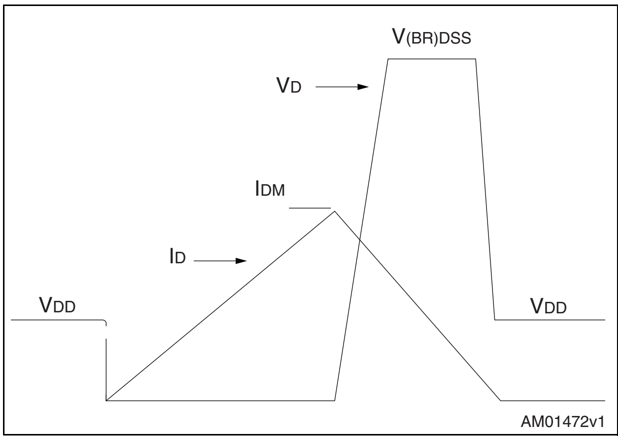
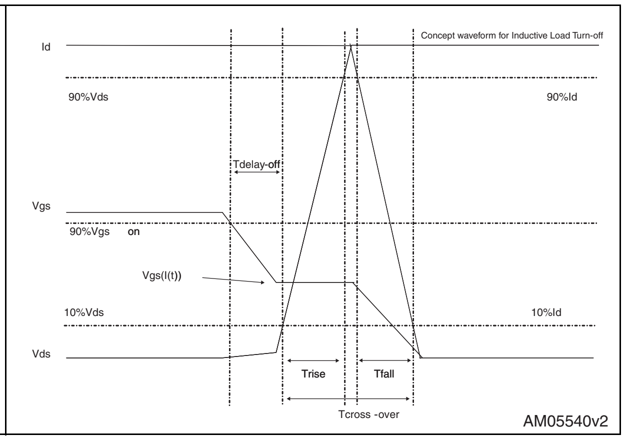


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 21. PowerFLAT™ 8x8 HV drawing mechanical data

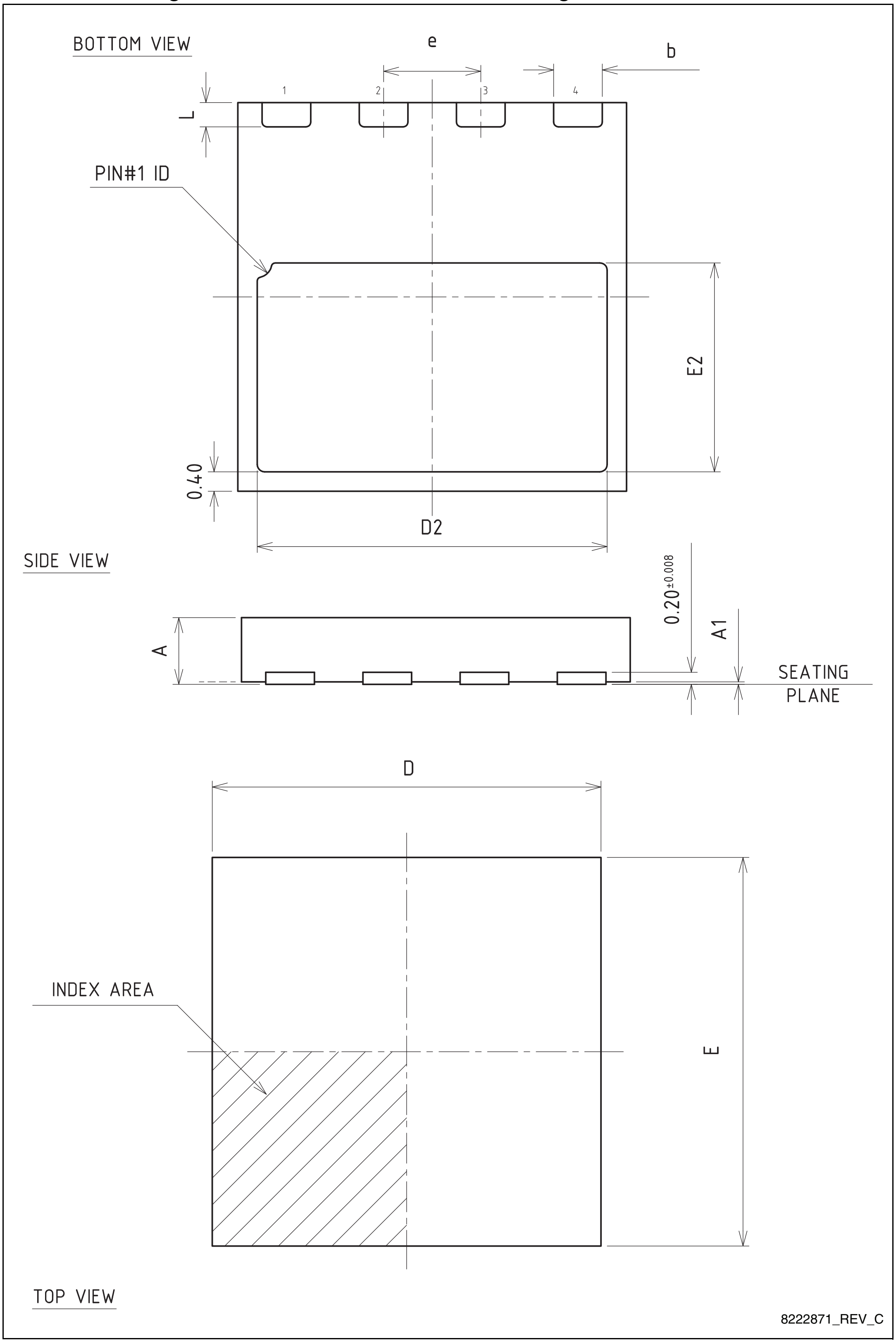
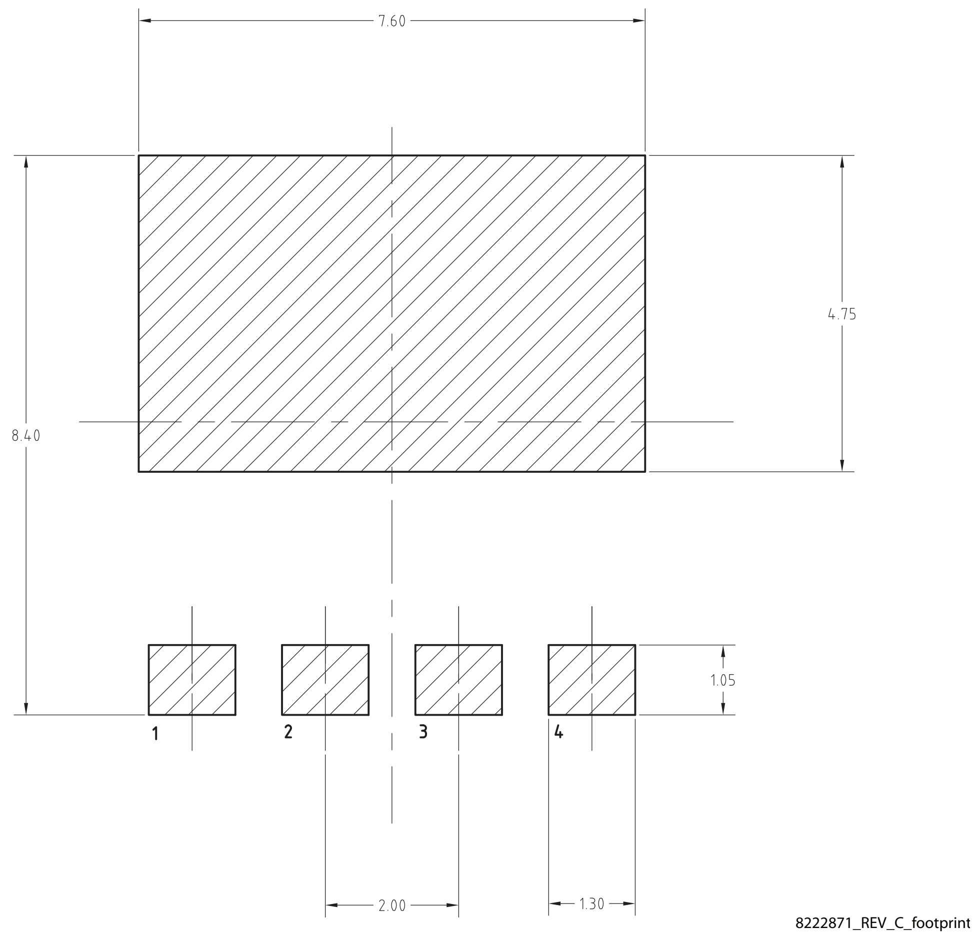


Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 22. PowerFLAT™ 8x8 HV recommended footprint



5 Packaging mechanical data

Figure 23. PowerFLAT™ 8x8 HV tape

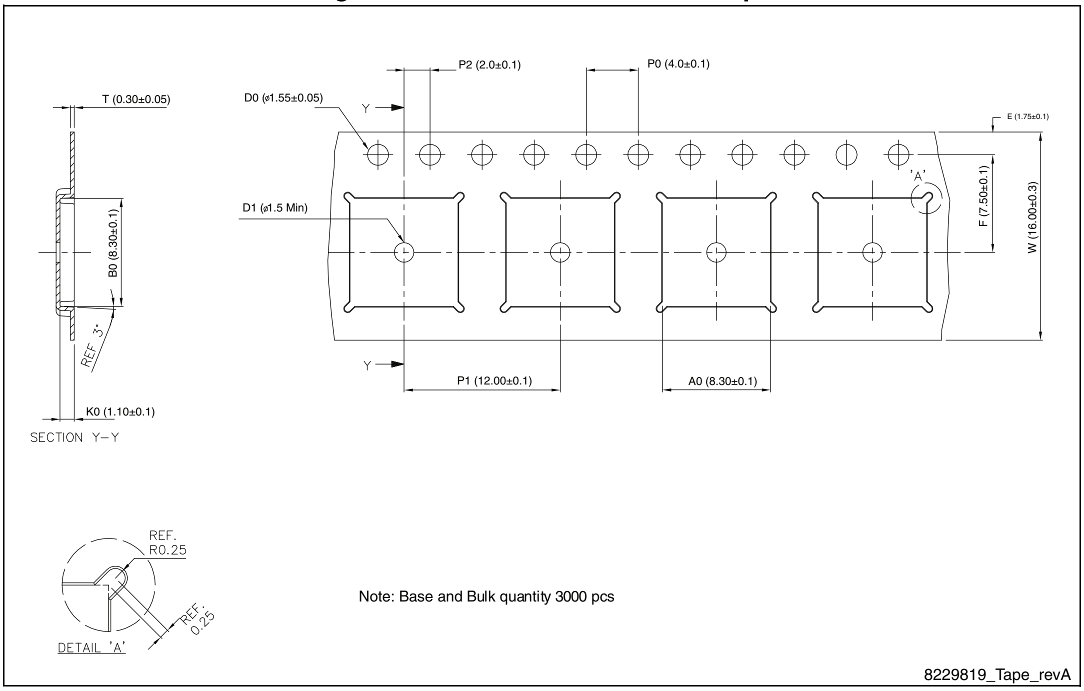


Figure 24. PowerFLAT™ 8x8 HV package orientation in carrier tape.

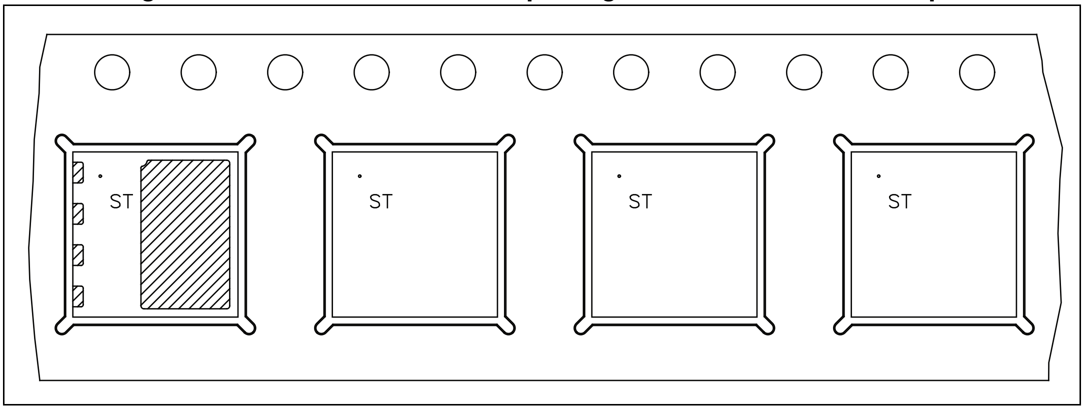
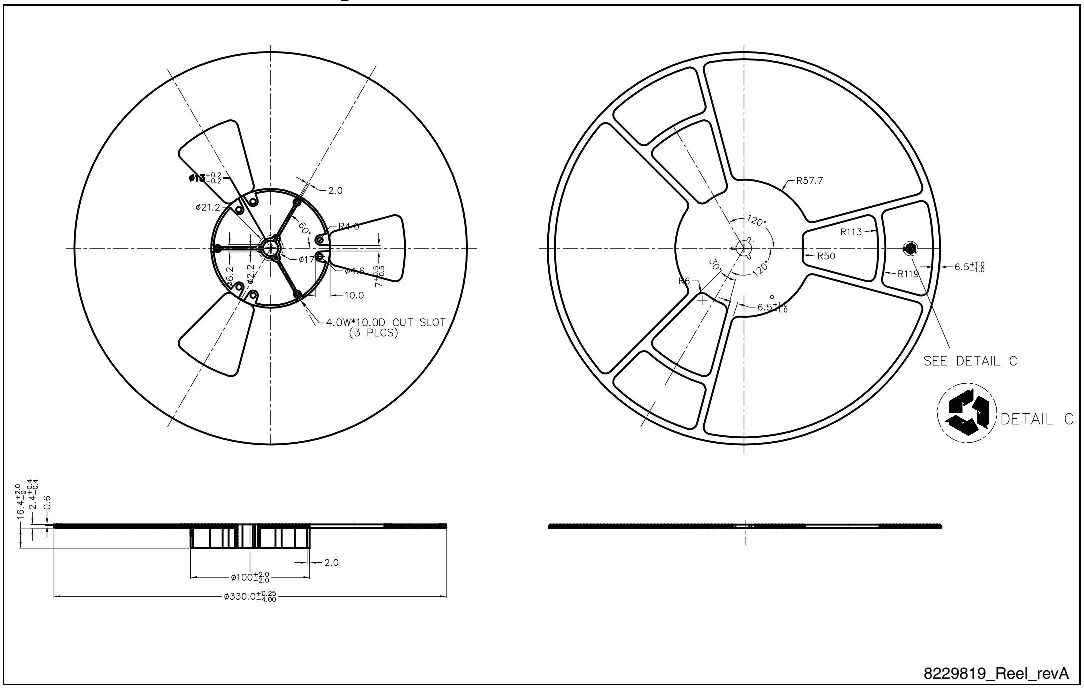


Figure 25. PowerFLAT™ 8x8 HV reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Dec-2011	1	First release.
17-Oct-2012	2	Updated: *Table 5*, *6* and *Table 7.: Source drain diode* typ. values
24-Jan-2013	3	– Modified: *Figure 1: Internal schematic diagram 4* and *6* – Document status promoted from preliminary data to production data – Modified: V_{DD} on *Table 5* – Minor text changes
22-Sep-2014	4	– Updated title, features and description in cover page. – Updated *Figure 1: Internal schematic diagram*. – Updated *Section 4: Package mechanical data*.