STP27N60M2-EP, STW27N60M2-EP

N-channel 600 V, 0.150 Ω typ., 20 A MDmesh™ M2 EP Power MOSFETs in TO-220 and TO-247 packages

Datasheet - production data

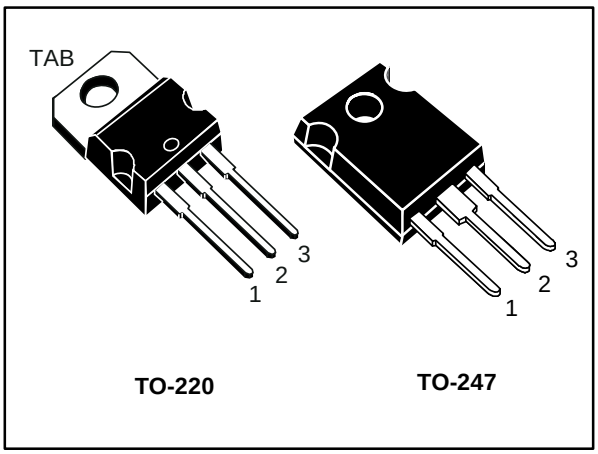
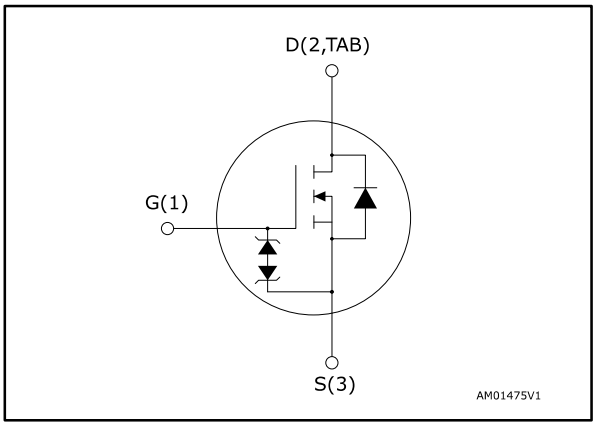


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STP27N60M2-EP	600 V	0.163 Ω	20 A
STW27N60M2-EP	600 V	0.163 Ω	20 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for very high frequency converters (f > 150 kHz)

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 EP enhanced performance technology. Thanks to their strip layout and an improved vertical structure, these devices exhibit low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering them suitable for the most demanding very high frequency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP27N60M2-EP	27N60M2EP	TO-220	Tube
STW27N60M2-EP		TO-247	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	20	A
I_D	Drain current (continuous) at T_C = 100 °C	13	A
I_{DM}(1)	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at T_C = 25 °C	170	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 20 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.

(3)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.74		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	3.6	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	260	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		0.150	0.163	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	1320	-	pF
C_{oss}	Output capacitance		-	70	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	146	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 20 A, V_{GS} = 10 V (see *Figure 17: "Test circuit for gate charge behavior"*)	-	33	-	nC
Q_{gs}	Gate-source charge		-	5.2	-	nC
Q_{gd}	Gate-drain charge		-	16	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16: "Test circuit for resistive load switching times"* and *Figure 21: "Switching time waveform"*)	-	13.4	-	ns
t_r	Rise time		-	8.1	-	ns
$t_{d(off)}$	Turn-off-delay time		-	55.6	-	ns
t_f	Fall time		-	6.3	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
I_{SDM} (1)	Source-drain current (pulsed)		-		80	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 20 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 21: "Switching time waveform"*)	-	271		ns
Q_{rr}	Reverse recovery charge		-	3.44		µC
I_{RRM}	Reverse recovery current		-	25.4		A
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 21: "Switching time waveform"*)	-	352		ns
Q_{rr}	Reverse recovery charge		-	4.82		µC
I_{RRM}	Reverse recovery current		-	27.4		A

Notes:

(1)Pulse width is limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for TO-220

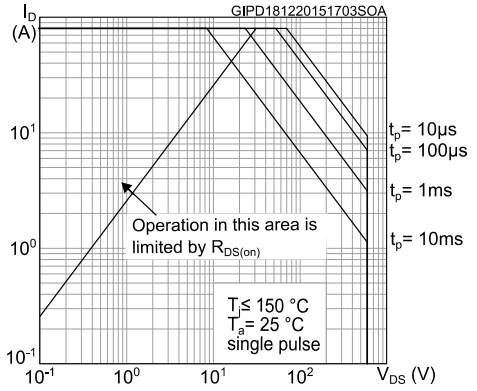


Figure 3: Thermal impedance for TO-220

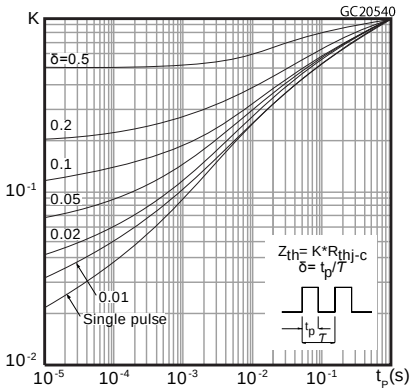


Figure 4: Safe operating area for TO-247

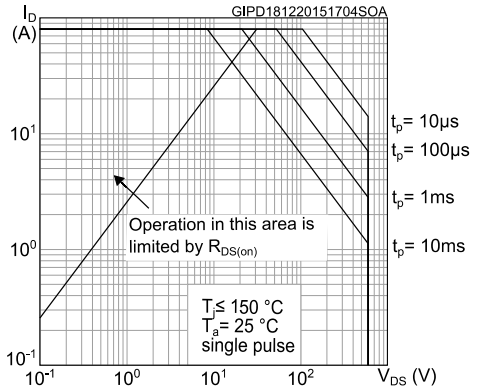


Figure 5: Thermal impedance for TO-247

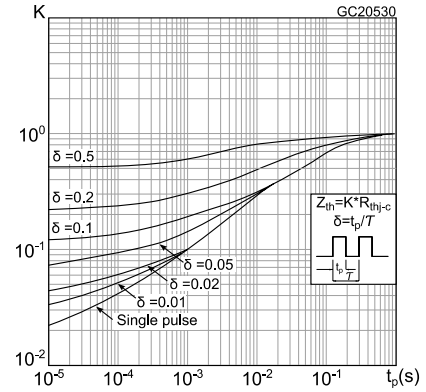


Figure 6: Output characteristics

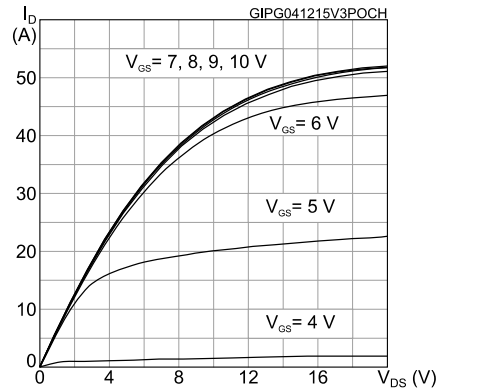


Figure 7: Transfer characteristics

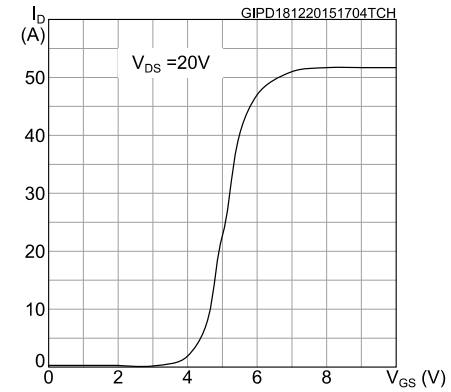


Figure 8: Gate charge vs gate-source voltage

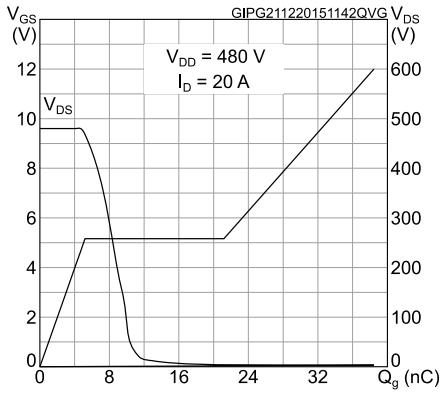


Figure 9: Static drain-source on-resistance

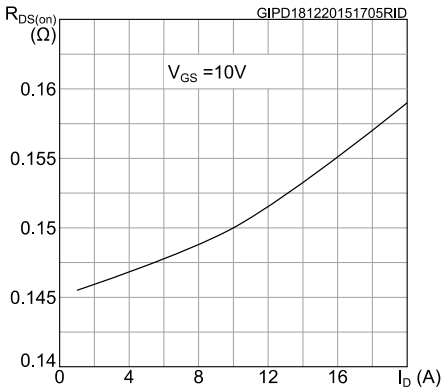


Figure 10: Capacitance variations

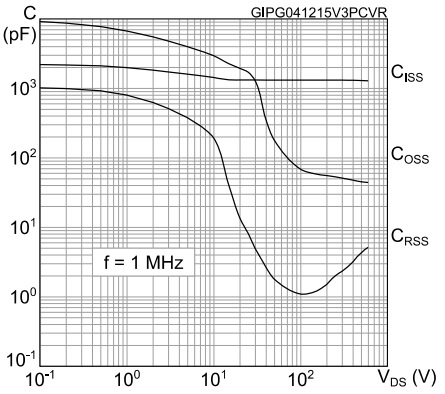


Figure 11: Output capacitance stored energy

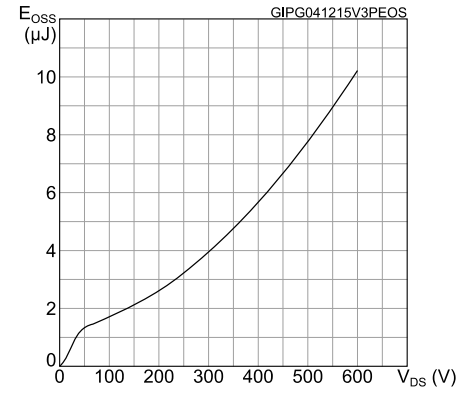


Figure 12: Normalized V(BR)DSS vs temperature

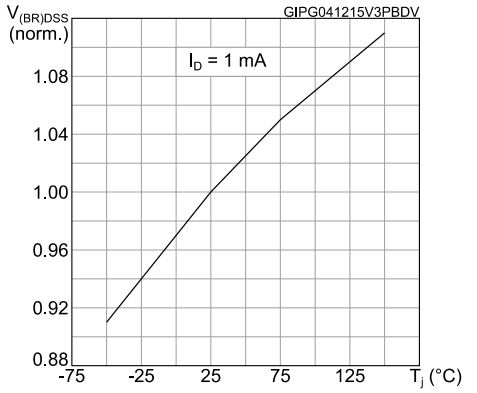


Figure 13: Normalized gate threshold voltage vs temperature

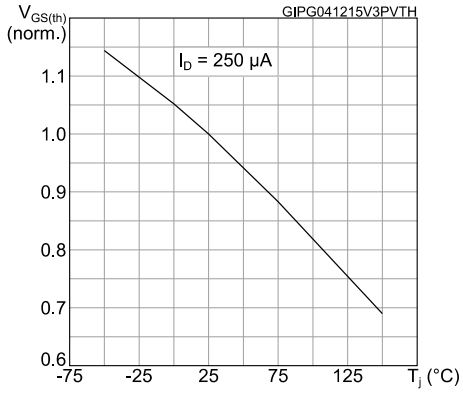


Figure 14: Normalized on-resistance vs temperature

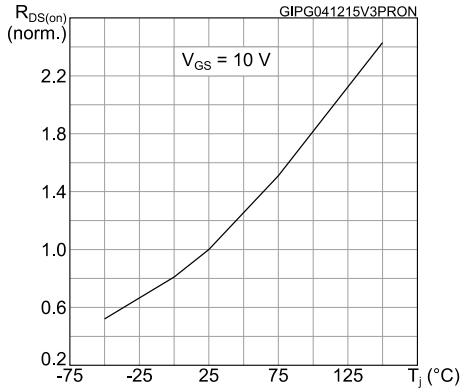
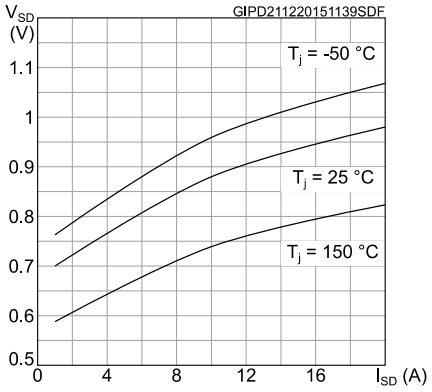


Figure 15: Source-drain diode forward characteristics



3 Test circuits

Figure 16: Test circuit for resistive load switching times

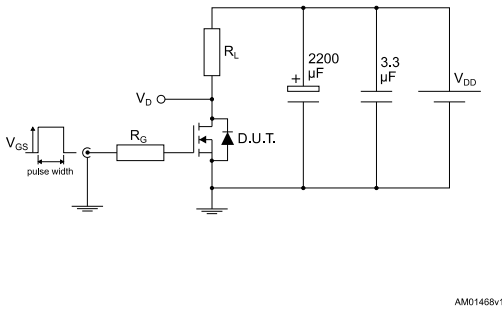


Figure 17: Test circuit for gate charge behavior

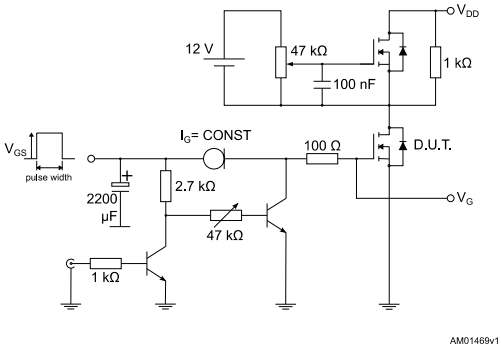


Figure 18: Test circuit for inductive load switching and diode recovery times

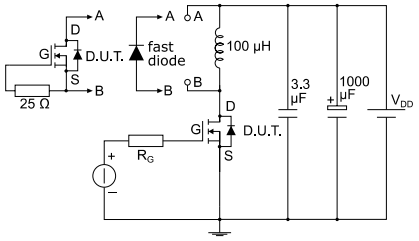


Figure 19: Unclamped inductive load test circuit

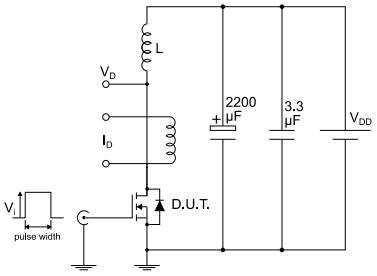


Figure 20: Unclamped inductive waveform

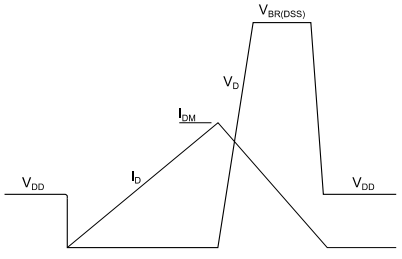
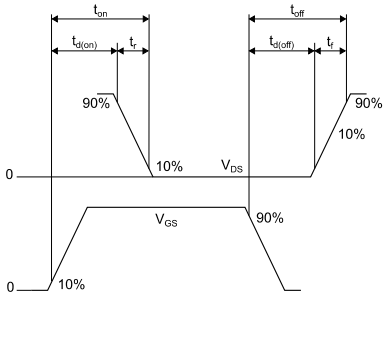


Figure 21: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 22: TO-220 type A package outline

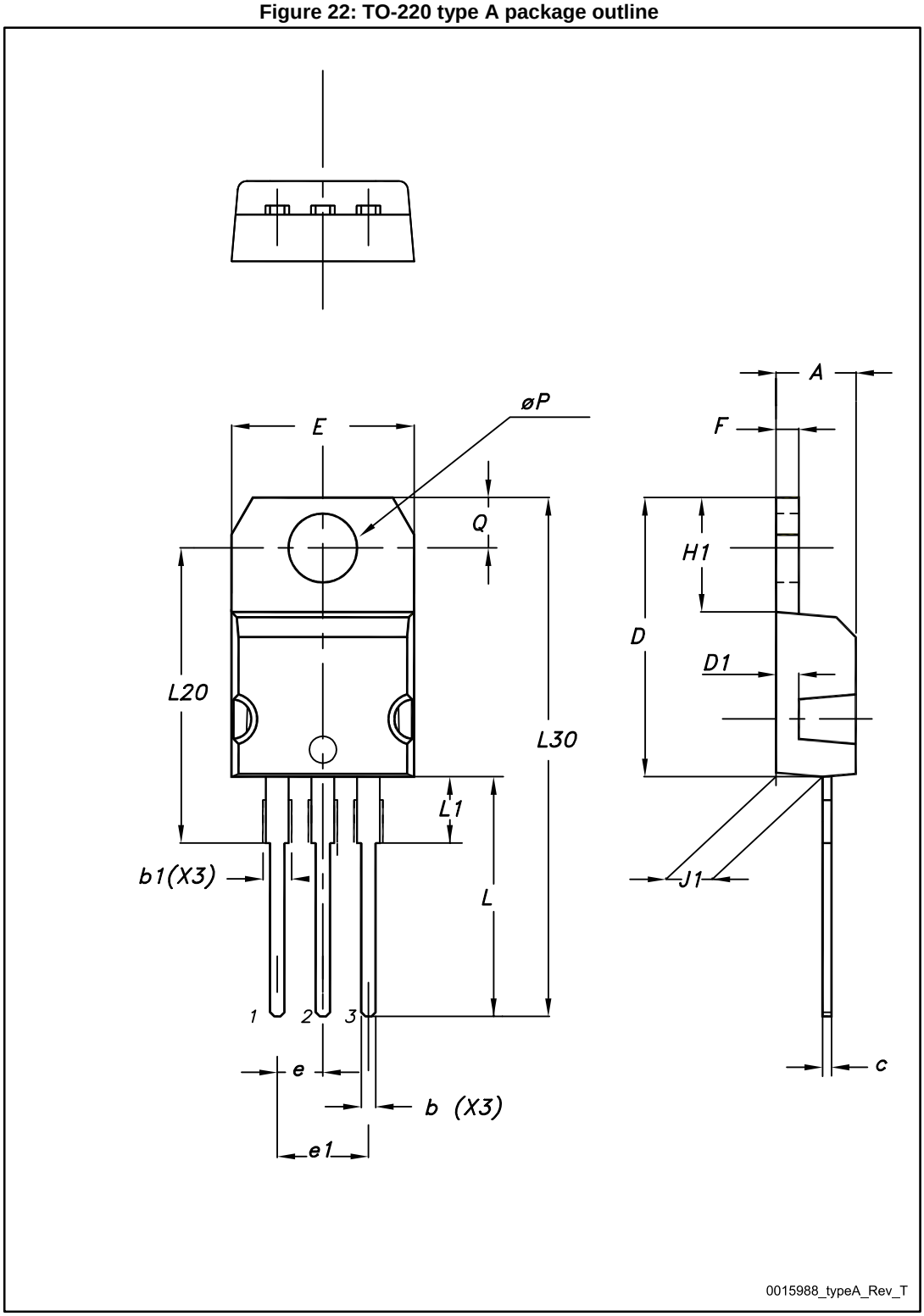


Table 9: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.2 TO-247 package information

Figure 23: TO-247 package outline

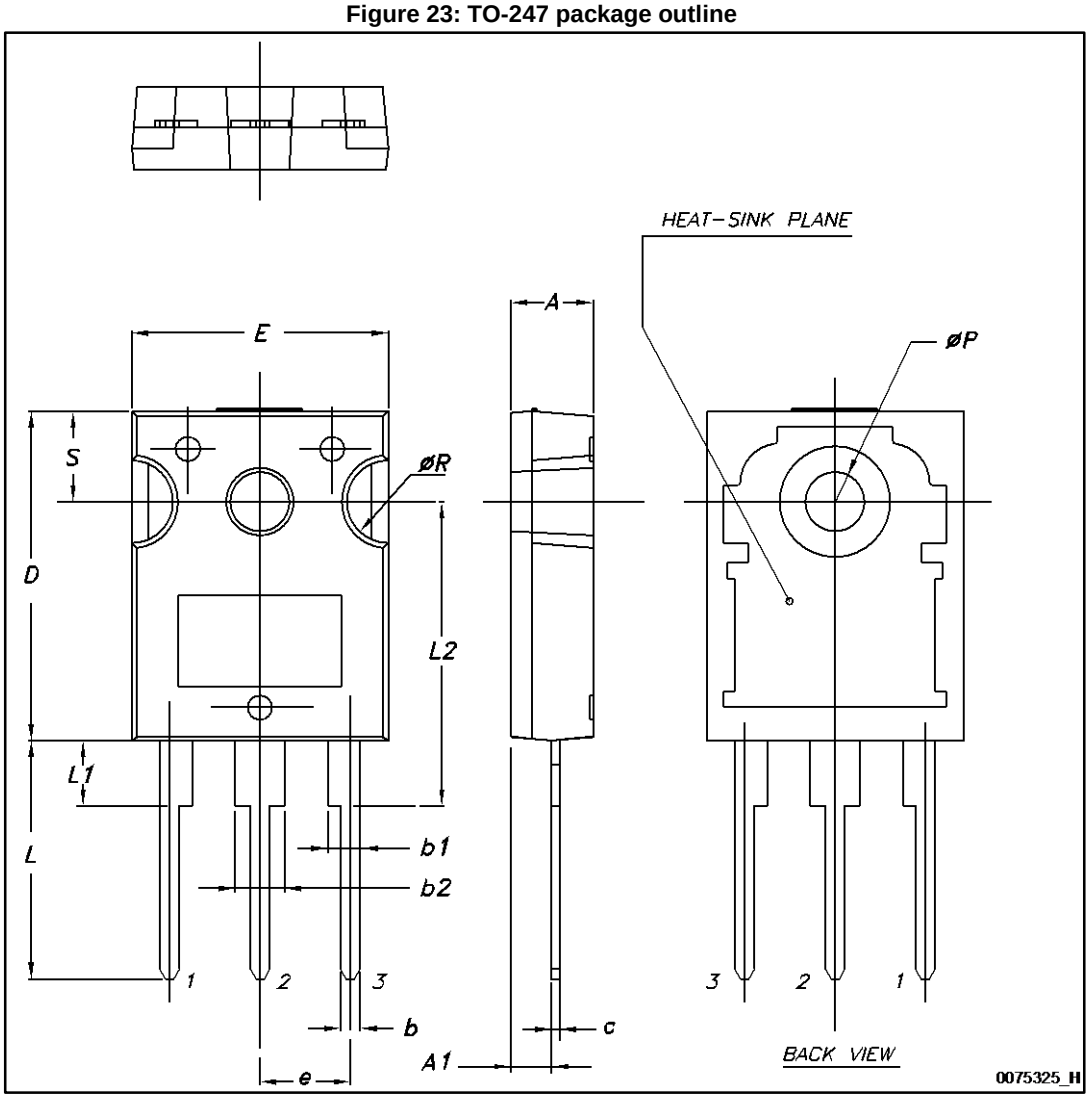


Table 10: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
15-Dec-2015	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.