STS5DP3LLH6

Dual P-channel -30 V, 48 mΩ typ., -5 A, STripFET™ H6 Power MOSFET in an SO-8 package

Datasheet - production data

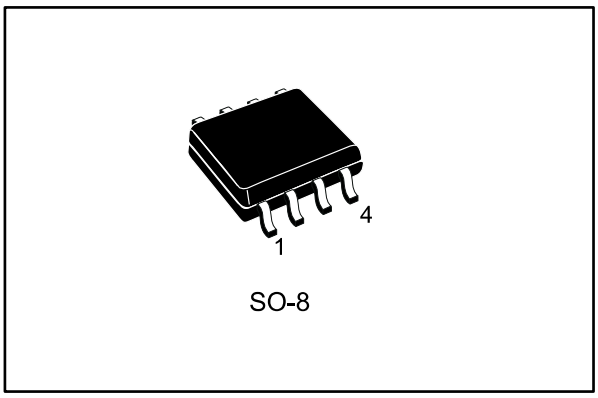
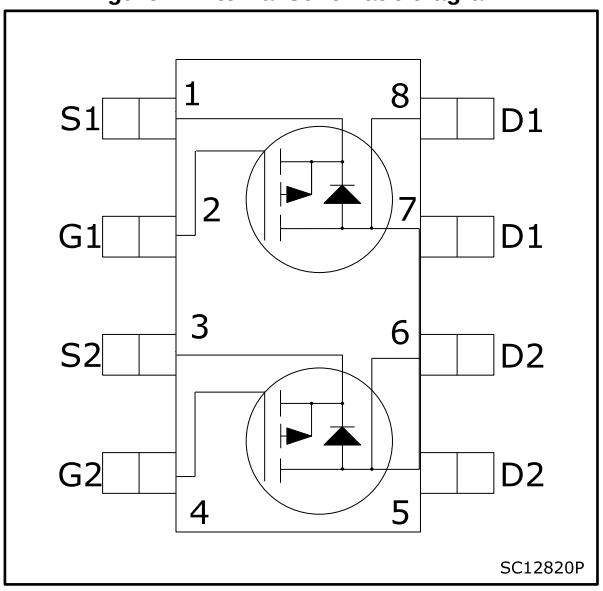


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STS10P3LLH6	-30 V	56 mΩ	-5 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STS5DP3LLH6	5KK3L	SO-8	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_{amb} = 25 °C	-5	A
	Drain current (continuous) at T_{amb} = 100 °C	-3.2	
I_{DM}(1)	Drain current (pulsed)	-20	A
P_{TOT}	Total dissipation at T_{amb} = 25 °C	2.7	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$(1)	Thermal resistance junction-amb	47	°C/W

Notes:

(1)When mounted on an 1-inch² FR-4 board, 2 oz. Cu., t ≤ 10 s

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = -30 V			-1	µA
		V_{GS} = 0 V, V_{DS} = -30 V, T_J = 125 °C(1)			-10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			-100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-2.5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = -10 V, I_D = -2.5 A		48	56	mΩ
		V_{GS} = -4.5 V, I_D = -2.5 A		75	90	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = -25 V, f = 1 MHz, V_{GS} = 0 V	-	639	-	pF
C_{oss}	Output capacitance		-	79	-	pF
C_{rss}	Reverse transfer capacitance		-	52	-	pF
Q_g	Total gate charge	V_{DD} = -15 V, I_D = -5 A V_{GS} = -4.5 V	-	6	-	nC
Q_{gs}	Gate-source charge		-	1.9	-	nC
Q_{gd}	Gate-drain charge		-	2.1	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = -15 V, I_D = -5 A, R_G = 4.7 Ω, V_{GS} = -10 V	-	5.4	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	19.2	-	ns
t_f	Fall time		-	3.4	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on-voltage	I_{SD} = -5 A, V_{GS} = 0 V	-		-1.1	V
t_{rr}	Reverse recovery time	I_{SD} = -5 A, di/dt = 100 A/µs, V_{DD} = -16 V, T_J = 150 °C	-	11.2		ns
Q_{rr}	Reverse recovery charge		-	3.5		nC
I_{RRM}	Reverse recovery current		-	-0.6		A

Notes:

(1)Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

For the P-channel Power MOSFET, current and voltage polarities are reversed.

Figure 2: Safe operating area

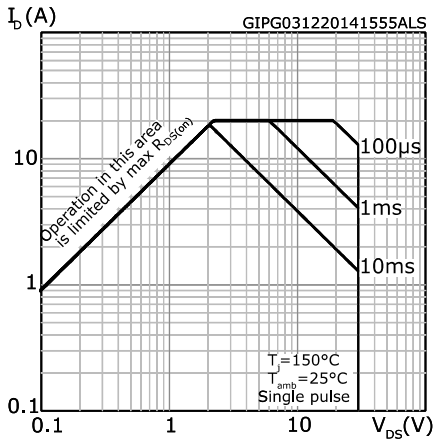


Figure 3: Thermal impedance

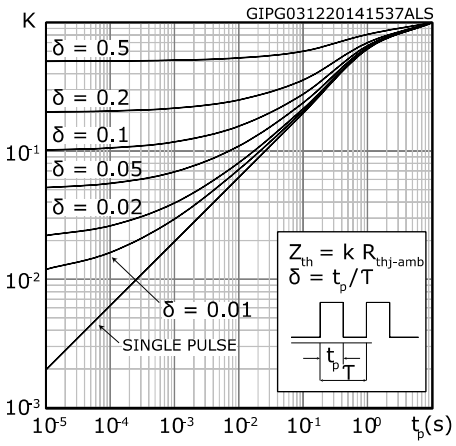


Figure 4: Output characteristics

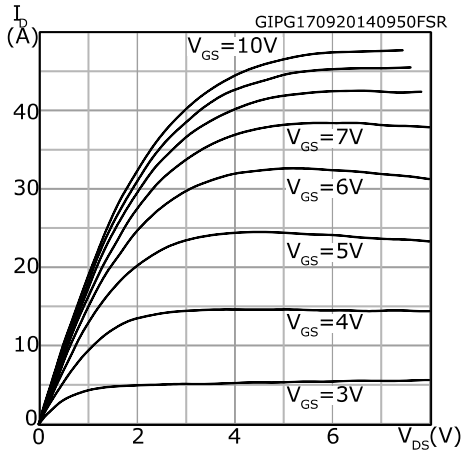


Figure 5: Transfer characteristics

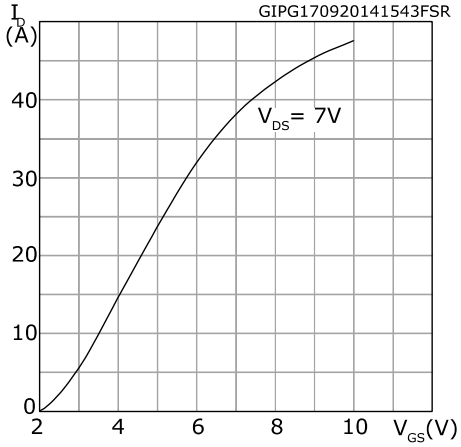


Figure 6: Gate charge vs gate-source voltage

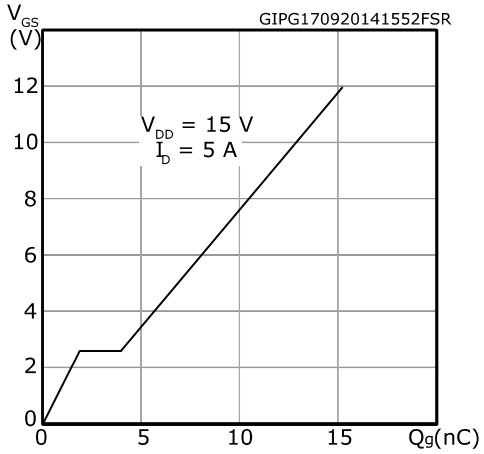


Figure 7: Static drain-source on-resistance

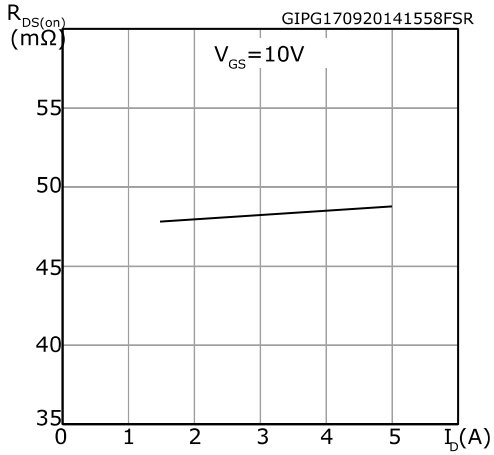


Figure 8: Normalized $V_{(BR)DSS}$ vs temperature

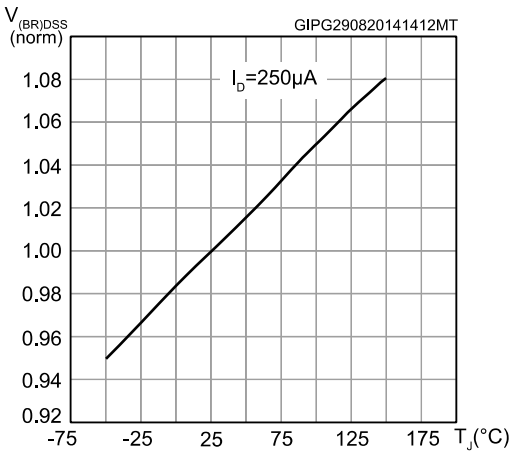


Figure 9: Capacitance variations

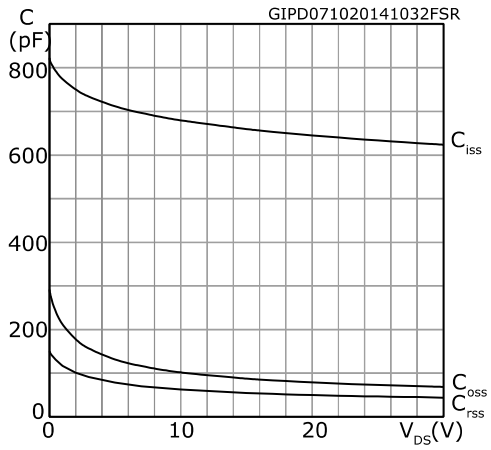


Figure 10: Normalized gate threshold voltage vs temperature

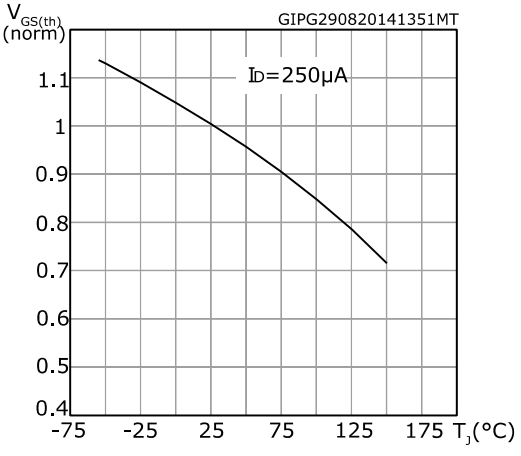


Figure 11: Normalized on-resistance vs temperature

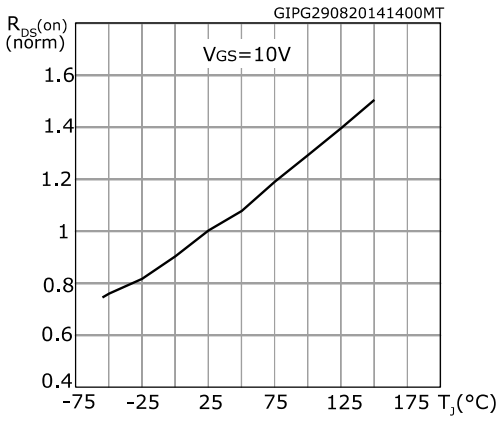
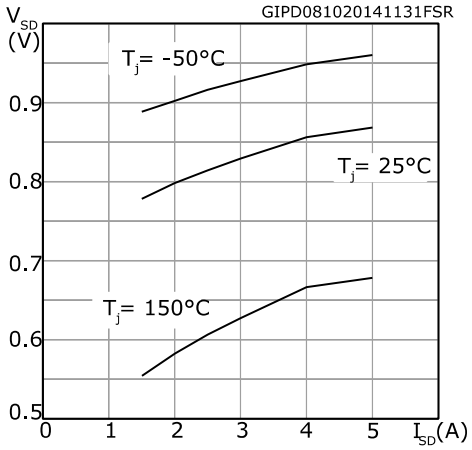


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

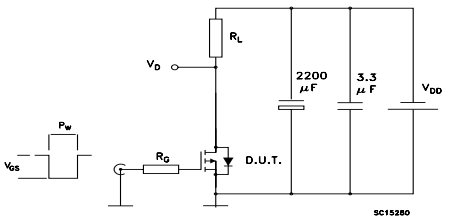


Figure 14: Gate charge test circuit

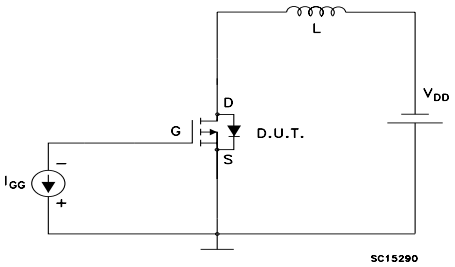
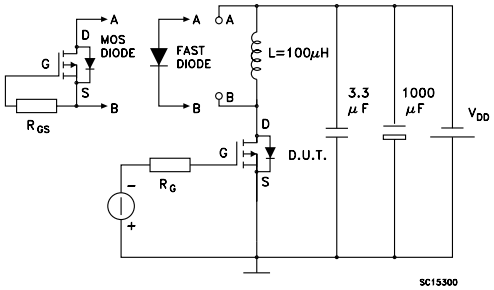


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 SO-8 package information

Figure 16: SO-8 package outline

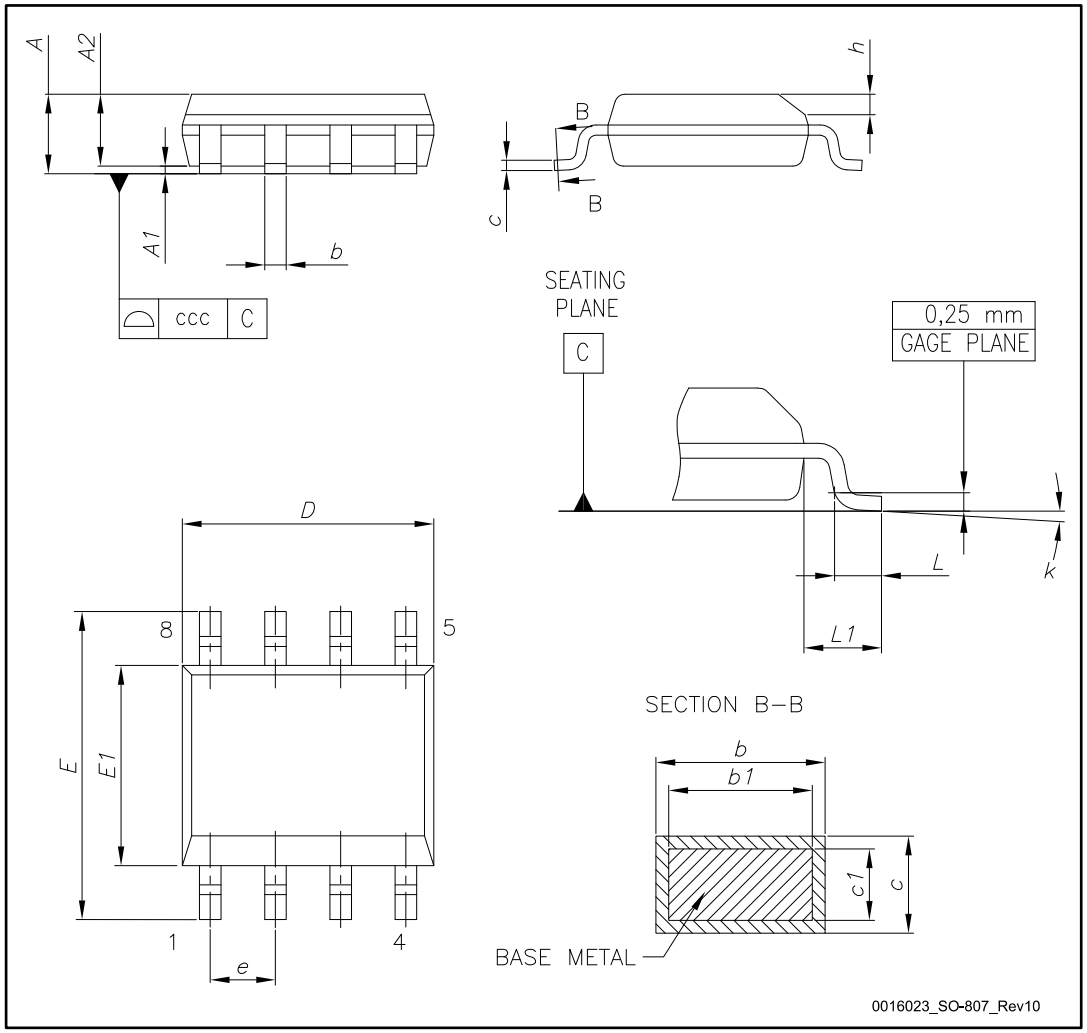
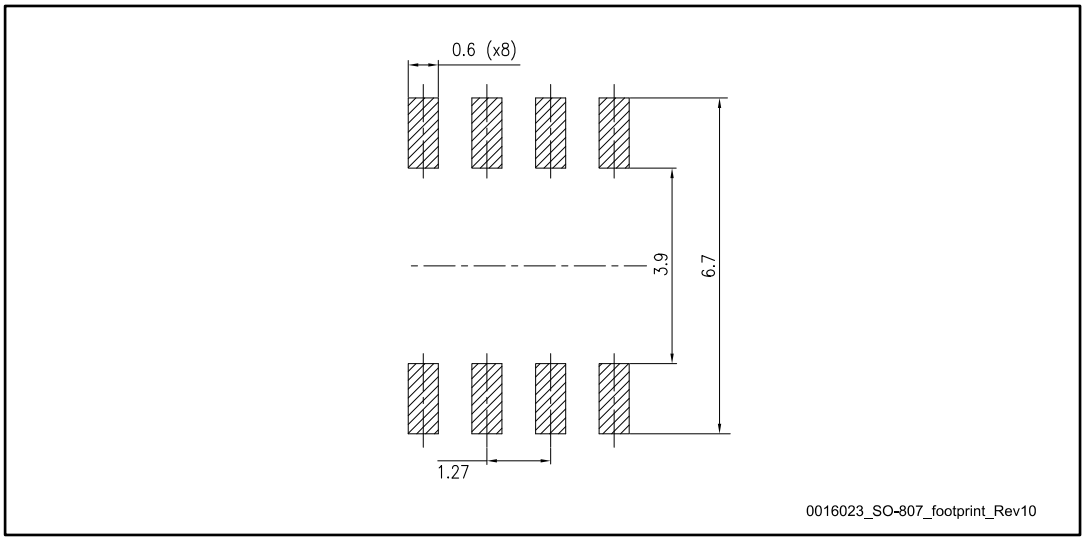


Table 8: SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 17: SO-8 recommended footprint (dimensions are in mm)



4.2 SO-8 packing information

Figure 18: SO-8 tape and reel dimensions

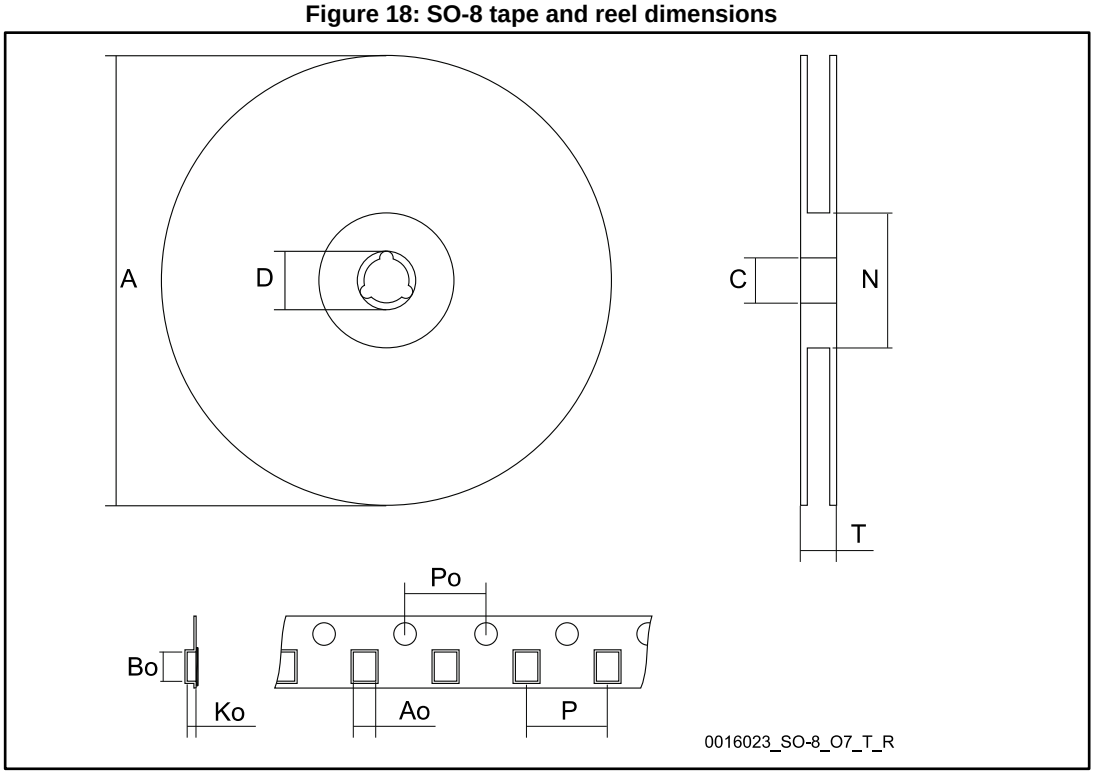


Table 9: SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
30-Jan-2014	1	First revision.
11-Dec-2014	2	Text edits throughout document On cover page: changed title description, updated Features, updated Description. In *Table 4*, changed RDS(on) values In *Table 5*, changed values and test conditions In *Table 6*, changed values and test conditions In *Table 7*, changed values and test conditions Added *Section 2.1: Electrical characteristics (curves)* Updated *Section 3: Test circuits* Updated *Section 4: Package mechanical data*
17-Jan-2018	3	Datasheet status promoted from preliminary to production data. Updated title and features on cover page. Updated *Section 1: "Electrical ratings"* and *Section 2: "Electrical characteristics"*. Minor text changes

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