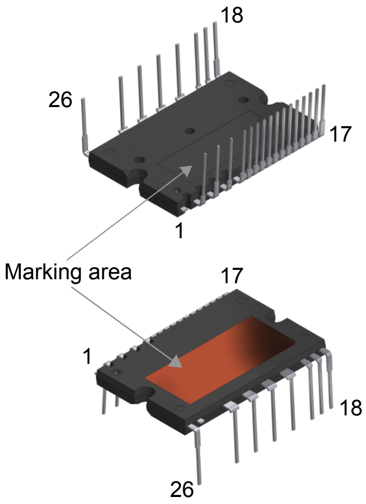
# STGIB8CH60S-L

Datasheet

# SLLIMM- $2^{nd}$ series IPM, 3-phase inverter, 12 A, 600 V short-circuit rugged IGBT



**SDIP2B-26L type L2**

| Product status link |
|---|
| STGIB8CH60S-L |

| Product summary | |
|---|---|
| **Order code** | STGIB8CH60S-L |
| **Marking** | GIB8CH60S-L |
| **Package** | SDIP2B-26L type L2 |
| **Packing** | Tube |

## Features

- IPM 12 A, 600 V 3-phase IGBT inverter bridge including 2 control ICs for gate driving and freewheeling diodes
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Internal bootstrap diode
- Undervoltage lockout of gate drivers
- Smart shutdown function
- Short-circuit protection
- Shutdown input/fault output
- Separate open emitter outputs
- Built-in temperature sensor
- Comparator for fault protection
- Short-circuit rugged TFS IGBTs
- Very fast, soft recovery diodes
- Fully isolated package
- Isolation ratings of 1500 Vrms/min.
- UL recognition: UL 1557, file E81734

## Applications

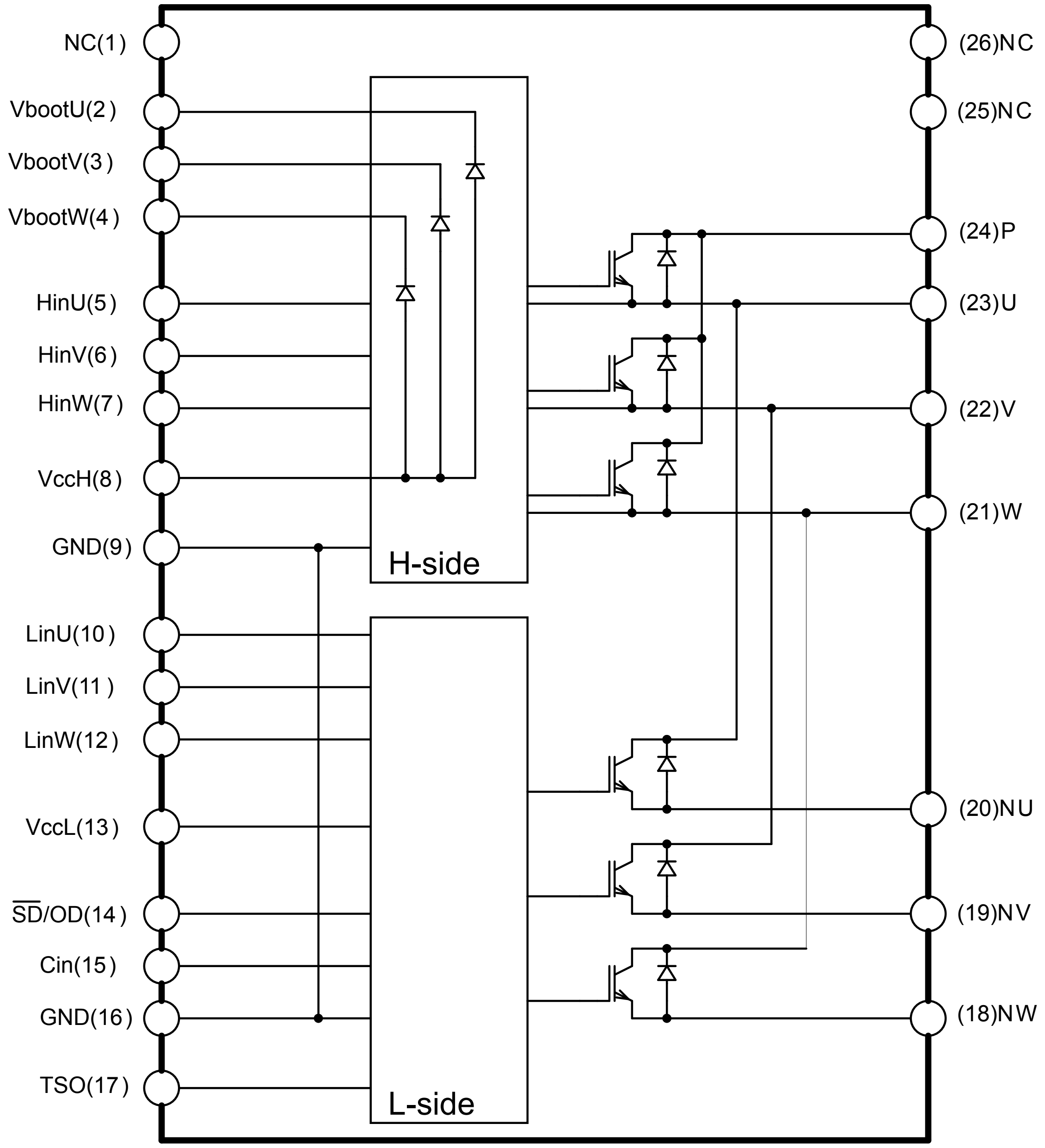
- 3-phase inverters for motor drives
- Home appliances such as washing machines, refrigerators, air conditioners and sewing machines

## Description

This second series of SLLIMM (small low-loss intelligent molded module) provides a compact, high-performance AC motor drive in a simple, rugged design. It combines new ST proprietary control ICs (one LS and one HS driver) with an improved short-circuit rugged trench gate field-stop (TFS) IGBT, making it ideal for motor drives operating up to 20 kHz in hard-switching circuitries. SLLIMM is a trademark of STMicroelectronics.

# 1 Internal schematic diagram and pin configuration

Figure 1. Internal schematic diagram and pin configuration



AMG171020161037SA

Table 1. **Pin description**

| Pin | Symbol | Description |
|---|---|---|
| 1 | NC | - |
| 2 | VBOOTu | Bootstrap voltage for U phase |
| 3 | VBOOTv | Bootstrap voltage for V phase |
| 4 | VBOOTw | Bootstrap voltage for W phase |
| 5 | HINu | High-side logic input for U phase |
| 6 | HINv | High-side logic input for V phase |
| 7 | HINw | High-side logic input for W phase |
| 8 | VCCH | High-side low voltage power supply |
| 9 | GND | Ground |
| 10 | LINu | Low-side logic input for U phase |
| 11 | LINv | Low-side logic input for V phase |
| 12 | LINw | Low-side logic input for W phase |
| 13 | VCCL | Low-side low voltage power supply |
| 14 | $\overline{\text{SD}}$/OD | Shutdown logic input (active low) / open-drain (comparator output) |
| 15 | CIN | Comparator input |
| 16 | GND | Ground |
| 17 | TSO | Temperature sensor output |
| 18 | NW | Negative DC input for W phase |
| 19 | NV | Negative DC input for V phase |
| 20 | NU | Negative DC input for U phase |
| 21 | W | W phase output |
| 22 | V | V phase output |
| 23 | U | U phase output |
| 24 | P | Positive DC input |
| 25 | NC | - |
| 26 | NC | - |

# 2 Absolute maximum ratings

$T_J$ = 25 °C unless otherwise noted.

Table 2. **Inverter part**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{PN}$ | Supply voltage among P -$N_U$, -$N_V$, -$N_W$ | 450 | V |
| $V_{PN(surge)}$ | Supply voltage surge among P -$N_U$, -$N_V$, -$N_W$ | 500 | V |
| $V_{CES}$ | Collector-emitter voltage each IGBT | 600 | V |
| ± $I_C$ | Continuous collector current each IGBT ($T_C$ = 25 °C) | 12 | A |
| | Continuous collector current each IGBT ($T_C$ = 80 °C) | 8 | |
| ± $I_{CP}$ | Peak collector current each IGBT (less than 1 ms) | 24 | A |
| $P_{TOT}$ | Total power dissipation at $T_C$=25 °C each IGBT | 50 | W |
| $t_{scw}$ | Short-circuit withstand time, $V_{CE}$ = 300 V, $T_J$ = 125 °C, $V_{CC}$ = $V_{boot}$ = 15 V, $V_{IN}$ = 0 to 5 V | 5 | µs |

Table 3. **Control part**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage between $V_{CCH}$-GND, $V_{CCL}$-GND | -0.3 | 20 | V |
| $V_{BOOT}$ | Bootstrap voltage | -0.3 | 619 | V |
| $V_{OUT}$ | Output voltage among U, V, W and GND | $V_{BOOT}$ - 21 | $V_{BOOT}$ + 0.3 | V |
| $V_{CIN}$ | Comparator input voltage | -0.3 | 20 | V |
| $V_{IN}$ | Logic input voltage applied among HINx, LINx and GND | -0.3 | 15 | V |
| $V_{\overline{SD}/OD}$ | Open-drain voltage | -0.3 | 7 | V |
| $I_{\overline{SD}/OD}$ | Open-drain sink current | | 10 | mA |
| $V_{TSO}$ | Temperature sensor output voltage | -0.3 | 5.5 | V |
| $I_{TSO}$ | Temperature sensor output current | | 7 | mA |

Table 4. **Total system**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{ISO}$ | Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s) | 1500 | Vrms |
| $T_J$ | Power chip operating junction temperature range | -40 to 175 | °C |
| $T_C$ | Module operation case temperature range | -40 to 125 | °C |

## 2.1 Thermal data

Table 5. **Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(j-c)}$ | Thermal resistance junction-case single IGBT | 3 | °C/W |
| | Thermal resistance junction-case single diode | 6 | |

# 3 Electrical characteristics

$T_J$ = 25 °C unless otherwise noted.

## 3.1 Inverter part

Table 6. **Static**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cut-off current | $V_{CE}$ = 600 V, $V_{CC}$ = $V_{boot}$ = 15 V | - | | 100 | µA |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_{CC}$ = $V_{boot}$ = 15 V, $V_{IN}$(1) = 0 to 5 V, $I_C$ = 8 A | - | 1.68 | 2.18 | V |
| | | $V_{CC}$ = $V_{boot}$ = 15 V, $V_{IN}$(1) = 0 to 5 V, $I_C$ = 12 A | - | 1.91 | | |
| $V_F$ | Diode forward voltage | $V_{IN}$ = 0 V, $I_C$ = 8 A | - | 1.55 | 2.1 | V |
| | | $V_{IN}$ = 0 V, $I_C$ = 12 A | - | 1.7 | | V |

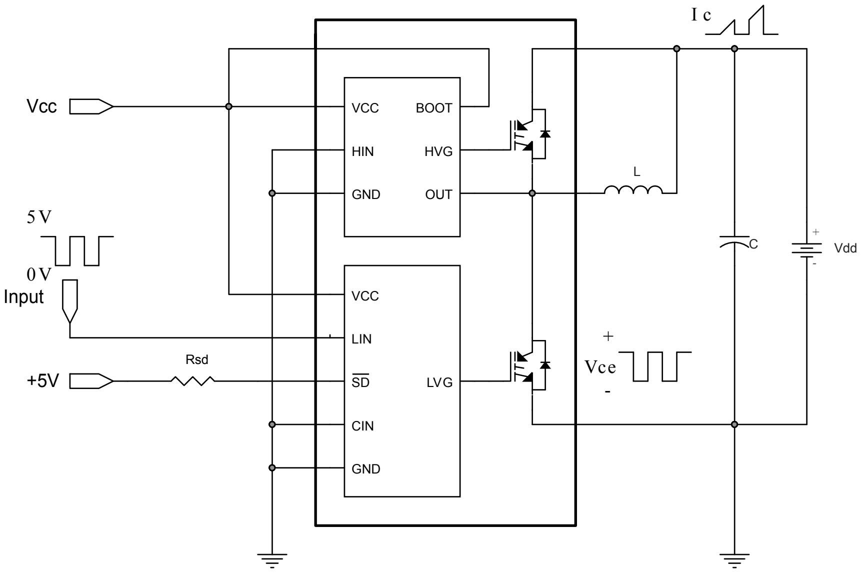
1. *Applied among HINx, LINx and GND for x = U, V, W.*

Table 7. **Inductive load switching time and energy**

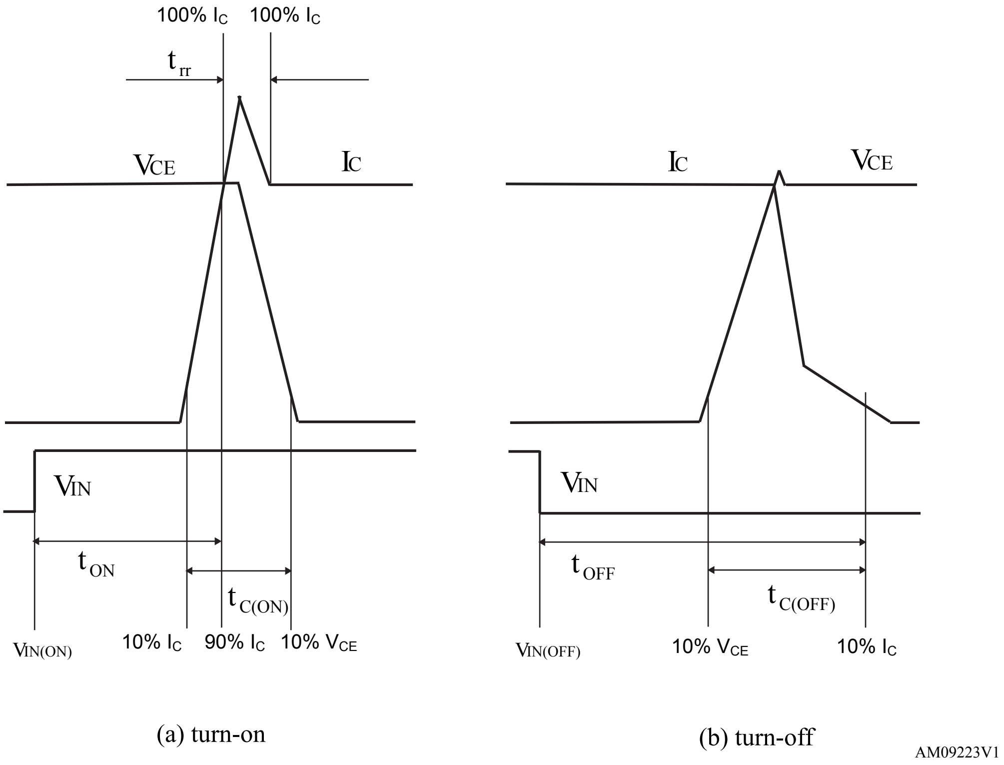
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{on}$(1) | Turn-on time | $V_{DD}$ = 300 V, $V_{CC}$ = $V_{boot}$ = 15 V, $V_{IN}$(2) = 0 to 5 V, $I_C$ = 8 A | - | 280 | - | ns |
| $t_{c(on)}$(1) | Crossover time on | | - | 142 | - | |
| $t_{off}$(1) | Turn-off time | | - | 400 | - | |
| $t_{c(off)}$(1) | Crossover time off | | - | 85 | - | |
| $t_{rr}$ | Reverse recovery time | | - | 215 | - | |
| $E_{on}$ | Turn-on switching energy | | - | 201 | - | µJ |
| $E_{off}$ | Turn-off switching energy | | - | 102 | - | |
| $E_{rr}$ | Reverse recovery energy | | - | 8.1 | - | |
| $t_{on}$(1) | Turn-on time | $V_{DD}$ = 300 V, $V_{CC}$ = $V_{boot}$ = 15 V, $V_{IN}$(2) = 0 to 5 V, $I_C$ = 12 A | - | 300 | - | ns |
| $t_{c(on)}$(1) | Crossover time on | | - | 175 | - | |
| $t_{off}$(1) | Turn-off time | | - | 380 | - | |
| $t_{c(off)}$(1) | Crossover time off | | - | 85 | - | |
| $t_{rr}$ | Reverse recovery time | | - | 220 | - | |
| $E_{on}$ | Turn-on switching energy | | - | 340 | - | µJ |
| $E_{off}$ | Turn-off switching energy | | - | 160 | - | |
| $E_{rr}$ | Reverse recovery energy | | - | 10.2 | - | |

1. *$t_{on}$ and $t_{off}$ include the propagation delay times of the internal drive. $t_{C(on)}$ and $t_{C(off)}$ are the switching times of the IGBT itself under the internally given gate driving conditions.*
2. *Applied among HINx, LINx and GND for x = U, V, W.*

### Figure 2. Switching time test circuit



### Figure 3. Switching time definition



(a) turn-on

(b) turn-off

## 3.2 Control/protection parts

**Table 8. High- and low-side drivers**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{il}$ | Low logic level voltage | | | | 0.8 | V |
| $V_{ih}$ | High logic level voltage | | 2 | | | V |
| $I_{INh}$ | IN logic “1” input bias current | $IN_x$ = 15 V | 80 | 150 | 200 | µA |
| $I_{INl}$ | IN logic “0” input bias current | $IN_x$ = 0 V | | | 1 | µA |
| **High-side** | | | | | | |
| $V_{CC\_hys}$ | $V_{CC}$ UV hysteresis | | 1.2 | 1.4 | 1.7 | V |
| $V_{CCH\_th(on)}$ | $V_{CCH}$ UV turn-on threshold | | 11 | 11.5 | 12 | V |
| $V_{CCH\_th(off)}$ | $V_{CCH}$ UV turn-off threshold | | 9.6 | 10.1 | 10.6 | V |
| $V_{BS\_hys}$ | $V_{BS}$ UV hysteresis | | 0.5 | 1 | 1.6 | V |
| $V_{BS\_th(on)}$ | $V_{BS}$ UV turn-on threshold | | 10.1 | 11 | 11.9 | V |
| $V_{BS\_th(off)}$ | $V_{BS}$ UV turn-off threshold | | 9.1 | 10 | 10.9 | V |
| $I_{QBSU}$ | Under voltage $V_{BS}$ quiescent current | $V_{BS}$ = 9 V, HINx(1) = 5 V | | 55 | 75 | µA |
| $I_{QBS}$ | $V_{BS}$ quiescent current | $V_{CC}$ = 15 V, HINx(1) = 5 V | | 125 | 170 | µA |
| $I_{qccu}$ | Under voltage quiescent supply current | $V_{CC}$ = 9 V, HINx(1) = 0 V | | 190 | 250 | µA |
| $I_{qcc}$ | Quiescent current | $V_{CC}$ = 15 V, HINx(1) = 0 V | | 560 | 730 | µA |
| $R_{DS(on)}$ | BS driver ON resistance | | | 150 | | Ω |
| **Low-side** | | | | | | |
| $V_{CC\_hys}$ | $V_{CC}$ UV hysteresis | | 1.1 | 1.4 | 1.6 | V |
| $V_{CCL\_th(on)}$ | $V_{CCL}$ UV turn-on threshold | | 10.4 | 11.6 | 12.4 | V |
| $V_{CCL\_th(off)}$ | $V_{CCL}$ UV turn-off threshold | | 9.0 | 10.3 | 11 | V |
| $I_{qccu}$ | Under voltage quiescent supply current | $V_{CC}$ = 10 V, $\overline{SD}$ pulled to 5 V through $R_{SD}$ = 10 kΩ,<br>CIN = LINx(1) = 0 | | 600 | 800 | µA |
| $I_{qcc}$ | Quiescent current | $V_{CC}$ = 15 V, $\overline{SD}$= 5 V,<br>CIN = LINx(1) = 0 | | 700 | 900 | µA |
| $V_{SSD}$ | Smart $\overline{SD}$ unlatch threshold | | 0.5 | 0.6 | 0.75 | V |
| $I_{SDh}$ | $\overline{SD}$ logic “1” input bias current | $\overline{SD}$ = 5 V | 25 | 50 | 70 | µA |
| $I_{SDl}$ | $\overline{SD}$ logic “0” input bias current | $\overline{SD}$ = 0 V | | | 1 | µA |

1. *Applied among HINx, LINx and GND for x = U, V, W*

**Table 9. Temperature sensor output**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{TSO}$ | Temperature sensor output voltage | $T_J$ = 25 °C | 0.974 | 1.16 | 1.345 | V |
| $I_{TSO\_SNK}$ | Temperature sensor sink current capability | | | 0.1 | | mA |
| $I_{TSO\_SRC}$ | Temperature sensor source current capability | | 4 | | | mA |

**Table 10.** **Sense comparator ($V_{CC}$ = 15 V, unless otherwise is specified)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CIN}$ | CIN input bias current | $V_{CIN}$ =1 V | -0.2 | | 0.2 | µA |
| $V_{ref}$ | Internal reference voltage | | 460 | 510 | 560 | mV |
| $V_{OD}$ | Open-drain low level output voltage | $I_{od}$ = 5 mA | | | 500 | mV |
| $t_{CIN\_SD}$ | $C_{IN}$ comparator delay to $\overline{SD}$ | $\overline{SD}$ pulled to 5 V through $R_{SD}$= 10 kΩ;<br>measured applying a voltage step 0-1 V to pin CIN;<br>50 % CIN to 90 % $\overline{SD}$ | 240 | 320 | 410 | ns |
| $SR_{SD}$ | $\overline{SD}$ fall slew rate | $\overline{SD}$ pulled to 5 V through $R_{SD}$= 10 kΩ;<br>$C_L$= 1 nF through $\overline{SD}$ and ground;<br>90 % $\overline{SD}$ to 10 % $\overline{SD}$ | | 25 | | V/µs |

The comparator stays enabled even if $V_{CC}$ is in the UVLO condition but higher than 4 V.

# 4 Fault management

The device integrates an open-drain output connected to the $\overline{SD}$ pin. As soon as a fault occurs, the open-drain is activated and the LVGx outputs are forced low. Two types of fault can be identified:

- Overcurrent (OC) sensed by the internal comparator (see more detail in Section 4.1 Smart shutdown function);
- Undervoltage on supply voltage ($V_{CC}$)

Each fault enables the SD open drain for a different time, as described in the following table.

Table 11. **Fault timing**

| Symbol | Parameter | Event time (1) | SD open-drain enable time result (1)(2) |
|---|---|---|---|
| OC | Over-current event | ≤ 24 µs | 24 µs |
| | | > 24 µs | OC time |
| UVLO | Under-voltage lockout event | ≤ 70 µs | 70 µs |
| | | > 70 µs<br>until the VCC_LS exceeds the VCC_LS UV turn ON threshold | UVLO time |

1. *Typical value (-40 °C ≤ $T_J$ ≤ +125 °C)*
2. *Without contribution of the RC network on SD*

Actually, the device remains in a fault condition ($\overline{SD}$ at low logic level and LVGx outputs disabled) for a time also depending on the RC network connected to the $\overline{SD}$ pin. The network generates a time contribution that is added to the internal value.

Figure 4. **Overcurrent timing (without contribution of the RC network on $\overline{SD}$)**

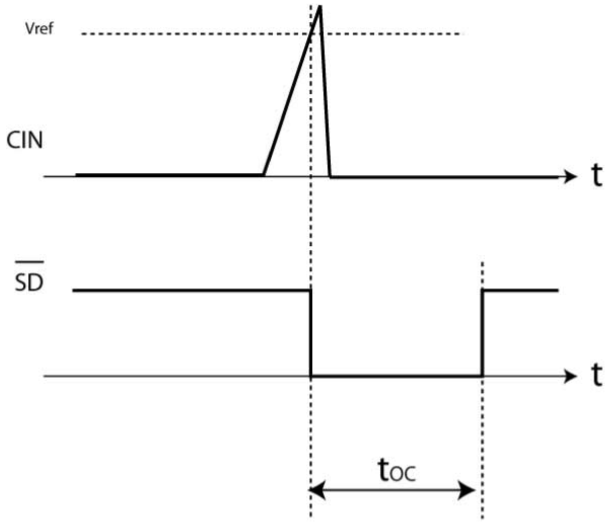


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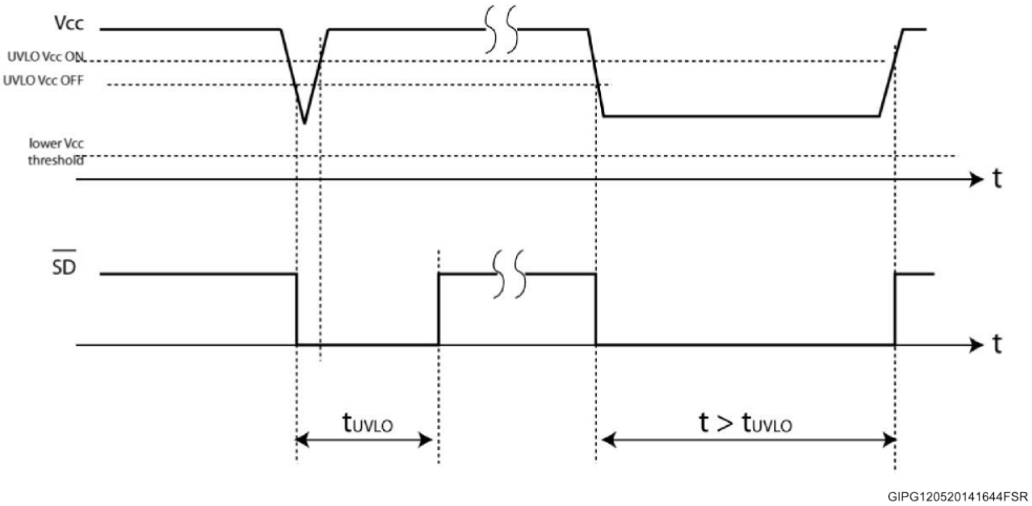
**Figure 5.** UVLO timing (without contribution of the RC network on $\overline{SD}$)

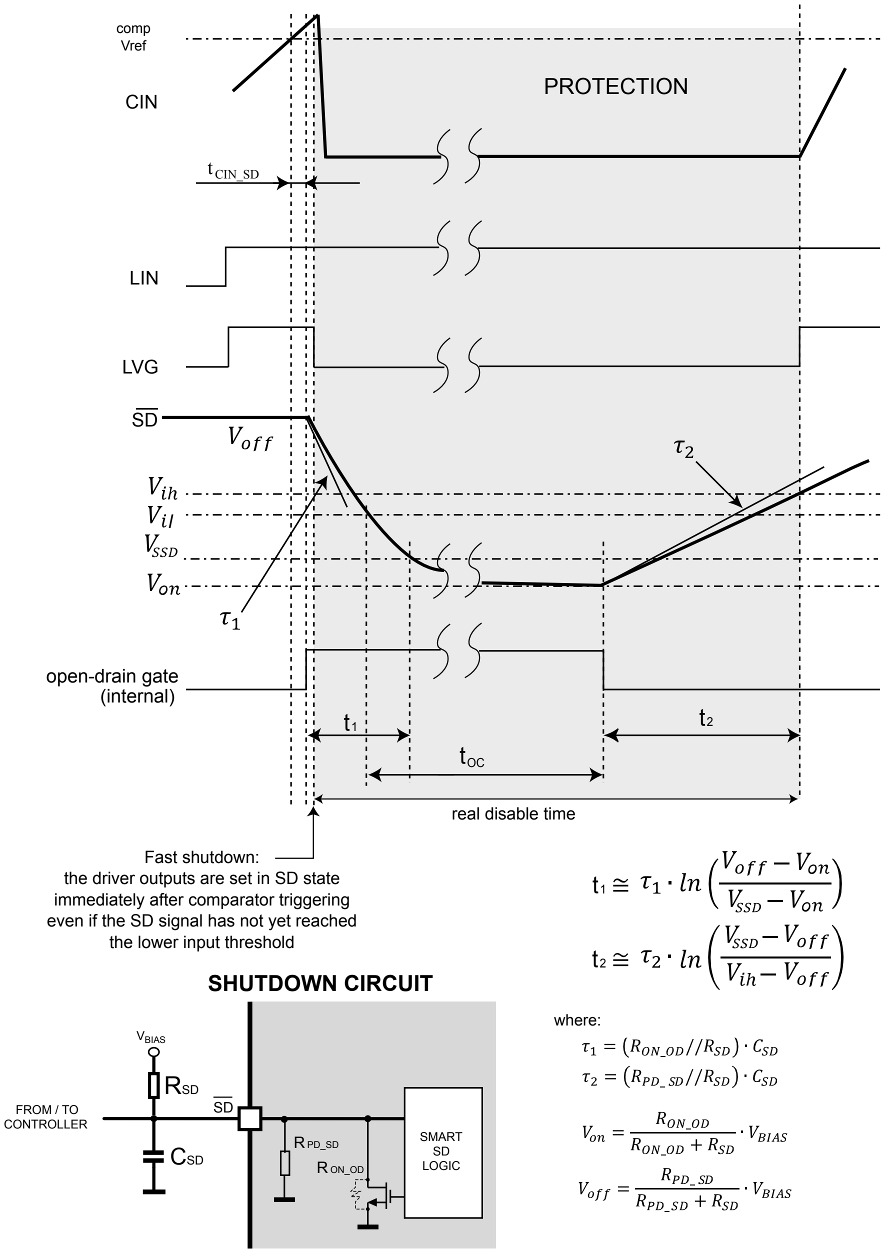


## 4.1 Smart shutdown function

The device integrates a comparator committed to the fault sensing function. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function.

The output signal of the comparator is fed to an integrated MOSFET with the open drain output available on the $\overline{\text{SD}}$ input. When the comparator triggers, the device is set in shutdown state and its outputs are all set to low level.

**Figure 6. Smart shutdown timing waveforms in case of overcurrent event**



$R_{ON\_OD} = V_{OD}/5$ mA, see Table 10. Sense comparator ($V_{CC}$ = 15 V, unless otherwise is specified);

$R_{PD\_SD}$ (typ.) = 5 V/$I_{SDh}$

In common overcurrent protection designs, the comparator output is usually connected to the $\overline{SD}$ input and an RC network is connected to this $\overline{SD}$ line in order to provide a mono-stable circuit which implements a protection time that follows the fault condition.

As opposed to common fault detection systems, the device smart shutdown architecture allows the immediate turn-off of output gates driver in case of fault, by minimizing the propagation delay between the fault detection event and the actual switching off of the outputs. In fact, the time delay between the fault and the turning off of the outputs is no longer dependent on the RC value of the external network connected to the pin.

In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering.

At the same time, the internal logic turns on the open-drain output and holds it on until the $\overline{SD}$ voltage goes below the $V_{SSD}$ threshold and the $t_{oc}$ time is elapsed.

The driver outputs restart following the input pins as soon as the voltage at the $\overline{SD}$ pin reaches the higher threshold of the $\overline{SD}$ logic input.

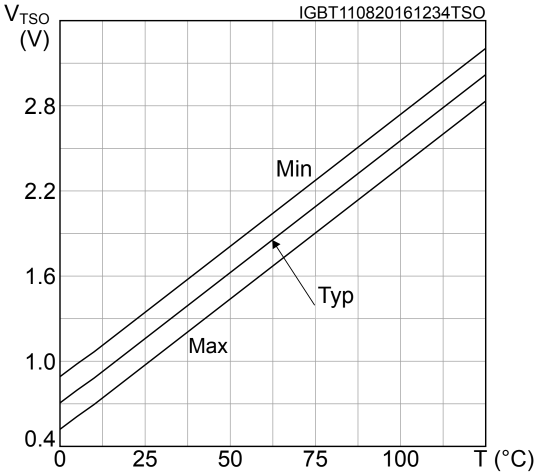
The smart shutdown system provides the possibility to increase the time constant of the external RC network (i.e., the disable time after the fault event) up to very high values without increasing the delay time of the protection.

# 5 Temperature monitoring solution

## 5.1 TSO output

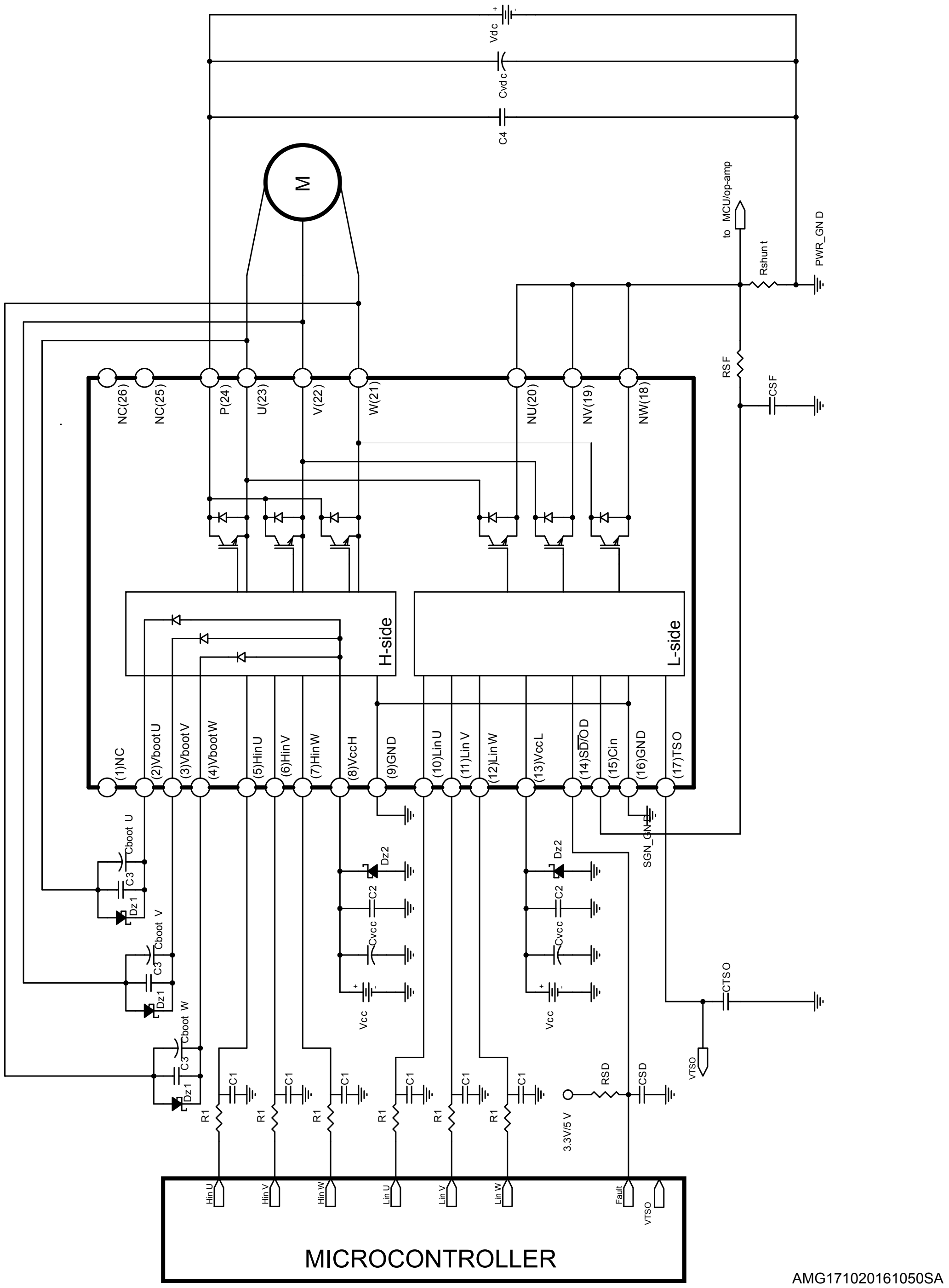
The device integrates a temperature sensor. A voltage proportional to the die temperature is available on the TSO pin. When this function is not used, the pin can be left floating.

Figure 7. $V_{TSO}$ output characteristics vs LVIC temperature



# 6 Application circuit example

**Figure 8.** Application circuit example



Application designers are free to use a different scheme according to the device specifications.

## 6.1 Guidelines

1. Input signals HIN, LIN are active-high logic. A 100 kΩ (typ.) pull-down resistor is built-in for each input pin. To prevent input signal oscillations, the wiring of each input should be as short as possible and the use of RC filters ($R_1$, $C_1$) on each input signal is suggested. The filters should be with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
2. The use of a bypass capacitor $C_{VCC}$ (aluminum or tantalum) can reduce the transient circuit demand on the power supply. Besides, to reduce any high-frequency switching noise distributed on the power lines, a decoupling capacitor $C_2$ (100 to 220 nF, with low ESR and low ESL) should be placed as close as possible to each $V_{cc}$ pin and in parallel with the bypass capacitor.
3. The use of an RC filter ($R_{SF}$, $C_{SF}$) prevents protection circuit malfunctions. The time constant ($R_{SF}$ x $C_{SF}$) should be set to 1 µs and the filter must be placed as close as possible to the CIN pin.
4. The $\overline{SD}$ is an input/output pin (open-drain type if it is used as output). It should be pulled up to a power supply (i.e., MCU bias at 3.3/5 V) by a resistor value, which can keep the $I_{od}$ no higher than 5 mA ($V_{OD} \leq$ 500 mV when open-drain MOSFET is ON). The filter on $\overline{SD}$ should be sized to get a desired re-starting time after a fault event and placed as close as possible to the $\overline{SD}$ pin.
5. A decoupling capacitor $C_{TSO}$ (between 1 nF and 10 nF) placed close to the MCU can be used to increase the noise immunity of the TSO thermal sensor.
6. The decoupling capacitor $C_3$ (100 to 220 nF with low ESR and low ESL) in parallel with each $C_{boot}$ filters high-frequency disturbances. Both $C_{boot}$ and $C_3$ (if present) should be placed as close as possible to the U,V,W and $V_{boot}$ pins. Bootstrap negative electrodes should be connected to the U,V,W terminals directly and separated from the main output wires.
7. To prevent overvoltage on the $V_{CC}$ pin, a Zener diode (Dz1) can be used. Similarly on the $V_{boot}$ pin, a Zener diode (Dz2) can be placed in parallel with each $C_{boot}$.
8. The use of the decoupling capacitor $C_4$ (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor $C_{Vdc}$ prevents surge destruction. Both capacitors $C_4$ and $C_{Vdc}$ should be placed as close as possible to the IPM ($C_4$ has priority over $C_{vdc}$).
9. By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an optocoupler is possible.
10. Low inductance shunt resistors should be used for phase leg current sensing.
11. In order to avoid malfunctions, the wiring on N pins, the shunt resistor and PWR_GND should be as short as possible.
12. The connection of the SGN_GND to the PWR_GND at one point only (close to the shunt resistor terminal) can reduce the impact of power ground fluctuation.

These guidelines ensure the device specifications for application designs. For further details, please refer to the relevant application note.

**Table 12. Recommended operating conditions**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{PN}$ | Supply voltage | Applied among P-Nu, $N_V$, $N_W$ | | 300 | 400 | V |
| $V_{CC}$ | Control supply voltage | Applied to $V_{CC}$-GND | 13.5 | 15 | 18 | V |
| $V_{BS}$ | High-side bias voltage | Applied to $V_{BOOTi}$-$OUT_i$<br>for i = U, V, W | 13 | | 18 | V |
| $t_{dead}$ | Blanking time to prevent arm-short | For each input signal | 1.0 | | | µs |
| $f_{PWM}$ | PWM input signal | -40 °C < $T_C$ < 100 °C<br>-40 °C < $T_J$ < 125 °C | | | 20 | kHz |
| $T_C$ | Case operation temperature | | | | 100 | °C |

# 7 Electrical characteristics (curves)

**Figure 9. Output characteristics**

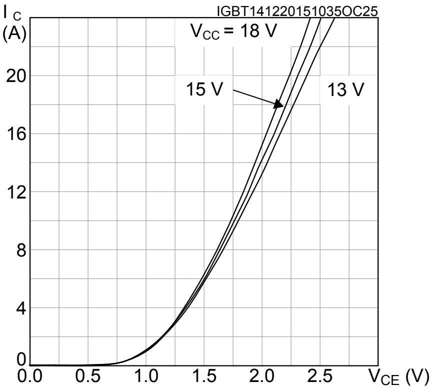


**Figure 10. $V_{CE(sat)}$ vs collector current**

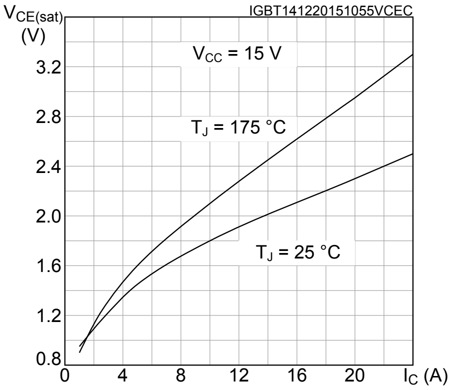


**Figure 11. $I_C$ vs case temperature**

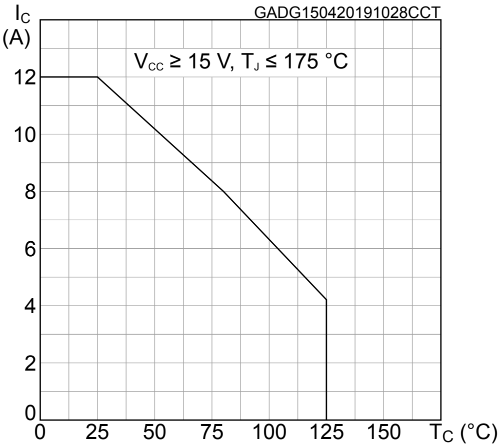


**Figure 12. Diode $V_F$ vs forward current**

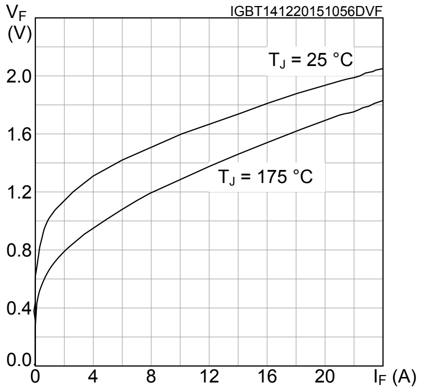


**Figure 13. $E_{on}$ switching energy vs collector current**

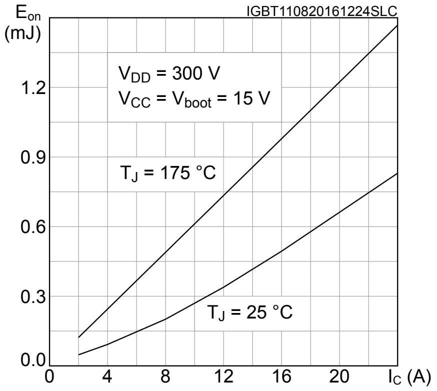


**Figure 14. $E_{off}$ switching energy vs collector current**

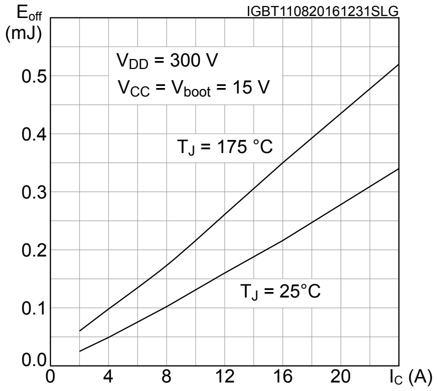
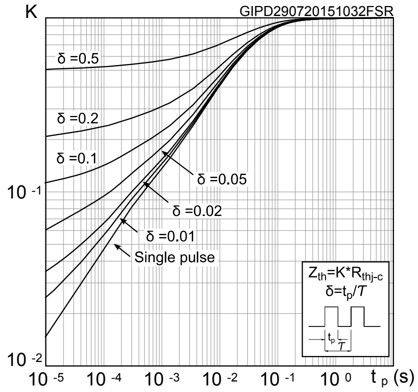


Figure 15. Thermal impedance for IGBT



# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 8.1 SDIP2B-26L type L2 package information

**Figure 16.** **SDIP2B-26L type L2 package outline**

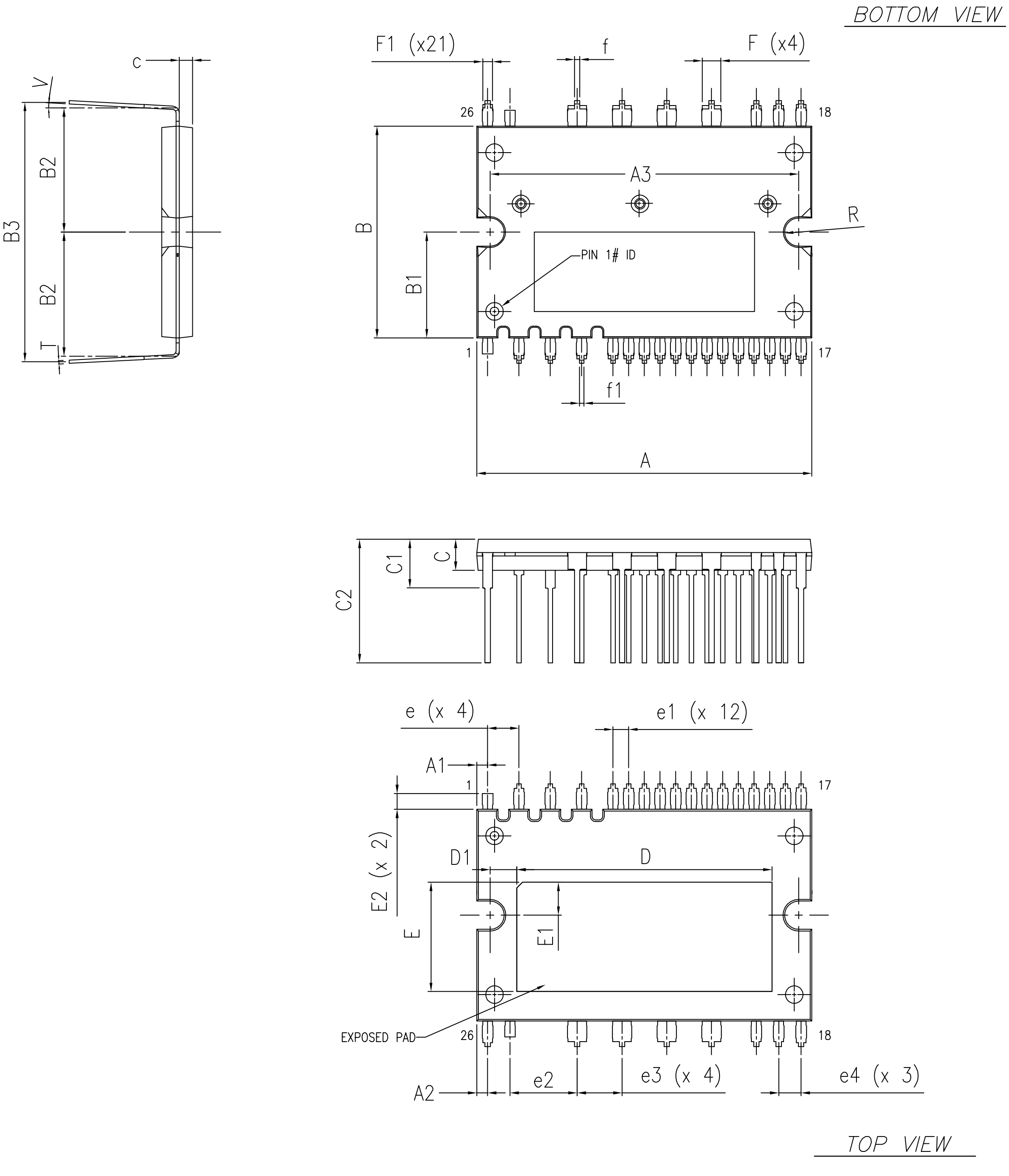


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Table 13. **SDIP2B-26L type L2 package mechanical data**

| Ref. | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 37.50 | 38.00 | 38.50 |
| A1 | 0.97 | 1.22 | 1.47 |
| A2 | 0.97 | 1.22 | 1.47 |
| A3 | 34.70 | 35.00 | 35.30 |
| c | 1.45 | 1.50 | 1.55 |
| B | 23.50 | 24.00 | 24.50 |
| B1 | | 12.00 | |
| B2 | 13.90 | 14.40 | 14.90 |
| B3 | 28.90 | 29.40 | 29.90 |
| C | 3.30 | 3.50 | 3.70 |
| C1 | 5.00 | 5.50 | 6.00 |
| C2 | 13.50 | 14.00 | 14.50 |
| D | 28.45 | 28.95 | 29.45 |
| D1 | 2.725 | 3.025 | 3.325 |
| e | 3.356 | 3.556 | 3.756 |
| e1 | 1.578 | 1.778 | 1.978 |
| e2 | 7.42 | 7.62 | 7.82 |
| e3 | 4.88 | 5.08 | 5.28 |
| e4 | 2.34 | 2.54 | 2.74 |
| E | 11.90 | 12.40 | 12.90 |
| E1 | 3.45 | 3.75 | 4.05 |
| E2 | | 1.80 | |
| f | 0.45 | 0.60 | 0.75 |
| f1 | 0.35 | 0.50 | 0.65 |
| F | 1.95 | 2.10 | 2.25 |
| F1 | 0.95 | 1.10 | 1.25 |
| R | 1.55 | 1.575 | 1.60 |
| T | 0.375 | 0.40 | 0.425 |
| V | 0° | | 5° |

## Revision history

Table 14. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 02-Dec-2016 | 1 | Initial release. |
| 17-May-2018 | 2 | Removed maturity status indication from cover page. The document status is production data.<br>Updated features list on cover page.<br>Updated *Table 11. Fault timing.*<br>Updated *Section 8.1 SDIP2B-26L type L2 package information*.<br>Minor text changes |
| 02-May-2019 | 3 | Added Figure 11. $I_C$ vs case temperature.<br>Minor text changes. |

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