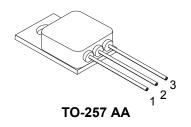
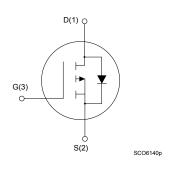


Rad-Hard 100 V, 12 A, P-channel Power MOSFET



The case is not connected to any lead



Product status link STRH12P10

Features

| V _{DS} | I _D | I _D R _{DS(on)} typ. | |
|-----------------|----------------|---|-------|
| 100 V | 12 A | 265 mΩ | 40 nC |

- Fast switching
- 100% avalanche tested
- Hermetic package
- 100 krad TID
- · SEE radiation hardened

Description

The STRH12P10 is a P-channel Power MOSFET developed with the Rad-hard STripFET technology in hermetic TO-257AA package.

Specifically designed to sustain Total Ionized Dose and immunity to heavy ion effects, it is qualified as per ESCC 5205/029 detail specification. In case of discrepancies between this datasheet and the relevant agency specification, the latter takes precedence.

Product summary

| | Product summary | | | | | |
|-----------------|-------------------|---------------------|----------|----------------|--------------------|--|
| Part numbers | Quality level | ESCC part number | Package | Lead finish | Radiation level | |
| STRH12P10GY1 | Engineering model | - | | Gold | - | |
| STRH12P10GYG | ESCC | | TO-257AA | | 100 krad | |
| STRH12P10GYT | ESCC flight | 5205/029 | | Solder dip | 100 krad | |

Note: See Table 8 for ordering information.



1 Electrical ratings

 T_C = 25 °C unless otherwise specified

Table 1. Absolute maximum ratings (pre-irradiation)

| Symbol | Parameter | Value | Unit |
|--------------------------------|--|-------|------|
| V _{DS} | Drain-source voltage (V _{GS} = 0) | 100 | V |
| V _{GS} | Gate-source voltage | ±18 | V |
| I _D ⁽¹⁾ | Drain current (continuous) at T _{case} = 25 °C | 12 | Α |
| iD. | Drain current (continuous) at T _{case} = 100 °C | 7.5 | Α |
| I _{DM} ⁽²⁾ | Drain current (pulsed) | 48 | Α |
| P _{TOT} | Total power dissipation at T _{case} = 25 °C | 75 | W |
| dv/dt ⁽³⁾ | Peak diode recovery voltage slope | 2.4 | V/ns |
| T _{stg} | T _{stg} Storage temperature range | | °C |
| Tj | Max. operating junction temperature range | 150 | °C |

- 1. Rated according to the $R_{thj\text{-case}} + R_{thc\text{-s}}$
- 2. Pulse width limited by safe operating area.
- 3. $I_{SD} \le 12~A$, $di/dt \le 36~A/\mu s$, $V_{DD} = 80~\% V_{(BR)DSS}$.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|---|-------|------|
| R _{thj-case} | R _{thj-case} Thermal resistance junction-case max. | | °C/W |
| R _{thc-s} | R _{thc-s} Thermal resistance case-sink typ. | | °C/W |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|--------------------------------|--|-------|------|
| I _{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max) | 6 | Α |
| E _{AS} ⁽¹⁾ | Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR} , V_{DD} = 50 V) at 110 °C | 112 | mJ |
| E _{AR} | Repetitive pulse avalanche energy $(V_{DS} = 50 \text{ V}, I_{AR} = 6 \text{ A}, f = 10 \text{ KHz},$ $T_J = 25 ^{\circ}\text{C}, \text{ duty cycle} = 50\%)$ | 17 | mJ |
| ⊢AR | Repetitive pulse avalanche energy $(V_{DS} = 50 \text{ V}, I_{AR} = 6 \text{ A}, f = 10 \text{ KHz},$ $T_J = 110 ^{\circ}\text{C}, \text{ duty cycle} = 50\%)$ | 5.5 | mJ |

1. Maximum rating value.

DS8699 - Rev 8 page 2/14



2 Electrical characteristics

For the P-channel MOSFET polarity of voltages and current has to be reversed.

Table 4. Electrical characteristics (T_{amb} = 25 °C unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Max. | Unit | | | |
|-------------------------------------|-----------------------------------|--|------|------|-----------|--|--|--|
| I _{DSS} | Zero gate voltage drain current | 80% V _{(BR)DSS} | | 10 | μA | | | |
| | | V _{GS} = 16 V | | 100 | | | | |
| | Cata hadu laakana ayyyant | V _{GS} = -16 V | -100 | | ^ | | | |
| I _{GSS} | Gate body leakage current | V _{GS} = 16 V, T _C = 125 °C | | 200 | nA 200 | | | |
| | | V _{GS} = -16 V, T _C = 125 °C | -200 | | | | | |
| V _{(BR)DSS} ⁽¹⁾ | Drain-to-source breakdown voltage | V _{GS} = 0 V, I _D = 1 mA | 100 | | V | | | |
| | | $V_{DS} = V_{GS}$, $I_D = 1$ mA | 2.0 | 4.5 | | | | |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 1$ mA, $T_C = 125$ °C | 1.6 | 3.8 | V | | | |
| | | V _{DS} = V _{GS} , I _D = 1 mA, T _C = -55 °C | 2.2 | 5.2 | | | | |
| R _{DS(on)} | Static drain-source on resistance | V _{GS} = 12 V, I _D = 12 A | | 0.30 | Ω | | | |
| C _{iss} ⁽²⁾ | Input capacitance | | 940 | 1410 | pF | | | |
| C _{oss} (2) | Output capacitance | $V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$ | | 205 | pF | | | |
| C _{rss} (2) | Reverse transfer capacitance | | | 85 | pF | | | |
| Qg | Total gate charge | V _{DD} = 50 V, I _D = 12 A, V _{GS} = 12 V | | 48 | nC | | | |
| Q _{gs} | Gate-to-source charge | | | 6.5 | nC | | | |
| Q _{gd} | Gate-to-drain ("Miller") charge | | | 13 | nC | | | |
| t _{d(on)} | Turn-on delay time | | | 13 | ns | | | |
| t _r | Rise time | | | 31 | ns | | | |
| t _{d(off)} | Turn-off delay time | V_{DD} = 50 V, I_{D} = 6 A, R_{G} = 4.7 Ω , V_{GS} = 12 V | 18 | 42 | ns | | | |
| t _f | Fall time | | 3.5 | 10.5 | ns | | | |
| I _{SD} | Source-drain current | | | 12 | Α | | | |
| I _{SDM} ⁽³⁾ | Source-drain current (pulsed) | | | 48 | Α | | | |
| ., | | I _{SD} = 12 A, V _{GS} = 0 V | | 1.5 | | | | |
| V_{SD} | Forward on voltage | I _{SD} = 12 A, V _{GS} = 0 V, T _C = 125 °C | | 1.25 | V | | | |
| t _{rr} | Reverse recovery time | | 178 | 258 | ns | | | |
| Q _{rr} | Reverse recovery charge | I_{SD} = 12 A, di/dt = 40 A/µs, V_{DD} = 60 V, T_j = 25 °C | | 2560 | nC | | | |
| I _{RRM} | Reverse recovery current | | | 24 | Α | | | |
| t _{rr} | Reverse recovery time | | 225 | 335 | ns | | | |
| Q _{rr} | Reverse recovery charge | I _{SD} = 12 A, di/dt = 40 A/μs, V _{DD} = 60 V, T _J = 150 °C | 2650 | 3950 | nC | | | |
| I _{RRM} | Reverse recovery current | | 18.5 | 28.5 | Α | | | |

^{1.} This rating is guaranteed at $T_J \le 25$ °C (see Figure 9. Normalized $V_{(BR)DSS}$ vs temperature).

DS8699 - Rev 8 page 3/14

^{2.} Not tested, guaranteed by process.

^{3.} Pulse width limited by safe operating area



3 Radiation characteristics

This products is guaranteed in radiation as per ESCC 5205/029 and ESCC 22900 specification at 100 krad. Each lot tested in radiation is accepted according to the characteristics as per Table 5.

3.1 Total dose radiation (TID) testing

The bias with VGS = + 15 V and VDS = 0 V is applied during irradiation exposure.

The parameters listed in Table 5 are measured:

- Before irradiation
- After irradiation
- After 24 hrs at room temperature
- after 168 hrs at 100 °C anneal

Table 5. Post-irradiation electrical characteristics (T_{amb} = 25 °C unless otherwise specified)

| Symbol | Parameter | Test conditions | Drift values Δ | Unit | |
|--------------------------------------|---|--|-----------------------------|------|--|
| I _{DSS} | Zero gate voltage drain current (V _{GS} = 0) | 80% V _{(BR)DSS} | +1 | μA | |
| 1 | Coto hadulaalaana surrant | V _{GS} = 12 V | 1.5 | nA | |
| I _{GSS} | Gate body leakage current | V _{GS} = -12 V | , I _D = 1 mA +5% | | |
| V _{(BR)DSS} | Drain-to-source breakdown voltage | V _{GS} = 0 V, I _D = 1 mA | +5% | V | |
| V _{GS(th)} | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$ | + 150% | V | |
| R _{DS(on)} | Static drain-source on resistance | V _{GS} = 10 V, I _D = 12 A | -4% / +35% | Ω | |
| Qg | Total gate charge | | -15% / +5% | | |
| Q _{gs} | Gate-to-source charge | $V_{DS} = 50 \text{ V, } I_{G} = 1 \text{ mA, } V_{GS} = 12 $ V, $I_{DS} = 12 \text{A}$ | -5% / +200% | nC | |
| Q _{gd} Gate-to-drain charge | | | -10% / +100% | | |
| V _{DS} (1) | Forward on voltage | V _{GS} = 0 V, I _{SD} = 12 A | ±5% | V | |

^{1.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

DS8699 - Rev 8 page 4/14



3.2 Single event effect SOA

This products is extremely resistant to heavy ion environment for single event effect (as per MIL-STD-750E, method 1080, bias circuit of Figure 2).

SEB and SEGR tests are performed with a fluence of 3e+5 ions/cm² with the following acceptance criteria:

- SEB (test): drain voltage checked, trigger level is set to V_{DS} = 5 V. Stop condition: as soon as a SEB occurs or if the fluence reaches 3e+5 ions/cm².
- SEGR test: the gate current is monitored every 200 ms. A gate stress is performed before and after irradiation. Stop condition: as soon as the gate current reaches 100 nA (during irradiation or during PIGS test) or if the fluence reaches 3e+5 ions/cm².

| lon | Let (Mev/(mg/cm²) | Energy (MeV) | Range (μm) |
|-----|-------------------|-----------------|---------------|
| Kr | 32 | 768 | 94 |
| KI | 32 | 756 | 92 |
| Cu | 28 | 285 | 43 |
| Xe | 60 | 1217 | 89 |

Table 6. Single event effect (SEE), safe operating area (SOA)



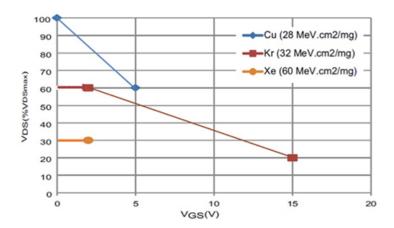
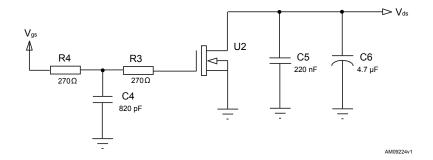


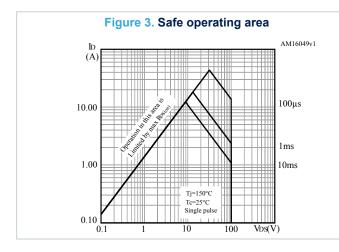
Figure 2. Single event effect, bias circuit



DS8699 - Rev 8 page 5/14



4 Electrical characteristics (curves)



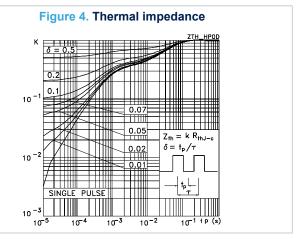
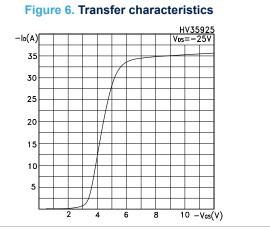
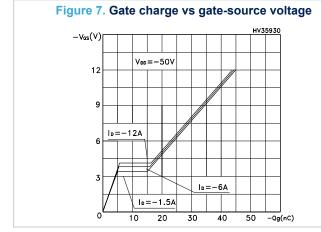
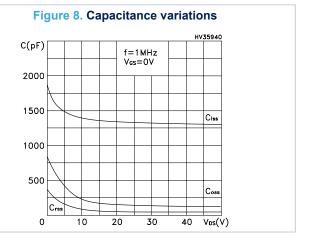


Figure 5. Output characteristics

-lo(A)
-lo







DS8699 - Rev 8 page 6/14



Figure 9. Normalized V_{(BR)DSS} vs temperature

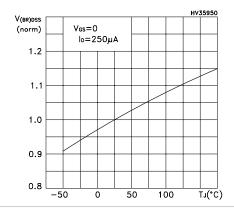


Figure 10. Static drain-source on-resistance

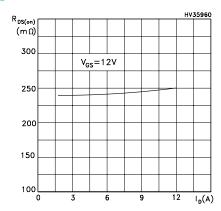


Figure 11. Normalized gate threshold voltage vs temperature

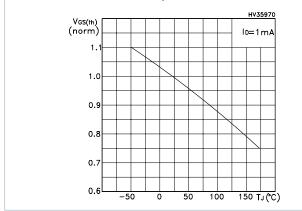


Figure 12. Normalized on-resistance vs temperature

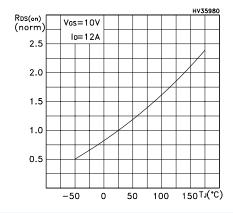
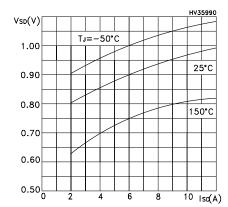


Figure 13. Source drain-diode forward characteristics

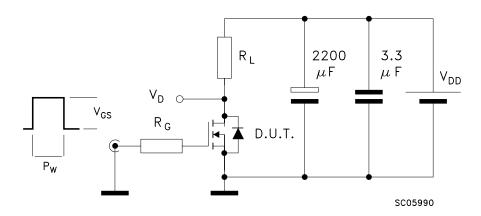


DS8699 - Rev 8 page 7/14



Test circuits 5

Figure 14. Switching times test circuit for resistive load



Note: $Max driver V_{GS} slope = 1V/ns (no DUT)$

Figure 15. Source drain diode waveform

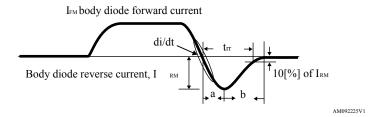
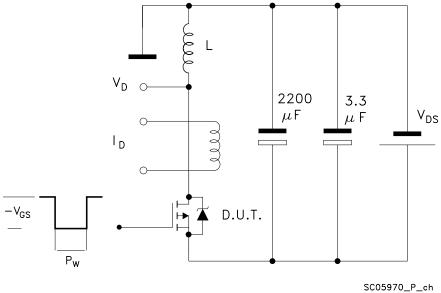


Figure 16. Unclamped inductive load test circuit (single pulse and repetitive)



DS8699 - Rev 8 page 8/14

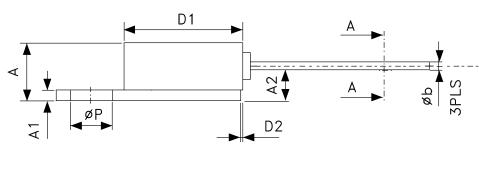


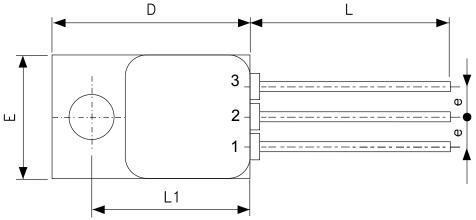
6 Package information

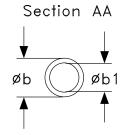
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 TO-257AA package information

Figure 17. TO-257AA package outline







Pin 1: Drain Pin 2: Source Pin 3: Gate

0117268 E

DS8699 - Rev 8 page 9/14



Table 7. TO-257AA package mechanical data

| Cumbala | D | imensions (m | m) | D | imensions (inche | es) |
|---------|-------|--------------|-------|-------|------------------|-------|
| Symbols | Min. | Тур. | Max. | Min. | Тур. | Max. |
| А | 4.83 | | 5.08 | 0.190 | | 0.200 |
| A1 | 0.89 | | 1.14 | 0.035 | | 0.045 |
| A2 | | 3.05 | | | 0.120 | |
| b | 0.64 | | 1.02 | 0.025 | | 0.040 |
| b1 | 0.64 | 0.76 | 0.89 | 0.025 | 0.030 | 0.035 |
| D | 16.38 | | 16.89 | 0.645 | | 0.665 |
| D1 | 10.41 | | 10.92 | 0.410 | | 0.430 |
| D2 | - | - | 0.97 | | | 0.038 |
| е | | 2.54 | | | 0.100 | |
| E | 10.41 | | 10.67 | 0.410 | | 0.420 |
| L | 15.24 | | 16.51 | 0.600 | | 0.650 |
| L1 | 13.39 | | 13.64 | 0.527 | | 0.537 |
| Р | 3.56 | | 3.81 | 0.140 | | 0.150 |

Note: The case is not connected to any lead.

DS8699 - Rev 8 page 10/14



7 Order codes

Table 8. Ordering information

| Part number | Agency specification | Quality level | Radiation level | Package | Weight | Lead finish | Marking ⁽¹⁾ | Packing |
|--------------|----------------------|---------------|----------------------|------------|--------|----------------|------------------------|---------|
| CTDU42D40CV4 | | Engineering | | | | | STRH12P10GY1 | |
| STRH12P10GY1 | | model | - | | | Gold | + BeO | |
| STRH12P10GYG | 5205/029/01 | | 100 kmd TO 25744 F a | | Gold | 520502901R | Ctrin nools | |
| SIRHIZPIUGIG | 5205/029/01 | | 257AA 5 g | | + BeO | Strip pack | | |
| STRH12P10GYT | ESCC flight 100 krad | | Solder | 520502902R | | | | |
| 31KH12P10G11 | 5205/029/02 | | 100 krad | | | dip | + BeO | |

Specific marking only. The full marking includes in addition: For the Engineering Models: ST logo, date code; country of origin (FR). For ESCC flight parts: STlogo, date code, country of origin (FR), ESA logo, serial number of the part within the assembly lot.

Contact ST sales office for information about the specific conditions for products in die form.

DS8699 - Rev 8 page 11/14



8 Other information

8.1 Traceability information

Date code information is described in the table below.

Table 9. Date codes

| Model | Date code |
|-------|-----------|
| EM | 3yywwN |
| ESCC | yywwN |

^{1.} yy = year, ww = week number, N = lot index in the week.

8.2 Documentation

Table 10. Documentation provided for each type of product

| Quality level | Radiation level | Documentation |
|-------------------|-----------------|---|
| Engineering model | - | Certificate of conformance |
| | | Certificate of conformance |
| ESCC | 100 krad | ESCC qualification maintenance lot reference |
| | | Radiation data at 25 / 50 / 70 / 100 krad at 0.1 rad / s. |

DS8699 - Rev 8 page 12/14



Revision history

Table 11. Document revision history

| Date | Version | Changes |
|-------------|---------|--|
| 07-Oct-2011 | 1 | First release. |
| 24-Jun-2013 | 2 | Document status promoted form preliminary data to production data. |
| | | - Modified: Figure 1 |
| | | - Modified: EAS, EAR parameter and values in Table 4 |
| | | - Modified: IGSS, and added note 1 in Table 5 |
| | | - Added: note 1 in Table 6 |
| | | - Modified: trr, qrr and IRRM parameter in Table 8 |
| | | Modified: RDS(on) test conditions in Table 9, the entire test conditions in Table 10 |
| | | - Modified: Figure 4 |
| 25-Nov-2013 | 3 | - Modified: package drawing and Figure 1. |
| 18-Dec-2013 | 4 | - Updated Table 1: Device summary and Table 14: Ordering information. |
| | | - Updated Section : Total dose radiation (TID) testing. |
| 19-Jan-2015 | 5 | - Updated Table 13.: TO-257AA mechanical data |
| | | - Minor text changes |
| 02-May-2019 | 6 | Updated Table 7. Pre-irradation source drain diode and Table 4. Preirradiation on/off states. |
| | | Minor text changes |
| 29-Feb-2020 | 7 | Updated Table 10 and TO-257 AA package information. |
| 21-Jan-2021 | 8 | Updated Product summary, Table 4, Table 5, Table 6, Figure 1, Table 8 and Table 10. |

DS8699 - Rev 8 page 13/14



IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2021 STMicroelectronics - All rights reserved

DS8699 - Rev 8 page 14/14