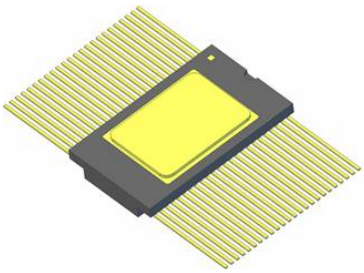
RHFLVDS217

Datasheet

Rad-hard LVDS serializer

Ceramic Flat-48



The upper metallic lid is connected to pin 17

Product status link
RHFLVDS217

Features

- 15 to 75 MHz shift clock support
- Fail-safe function
- 8 kV HBM on LVDS pins
- Power-down mode < 216 µW (max.)
- Cold sparing all pins
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Mbytes/s bandwidth
- 325 mV (typ.) LVDS swing
- PLL requires no external components
- Rising edge strobe
- Operational environment: total dose irradiation testing to MIL-STD-883 method 1019
  - Total dose: 300 krad (Si)
  - Latch-up immune (LET > 120 MeV-cm2/mg)
- Compatible with ANSI/TIA/EIA-644 standard

Description

The RHFLVDS217 serializer converts 21 bits of CMOS/TTL data into three LVDS (low voltage differential signaling) data streams. A phase-locked transmitter clock is transmitted in parallel with the data streams over a fourth LVDS link. With every cycle of the transmitter clock, 21 bits of input data are sampled and transmitted.

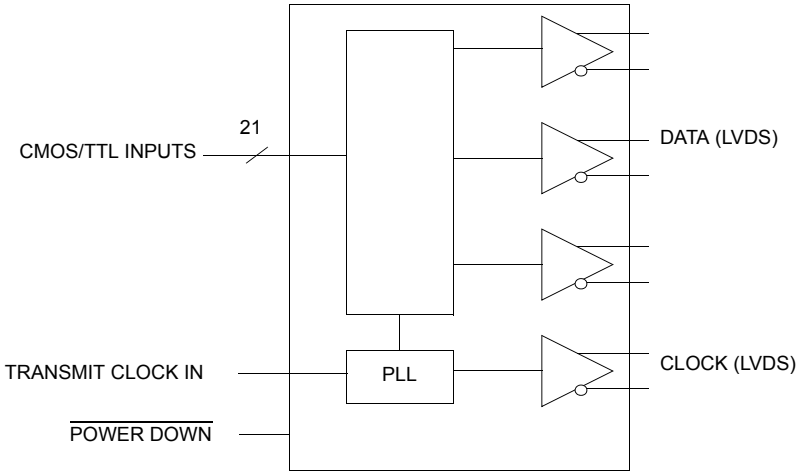
At a transmitter clock frequency of 75 MHz, 21 bits of TTL data are transmitted at a rate of 525 Mbps per LVDS data channel. Using a 75 MHz clock, the data throughput is 1.575 Gbit/s (197 Mbytes/s).

The RHFLVDS217 serializer allows the use of wide, high speed TTL interfaces while reducing overall EMI and cable size.

All pins have cold spare buffers. These buffers are high impedance when V_{CC} is tied to 0 V.

1 Functional description

Figure 1. **RHFLVDS217 serializer functional block diagram**

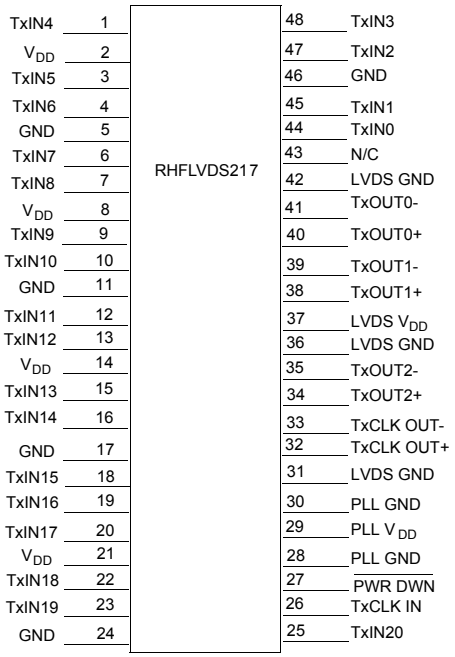


2 Pin configuration

Table 1. Pin description

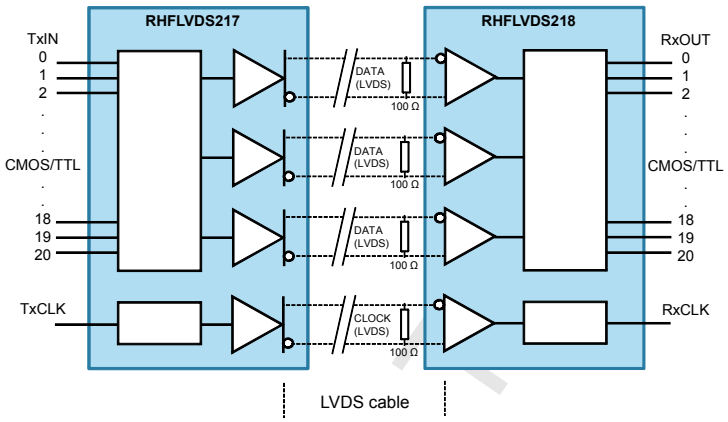
Pin name	I/O	Number	Description
TxIN	I	21	TTL level input
TxOUT+	O	3	Positive LVDS differential data output
TxOUT-	O	3	Negative LVDS differential data output
TxCLK IN	I	1	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT-	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DWN}}$	I	1	TTL level input. Assertion (low input) TRISTATEs the clock and data outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL inputs and logic
GND	I	5	Ground pins for TTL inputs and logic
PLL V_{CC}	I	1	Power supply pins for PLL
PLL GND	I	2	Ground pins for PPL
LVDS V_{CC}	I	1	Power supply pin for LVDS output
LVDS GND	I	3	Ground pins for LVDS outputs

Figure 2. RHFLVDS217 pinout



3 Typical application

Figure 3. **RHFLVDS217 typical application**



4 Absolute maximum ratings and operating conditions

Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond the limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

Table 2. Absolute maximum ratings (references to GND)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		4.8	V
V_i	TTL inputs (operating or cold-spare)		-0.3 to 4.8	
T_{stg}	Storage temperature range		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thjc}	Thermal resistance junction to case (2)		10	°C/W
ESD	HBM: human body model	All pins except LVDS outputs	2	kV
		LVDS outputs vs. GND	8	
	CDM: charge device model		500	V

1. *All voltages, except the differential I/O bus voltage, are with respect to the network ground terminal.*
2. *Test per MIL-STD-883, method 1012. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.*

Table 3. Recommended operating conditions (referenced to GND)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IN}	Driver DC input voltage (TTL inputs)	0		VCC	
T_A	Ambient temperature range	-55		125	°C

5 Electrical characteristics

In Table 4. DC electrical characteristics, V_{CC} = 3 V to 3.6 V, - 55 °C < T_A < 125 °C, unless otherwise specified, T_A is per the temperature noted. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.

Table 4. DC electrical characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
CMOS/TTL DC specifications					
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		GND	0.8	
I_{IH}	High-level input current	V_{IN} = 3.6 V, V_{CC} = 3.6 V	-10	10	µA
I_{IL}	Low-level input current	V_{IN} = 0 V, V_{CC} = 3.6 V	-10	10	
V_{CL}	Input clamp voltage	I_{CL} = -18 mA		-1.5	V
I_{CS}	Cold spare leakage current	V_{IN} = 3.6V, V_{CC} = 0 V	-20	20	µA
LVDS output DC specifications (OUT+, OUT-)					
V_{OD} (1)	Differential output voltage	R_L = 100 ohm (see Figure 14. Driver V_{OD} and V_{OS} test circuit or equivalent circuit)	250	400	mV
DV_{OD} (1)	Change in V_{OD} between complimentary output states	R_L = 100 ohm (see Figure 14. Driver V_{OD} and V_{OS} test circuit or equivalent circuit)		35	
V_{OS} (1)	Offset voltage	R_L = 100 ohm, V_{OS} = (V_{OH} + V_{OL})/2	1.125	1.450	V
DV_{OS} (1)	Change in V_{OS} between complimentary output states	R_L = 100ohm		35	mV
I_{OZ}	Output three-state current	PWR DWN = 0 V V_{OUT} = 0 V or V_{CC}	-10	10	µA
I_{OS} (2)	Output short circuit current	V_{OUT}^+ or V_{OUT}^- = 0 V	3.5	9	mA
I_{CSOUT}	Cold spare leakage current	V_{IN} = 3.6 V, V_{CC} = 0 V	-20	20	µA
Supply current					
I_{CCL}	Transmitter supply current with loads	R_L = 100 ohm all channels C_L = 5 pF, f = 50 MHz, (see Figure 5. RHFLVDS217 output load and transition times)		65	mA
I_{CCZ}	Power down current	D_{IN} = V_{CC} or 0 V, PWR DWN = 0 V, f = 0 Hz		200	µA

1. *Clock outputs guaranteed by design.*
2. *Output short-circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, for a maximum duration of one second.*

In Table 5. AC switching characteristics, V_{CC} = 3 V to 3.6 V, - 55 °C < T_A < 125 °C, unless otherwise specified, T_A is per the temperature noted. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25 °C per MIL-STD-883 Method 1019, condition A up to the maximum TID level procured. The recommend transition time for TXCLK In is 1.0 to 6.0 ns (see Figure 6. RHFLVDS217 input clock transition time)

Table 5. AC switching characteristics

Symbol	Parameter	Min.	Max.	Unit
LLHT (1)	LVDS low-to-high transition time (seeFigure 5. RHFLVDS217 output load and transition times)		1.5	ns
LHLT (1)	LVDS high-to-low transition time (see Figure 5. RHFLVDS217 output load and transition times)		1.5	
TPPos0 (1)	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 50 MHz	0.07	0.24	
	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 75 MHz	0.08	0.30	
TPPos1 (1)	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 50 MHz	2.84	3.26	
	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 75 MH	1.98	2.30	
TPPos2 (1)	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 50 MHz	5.63	5.98	
	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 75 MHz	3.85	4.13	
TPPos3 (1)	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 50 MHz	8.58	9.07	
	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 75 MHz	5.79	6.14	
TPP0s4 (1)	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 50 MHz	11.14	11.66	
	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 75 MHz	7.54	7.89	
TPP0s5 (1)	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 50 MHz	14.20	14.54	
	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 75 MHz	9.52	9.78	
TPP0s6 (1)	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 50 MHz	17.00	17.46	
	Transmitter output pulse position for bit 0 (see Figure 13. RHFLVDS217 output pulse position measurement), f = 75 MHz	11.41	11.76	
TCCS (2)	Channel-to-channel skew (see Figure 7. RHFLVDS217 channel-to-channel skew), f = 75 MHz		0.45	
TCIP (1) (2)	TxCLK IN period (see Figure 8. RHFLVDS217 setup/hold and high/low times)	13.3	66.7	
TCIH (3) (2)	TxCLK IN high time (see Figure 8. RHFLVDS217 setup/hold and high/low times)	0.35 T_{cip}	0.65 T_{cip}	
TCIL (2) (3)	TxCLK IN low time (see Figure 8. RHFLVDS217 setup/hold and high/low times)	0.35 T_{cip}	0.65 T_{cip}	
TSTC (1) (2)	TxIN setup to TxCLK IN (see Figure 8. RHFLVDS217 setup/hold and high/low times), 15 MHz	1.0		
	TxIN setup to TxCLK IN (see Figure 8. RHFLVDS217 setup/hold and high/low times), 75 MHz	0.5		
THTC (1) (2)	TxIN hold to TxCLK IN (see Figure 8. RHFLVDS217 setup/hold and high/low times), 15 MHz	0.7		
	TxIN hold to TxCLK IN (see Figure 8. RHFLVDS217 setup/hold and high/low times), 75 MHz	0.5		
TCCD (2)	TxCLK IN to TxCLK OUT delay (see Figure 9. RHFLVDS217 clock-to-clock out delay)	0.5	3	

Symbol	Parameter	Min.	Max.	Unit
TPLLS (4) (2)	Transmitter phase lock loop set (see Figure 10. RHFLVDS217 phase-lock-loop set time)		10	ms
TPDD	Transmitter power down delay (see Figure 12. Transmitter power-down delay)		100	µs

1. *Guaranteed by characterization.*
2. *Recommended transition time for TxCLK IN is 1 to 6 ns (see Figure 6. RHFLVDS217 input clock transition time)*
3. *Guaranteed by design*
4. *Functionally tested*

Cold sparing

The RHFLVDS217 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (VCC = GND) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and VCC. ESD protection is ensured through a non-conventional dedicated structure.

Fail-safe

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of TTL floating inputs, the LVDS outputs remain in a stable logic-high state.

6 Radiations

Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDS217 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in Table 4. DC electrical characteristics apply to both pre- and post-irradiation, as follows:

- All tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy-ions

The behavior of the product when submitted to heavy-ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiation

Type	Characteristics	Value	Unit
TID(1)	High-dose rate (50 - 300 rad/s) up to:	300	krad
Heavy-ions	SEL(2) immune up to: (with a particle angle of 60 ° at 125 °C) and a fluence of 1e+7 cm^{-2})	120	MeV.cm²/mg
	SEL (2) immune up to: (with a particle angle of 0 ° at 125 °C) and a fluence of 1e+7 cm^{-2})	60	

1. *A total ionizing dose (TID) of 300 krad(Si) is equivalent to 3000 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latch-up.*

7 Test circuit and AC timing diagrams

Figure 4. Test pattern

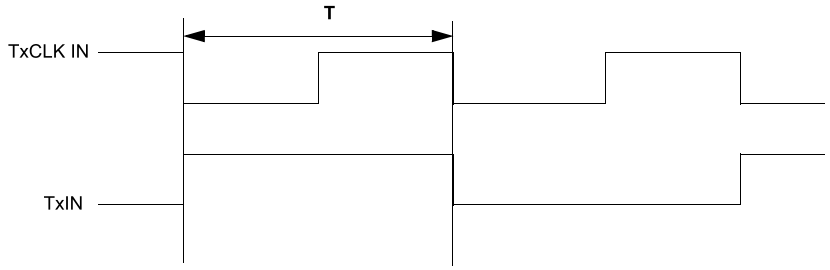


Figure 5. RHFLVDS217 output load and transition times

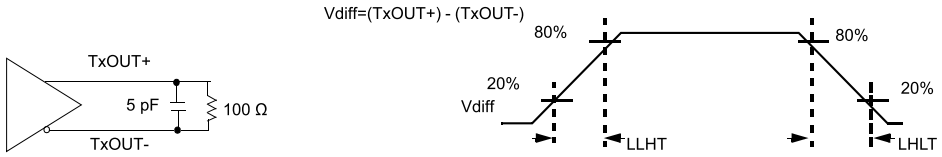


Figure 6. RHFLVDS217 input clock transition time

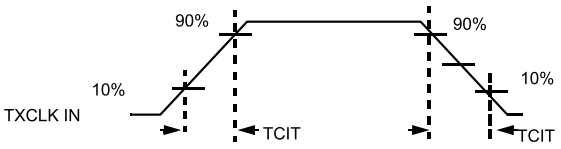
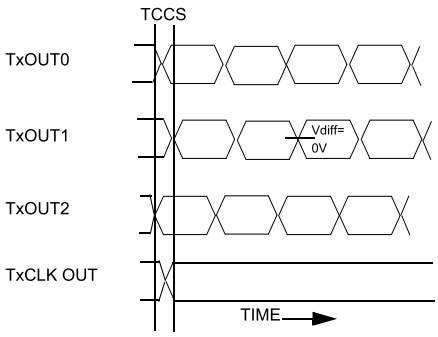


Figure 7. RHFLVDS217 channel-to-channel skew



1. Measurements at V_{DIFF} = 0 V
2. TCCS measured between earliest and latest LVDS edges
3. TxCLK differential low-high edge

Figure 8. RHFLVDS217 setup/hold and high/low times

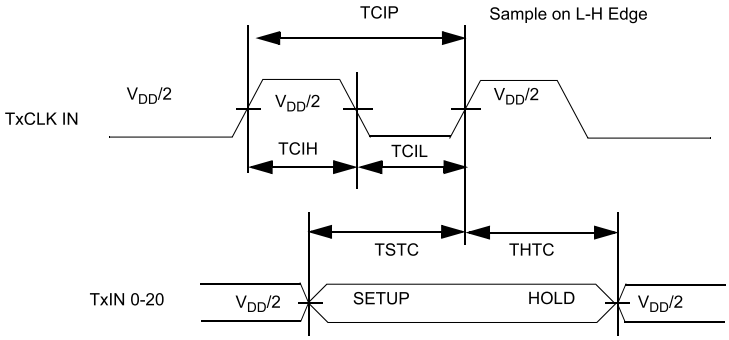


Figure 9. RHFLVDS217 clock-to-clock out delay

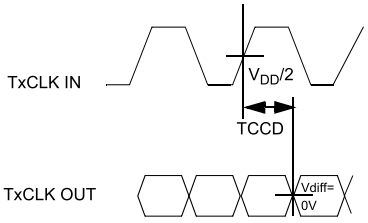


Figure 10. RHFLVDS217 phase-lock-loop set time

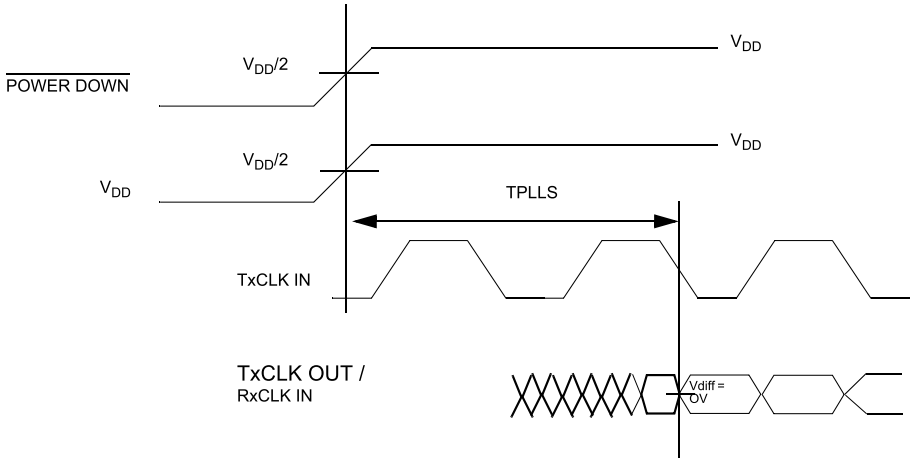


Figure 11. RHFLVDS217 parallel TTL data inputs mapped to LVDS outputs

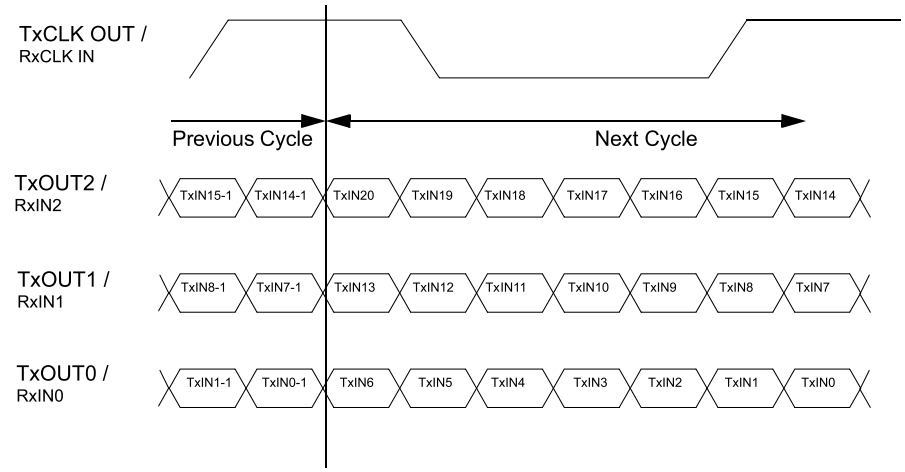


Figure 12. Transmitter power-down delay

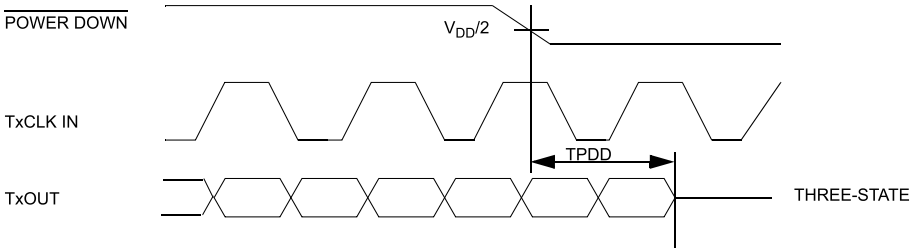


Figure 13. **RHFLVDS217 output pulse position measurement**

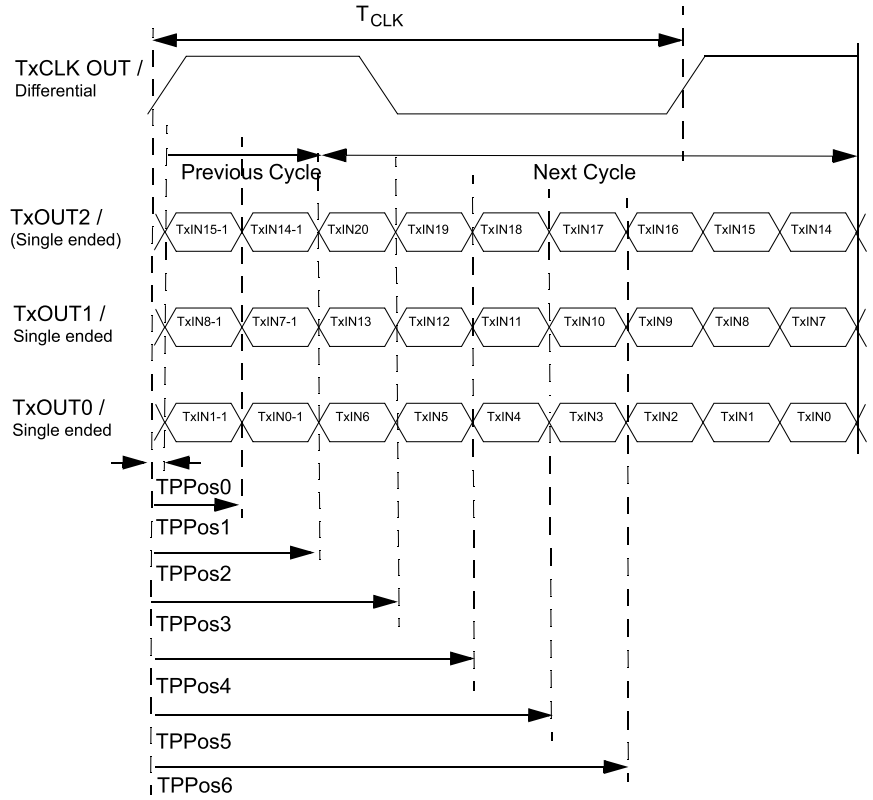
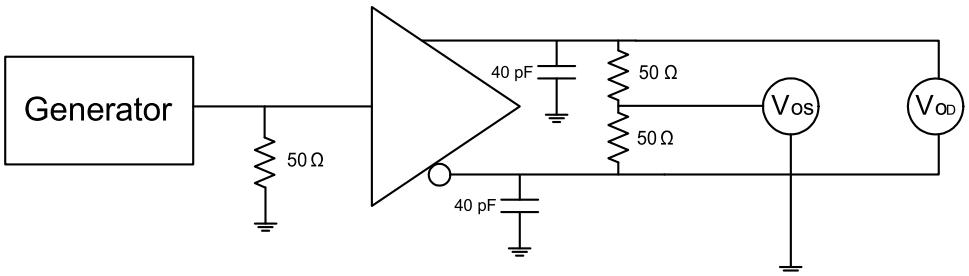


Figure 14. **Driver V_{OD} and V_{OS} test circuit or equivalent circuit**

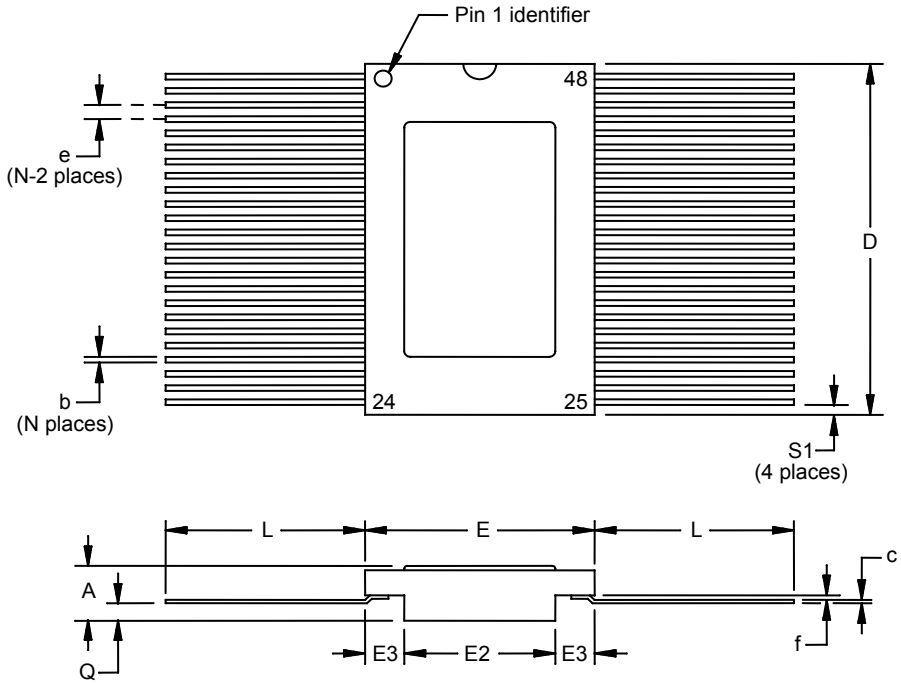


8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 Ceramic Flat-48 package information

Figure 15. Ceramic Flat-48 package outline



1. The upper metallic lid is connected to pin 17.

Table 7. Ceramic Flat-48 mechanical data

Dim.	mm			Inches		
	Typ	Min.	Max.	Typ.	Min.	Max.
A	2.47	2.18	2.72	0.097	0.086	0.107
b	0.254	0.20	0.30	0.010	0.008	0.012
c	0.15	0.12	0.18	0.006	0.005	0.007
D	15.75	15.57	15.92	0.620	0.613	0.627
E	9.65	9.52	9.78	0.380	0.375	0.385
E2	6.35	6.22	6.48	0.250	0.245	0.255
E3	1.65	1.52	1.78	0.065	0.060	0.070
e	0.635			0.025		
f	0.20			0.008		
L	8.38	6.85	9.40	0.330	0.270	0.370
Q	0.79	0.66	0.92	0.031	0.026	0.036
S1	0.43	0.25	0.61	0.017	0.010	0.024

9 Ordering information

Table 8. Order code

Order code	SMD[1]	Quality level	Temp. range	Mass	Package	Lead finish	Marking[2]	Packing
RHFLVDS217K1	-	Engineering model	-55 to +125 °C	1.22 g	Flat-48	Gold	RHFLVDS217K1	Conductive strip pack
RHFLVDS217K01V	5962F01534	QML-V flight					5962F0153403VYC	

1. *Standard microcircuit drawing.*
2. *Specific marking only. Complete marking includes the following:*
   - *ST logo*
   - *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
   - *Country of origin (FR = France)*

Note: Contact your ST sales office for information about the specific conditions for products in die form.

Other information

Date code:

The date code is structured as engineering model: EM xyywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 9. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including : Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID

Quality level	Item
QML-V Flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
08-Apr-2016	1	Initial release
03-Oct-2016	2	Status of datasheet changed from "preliminary data" to "production data". Added order code RHFLVDS217K01V to Table 1: "Device summary" Table 3: "Absolute maximum ratings (references to GND)": updated Rthjc value from 22 °C/W to 10 °C/W; updated footnote 2. Table 5: "DC electrical characteristics": updated ICCZ condition; updated footnotes. Table 6: "AC switching characteristics": updated footnotes Added order code RHFLVDS217K01V to Table 9: "Order codes"
04-Jul-2018	3	Updated Section 5 Electrical characteristics, Section 6 Radiations and Section 9 Ordering information.

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