ST60A2G0

Data brief

60 GHz RF transceiver for short-range contactless connectivity

VFBGA25 (2.2 x 2.2 x 0.8 mm)

Product status link
ST60A2G0

Features

- 60 GHz V-Band transceiver for short range contactless connectivity
- Up to 6.25 Gbit/s data rate
- Compact solution integrating full RF transceiver operating in half-duplex mode
- Low-power ASK modulation scheme supported
- Differential SLVS input-output port (NRZ) or single-ended CMOS 1.8 V bidirectional data for low data rate (9.6 Kbit/s to 100 Mbit/s with 15 pF PCB load)
- 24 dB typical total link budget
- 7 ns typical latency
- Supply voltage: power-optimized dual 1.8 V and 1.45 V supply or single-supply 1.8 V
- Low power consumption (typical values at 5 Gbit/s)
  - 44 mW in TX mode
  - 27 mW in RX mode
  - 3.5 µW in OFF mode
- 7 pJ/bit for TX and 5.4 pJ/bit for RX at maximum data rate
- 50 Ω single-ended nominal RF input/output impedance with recommended PCB transition
- Operating temperatures:
  - consumer range: -20 to 85°C
  - industrial range: -40 to 105°C
- Package: VFBGA 2.2 mm x 2.2 mm x 0.8 mm, 25 balls, F5x5, 0.4 mm pitch
- Optimized BOM without external matching network and clock references

Description

The ST60A2G0 is an RF millimeter-wave transceiver product operating in the 60 GHz V-Band. It provides a very power efficient and high data-rate wireless link enabling freedom from physical cables and connectors for short-range (a few cm) point-to-point communications, using a variety of external antennas (such as patch antennas designed on PCB or highly directive SMT horn antennas allowing both end-fire and broadside radiation patterns).

The ST60A2G0 offers best-in-class wireless performance with transfer speeds up to 6.25 Gbit/s, along with very low power consumption. Its unmatched efficiency, very small form factor, and innovative architecture designed for optimized system bill-of-materials, make it ideally suited for a wide range of applications including personal electronics, industrial, computer and peripherals.

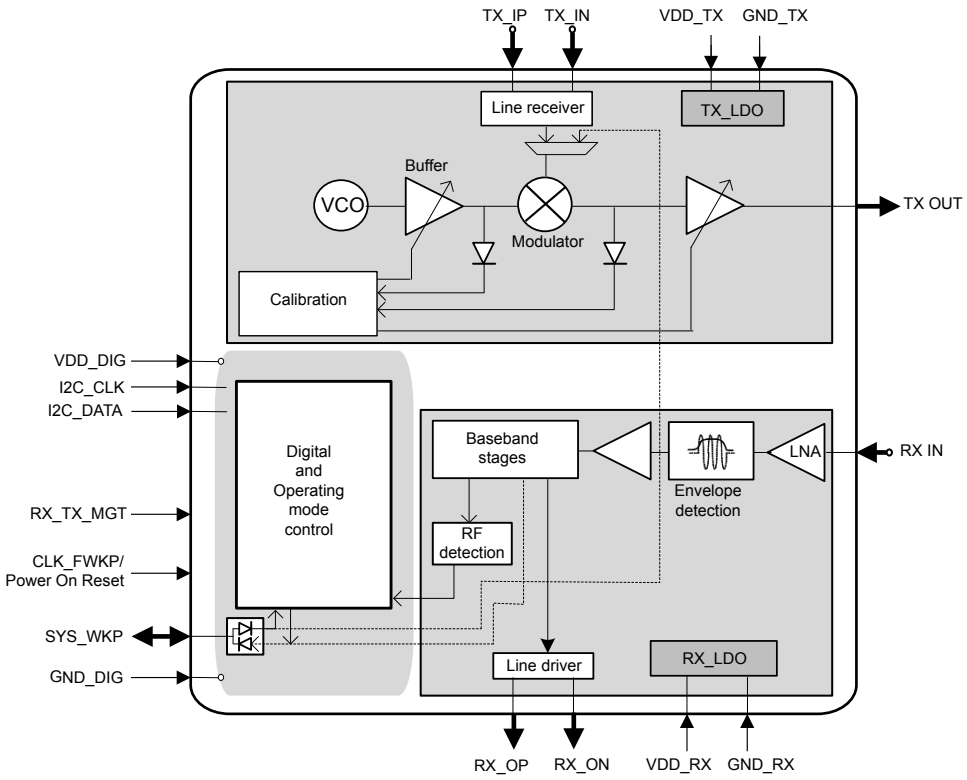
Applications

- Board-to-board contactless connections
  - To remove Flex cables in consumer electronics devices
  - To remove cables in industrial electronic systems that undergo mechanical stresses or movement
- Connector-free solutions
  - For water and dust proof connector-free devices
  - For seamless docking and on-the-go device-to-device data synchronization
  - For harsh industrial environment use-cases, avoiding exposure of internal electronics through connector ports
- Contactless connector solutions for industrial applications

1 Block diagram

Figure 1 shows a high-level view of the ST60A2G0.

Figure 1. ST60A2G0 block diagram



2 Overview

The ST60A2G0 is a compact and fully integrated transceiver including full transmit and receive paths, as well as the digital control and power management necessary to operate the IC seamlessly in a low-footprint, single or dual supply application. The I²C bus and hardware control pins enable configuration and management of the IC transitions, which does not require any external RF components or precision frequency reference. Baseband data can be interfaced either on a single-ended CMOS IO or an SLVS differential line driver and receiver.

The transmitter generates the RF ASK modulation by mixing the incoming baseband data with the carrier generated by the on-chip oscillator

The receiver demodulates data using a non-coherent envelope detection technique and an adaptive threshold comparator, followed by a differential SLVS line driver.

2.1 Transmitter subsystem

The carrier generator is based on an on-chip VCO (voltage-controlled oscillator). A differential sine-wave signal with a frequency in the region of 60.5 GHz is generated at the output. The exact VCO frequency is calibrated for each device by ST during the industrial test phase. The VCO calibration is stored within the chip and is read automatically each time the IC is powered on.

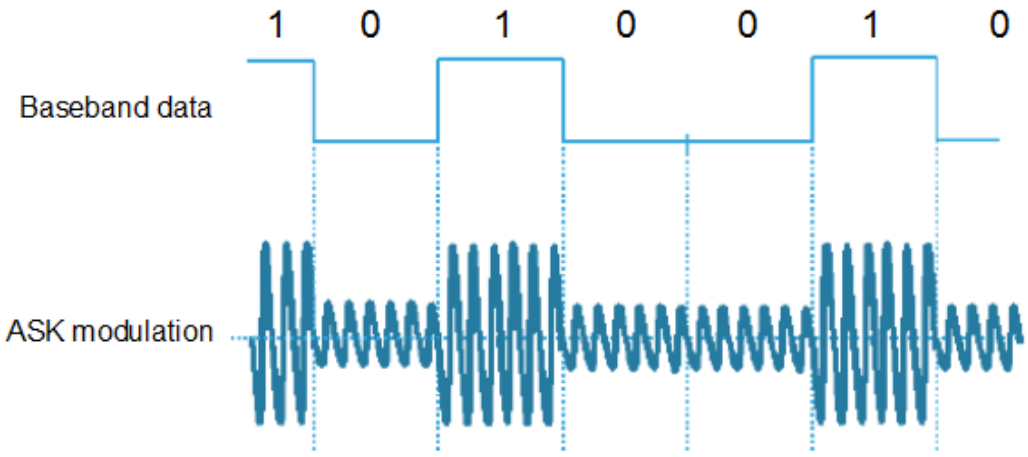
The output signal of the carrier generator is then amplified in order to provide a large sine wave to the modulator in order to maximize power efficiency.

The line receiver supports 2 different input modes:

- Low-amplitude high speed input, the electrical specification of which depends on the operating protocol. The differential pair is referred to as TX_IP, TX_IN
- A CMOS signal can be input on SYS_WKP IO

The modulator directly mixes the buffer output signal with the incoming serial baseband differential data, thereby implementing a power-efficient ASK modulator (see Figure 2). The RF output signal is driven on a single-ended output matched to 50 Ω after recommended PCB transition, to be fed to the antenna. The RF output power is calibrated for each device by ST during the industrial test phase. The RF output calibration is stored within the chip, and is read automatically each time the IC is powered-on.

Figure 2. ASK modulated signal versus time



2.2 Receiver subsystem

The device contains an on-chip LNA, which amplifies the RX ASK signal. It is single-ended at the input and matched to 50 Ω at the reference plane with recommended PCB transition. The LNA output connects to the envelope detector.

The power detector extracts the signal envelope containing ASK modulation, in order to retrieve the data. The analog baseband circuitry reshapes the data, which is then provided to the line driver, and to the high speed digital logic.

The demodulated data is output to either:

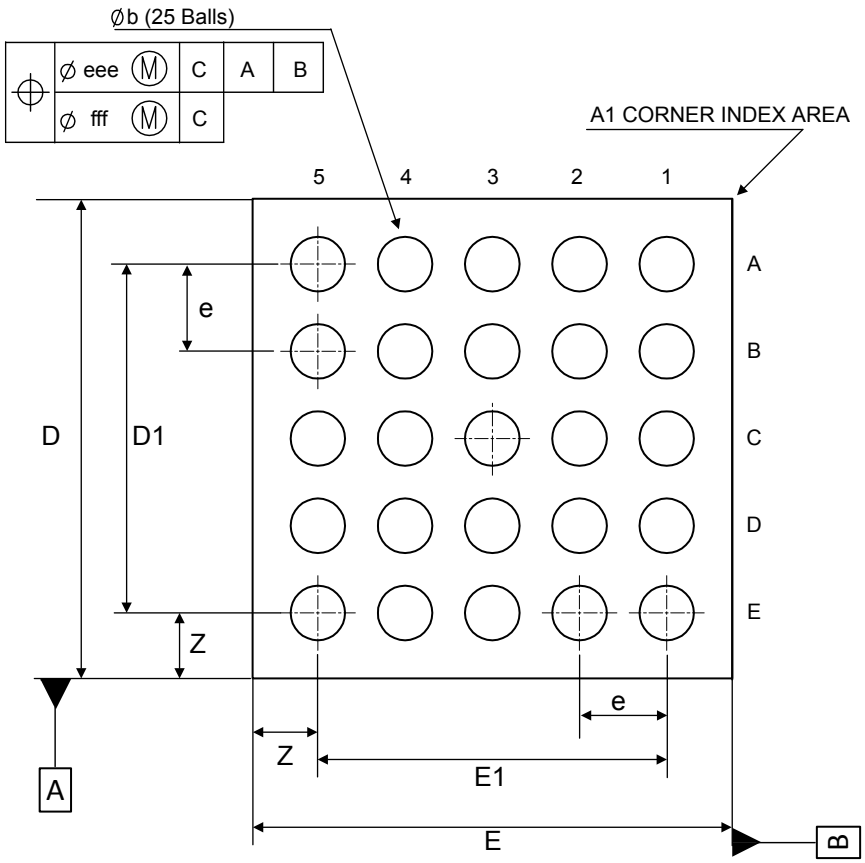
- a differential line driver feeding the RX_OP, RX_ON pair, the electrical specification of which depends on the operating protocol
- a CMOS signal on SYS_WKP IO.

3 Package information

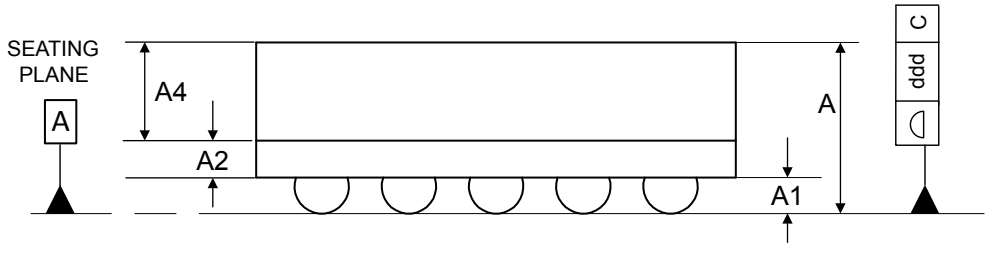
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 VFBGA25 package information

Figure 3. VFBGA - 25 balls, 2.20 x 2.20 mm, 0.40 mm pitch, fine pitch square ball grid array package outline



BOTTOM VIEW



SIDE VIEW

1. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug. A distinguishing feature is allowed on the surface of the package to identify the terminal A1 corner. The exact shape and size of this feature are optional.

Table 1. VFBGA - 25 balls, 2.20 x 2.20 mm, 0.40 mm pitch, fine pitch square ball grid array mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	0.665	0.785	0.900	0.0262	0.0309	0.0354
A1	0.120	-	-	0.0047	-	-
A2	-	0.170	-	-	0.0067	-
A4	0.400	-	-	0.0157	-	-
b	0.200	-	-	0.0079	-	-
D	2.100	2.200	2.300	0.0827	0.0866	0.0906
D1	-	1.600	-	-	0.0630	-
E	2.100	2.200	2.300	0.0827	0.0866	0.0906
E1	-	1.600	-	-	0.0630	-
e	-	0.400	-	-	0.0157	-
Z	-	0.300	-	-	0.0118	-
ddd	-	0.080	-	-	0.0031	-
eee(3)	-	0.150	-	-	0.0059	-
fff(4)	-	0.050	-	-	0.0020	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *VFBGA stands for very thin profile fine pitch ball grid array package. Very thin profile: 0.80 < A Max ≤ 1.00 mm / Fine pitch: e < 1.00 mm. The total profile height (Dim.A) is measured from the seating plane “C” to the top of the component.*
3. *The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
4. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.*

Figure 4. **VFBGA - 25 balls, 2.20 x 2.20 mm, 0.40 mm pitch, fine pitch square ball grid array recommended footprint**

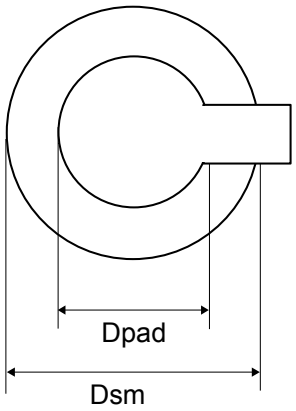


Table 2. **VFBGA25 recommended PCB design rules**

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.250 mm
Dsm	0.325 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Revision history

Table 3. Document revision history

Date	Version	Changes
20-Mar-2019	1	Initial version.
22-Aug-2019	2	Updated Section Features. Updated Section 3.1 VFBGA25 package information.
18-Aug-2020	3	Updated features: • removed IDLE state • HDR maximum data rate updated to 6.25 Gbit/s • LDR minimum data rate updated to 9.6 Kbit/s • package thickness updated. Updated Table 1. VFBGA - 25 balls, 2.20 x 2.20 mm, 0.40 mm pitch, fine pitch square ball grid array mechanical data.
04-Jan-2021	4	Updated features: • added latency • added operating temperatures.
06-Apr-2021	5	Updated power consumption in cover-page features list.