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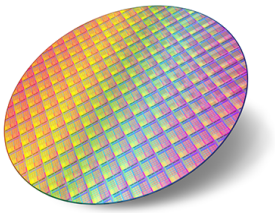
ST32F512M

Data brief

M2M MCU with 32-bit Arm® Cortex®-M3 CPU and 512 Kbyte high-density Flash memory

DFN8 (5 × 6 cm)



Wafer

Product status link
ST32F512M

Features

Hardware features

- Arm® Cortex®-M3 32-bit RISC core
- 12 Kbytes of user RAM
- 512 Kbytes of user Flash memory with a one-time programmable (OTP) area
  - 10-year data retention at 105 °C, or 15 years at 85 °C
  - 500 000 Erase/Write cycles per page
  - 50 million Erase/Write cycles per 64 Kbyte sector
  - Page granularity of 128 bytes
  - Block granularity: 1 Kbyte
  - 128 bytes of user OTP area
  - Page Erase time 4 ms
  - Block Erase (1 Kbyte) in 20 ms
  - Programming performance up to 10 µs/byte
  - Flash memory Erase/Write protection software programmable on 64-Kbyte sectors
- Asynchronous receiver transmitter supporting ISO 7816-3 T=0 and T=1 protocols
- Two 16-bit timers with interrupt capability
- 1.8 V, 3 V and 5 V supply voltage ranges
- External clock frequency from 1 MHz up to 7.5 MHz
- High performance provided by:
  - CPU clock frequency up to 15 MHz
  - External clock multiplier (2x, 3x, and 4x)
- Current consumption compatible with the GSM (global system for mobile communications) and ETSI (European telecommunications standards institute) specifications
- Power-saving Standby state
- Contact assignment compatible with ISO 7816-2
- Electrostatic disturbance (ESD) protection greater than 4 kV (human body model)
- 8-pin DFN (5 × 6 mm) ECOPACK package

Security features

- Monitoring of environmental parameters
- Protection against faults
- ISO 3309 cyclic redundancy check (CRC) calculation block
- True random number generator
- Unique serial number on each die
- Hardware data encryption standard (DES) accelerator

Software features

- Flash memory loader
- Flash memory drivers

Development environment

- Software development and firmware generation are supported by a comprehensive set of development tools dedicated to software design and validation:
  - C compiler
  - Simulator
  - Emulator

Description

The ST32F512M is designed for machine-to-machine (M2M) applications. Its Cortex®-M3 32-bit RISC core operating at a 15-MHz frequency provides great performance and excellent code compactness.

1 Functional description

1.1 Hardware description

The ST32F512M is a serial access microcontroller designed for machine-to-machine (M2M) applications that incorporates the most recent generation of Arm® processors for embedded systems. Its Cortex-M3 32-bit RISC core operating at a 15-MHz frequency brings great performance and excellent code compactness to the application thanks to the Thumb®-2 instruction set.

The high-speed, embedded, 512 Kbyte Flash memory gives more flexibility to the system.

The ST32F512M also offers a serial communication interface fully compatible with the ISO 7816-3 standard (T=0, T=1) for smartcard applications.

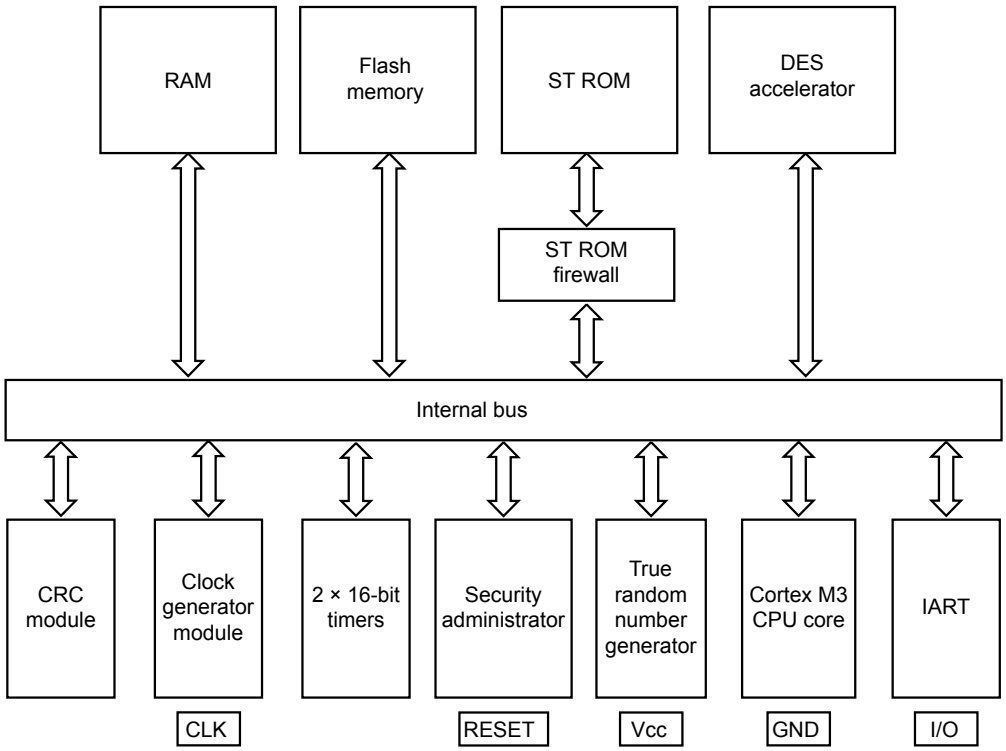
Two general-purpose 16-bit timers are available.

A hardware data encryption standard (DES) accelerator can be used to optimize application performance. A software library is provided for advanced encryption standard (AES) implementation.

The ST32F512M operates in the –40 to +105 °C temperature range, and the 1.8 V, 3 V and 5 V supply voltage ranges. A comprehensive range of power-saving modes enables the design of efficient low-power applications.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Figure 1. ST32F512M block diagram



1.2 Package features

Package qualification for M2M applications:

- Moisture sensitivity level test according to IPC/JEDEC J-STD-20: MSL1 with 260 °C peak temperature.
- Temperature Humidity Bias test according to JEDEC JESD22-A101: 85 °C, 85% RH, 1000 hours.
- Autoclave test according to JEDEC JESD22-A102: 121 °C, 100% relative humidity, 205 kPa, 96 hours.
- Vibration test according to JEDEC JESD22-B103 service condition 1: 20/2000 Hz, 20 g peak acceleration.
- Mechanical Shock test according to JEDEC JESD22-B104 service condition B: 1500 g acceleration for 0.5 ms pulse duration.
- Temperature cycling test according to JEDEC JESD22-A104: –65/+150 °C, 500 cycles.

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

1.3 Software development tool description

Dedicated Cortex-M3 software development tools are provided by Arm® and Keil®. This includes the instruction set simulator (ISS) and C compiler. The documentation is available on the Arm and Keil websites.

Moreover, STMicroelectronics provides:

- A time-accurate hardware emulator controlled by the Keil debugger and the ST development environment.
- A complete product simulator based on the Keil ISS simulator for the Cortex-M3 CPU.
- A ROMed Flash memory loader with very high-speed software downloading capability.

Revision history

Table 1. **Document revision history**

Date	Version	Changes
05-Apr-2019	1	Initial release.

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