# 具有 1.8V 逻辑的 TMUX7219 44V、抗闩锁、2:1 (SPDT) 精密开关

## 1 特性

- 抗闩锁效应
- 双电源电压范围：±4.5V 至 ±22V
- 单电源电压范围：4.5V 至 44V
- 低导通电阻：2Ω
- -40°C 至 +125°C 工作温度
- 逻辑电平：1.8V 至 VDD
- 失效防护逻辑
- 轨到轨运行
- 双向信号路径
- 先断后合开关
- ESD 保护 HBM：2000V

## 2 应用

- 工厂自动化和工业控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 半导体测试
- 交流充电（桩）站
- 超声波扫描仪
- 患者监护和诊断
- 光纤网络
- 光学测试设备
- 远程无线电单元
- 有线网络
- 数据采集系统

## 3 说明

TMUX7219 是一款具有抗闩锁效应的互补金属氧化物半导体 (CMOS) 开关，采用单通道 2:1 (SPDT) 配置。此器件在双电源（±4.5V 至 ±22V）、单电源（4.5V 至 44V）或非对称电源（例如 $V_{DD}$ = 12V，$V_{SS}$ = -5V）供电时均能正常运行。TMUX7219 可在源极 (Sx) 和漏极 (D) 引脚上支持从 $V_{SS}$ 到 {15}VDD 范围的双向模拟和数字信号。

可以通过控制 EN 引脚来启用或禁用 TMUX7219。当禁用时，两个信号路径开关都关闭。当启用时，SEL 引脚可用于打开信号路径 1（S1 至 D）或信号路径 2（S2 至 D）。所有逻辑控制输入均支持 1.8V 到 $V_{DD}$ 的逻辑电平，因此，当器件在有效电源电压范围内运行时，可确保 TTL 和 CMOS 逻辑兼容性。失效防护逻辑电路允许先在控制引脚上施加电压，然后在电源引脚上施加电压，从而保护器件免受潜在的损害。

TMUX72xx 系列具有抗闩锁特性，可防止器件内寄生结构之间通常由过压事件引起的大电流不良事件。闩锁状态通常会一直持续到电源轨关闭为止，并可能导致器件故障。抗闩锁特性使得 TMUX72xx 系列开关和多路复用器能够在恶劣的环境中使用。

**器件信息**

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TMUX7219 | VSSOP (8) (DGK) | 3.00mm × 3.00mm |

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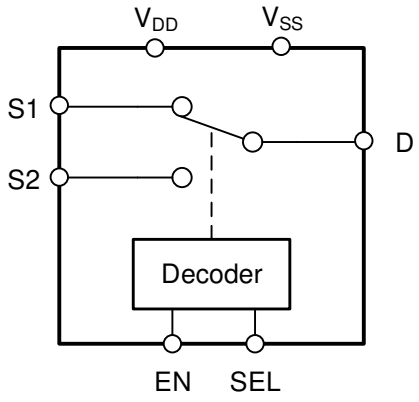


**框图**

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (January 2019) to Revision A (December 2020) | Page |
|---|---|
| • Updated Figure 6-9 *Leakage Current vs Temperature* | 16 |
| • Updated Figure 6-15 *Charge Injection vs Source Voltage – Dual Supplies (Source Side)* | 16 |

# 5 Pin Configuration and Functions

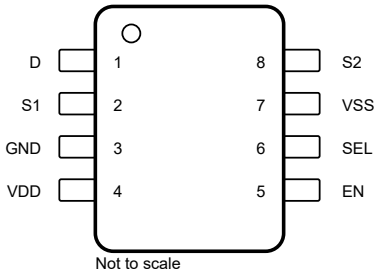


**图 5-1. DGK Package**
**8-Pin VSSOP**
**Top View**

**表 5-1. Pin Functions**

| NAME | NO. | TYPE(1) | DESCRIPTION(2) |
|---|---|---|---|
| D | 1 | I/O | Drain pin. Can be an input or output. |
| S1 | 2 | I/O | Source pin 1. Can be an input or output. |
| GND | 3 | P | Ground (0 V) reference |
| $V_{DD}$ | 4 | P | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{DD}$ and GND. |
| EN | 5 | I | Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on. |
| SEL | 6 | I | Logic control input, has internal pull-down resistor. Controls the switch connection as shown in 节 8.5. |
| $V_{SS}$ | 7 | P | Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{SS}$ and GND. |
| S2 | 8 | I/O | Source pin 2. Can be an input or output. |

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to 节 8.4 for what to do with unused pins.

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ – $V_{SS}$ | Supply voltage | | 48 | V |
| $V_{DD}$ | | – 0.5 | 48 | V |
| $V_{SS}$ | | – 48 | 0.5 | V |
| $V_{SEL}$ or $V_{EN}$ | Logic control input pin voltage (SEL, EN)(4) | – 0.5 | 48 | V |
| $I_{SEL}$ or $I_{EN}$ | Logic control input pin current (SEL, EN)(4) | – 30 | 30 | mA |
| $V_S$ or $V_D$ | Source or drain voltage (Sx, D)(4) | $V_{SS}$ – 0.5 | $V_{DD}$+0.5 | V |
| $I_{IK}$ | Diode clamp current(4) | – 30 | 30 | mA |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, D) | $I_{DC}$ + 10 %(5) | | mA |
| $T_A$ | Ambient temperature | – 55 | 135 | °C |
| $T_{stg}$ | Storage temperature | – 65 | 150 | °C |
| $T_J$ | Junction temperature | | 140 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(5) Refer to *Source or Drain Continuous Current* table for $I_{DC}$ specifications.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Thermal Information

| THERMAL METRIC(1) | | TMUX7219 DGK (VSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 152.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 73.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 4.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 71.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ - $V_{SS}$ (1) | Power supply voltage differential | 4.5 | | 44 | V |
| $V_{DD}$ | Positive power supply voltage | 4.5 | | 44 | V |
| $V_S$ or $V_D$ | Signal path input/output voltage (source or drain pin) (Sx, D) | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{SEL}$ or $V_{EN}$ | Address or enable pin voltage | 0 | | 44 | V |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, D) | | $I_{DC}$ (2) | | mA |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |

(1) $V_{DD}$ and $V_{SS}$ can be any value as long as 4.5 V ≤ ($V_{DD}$ – $V_{SS}$) ≤ 44 V, and the minimum $V_{DD}$ is met.
(2) Refer to *Source or Drain Continuous Current* table for $I_{DC}$ specifications.

## 6.5 Source or Drain Continuous Current

at supply voltage of $V_{DD}$ ± 10%, $V_{SS}$ ± 10 % (unless otherwise noted)

| CONTINUOUS CURRENT PER CHANNEL ($I_{DC}$) | | $T_A$ = 25°C | $T_A$ = 85°C | $T_A$ = 125°C | UNIT |
|---|---|---|---|---|---|
| PACKAGE | TEST CONDITIONS | | | | |
| DGK (VSSOP) | +44 V Single Supply(1) | 330 | 210 | 120 | mA |
| | ±15 V Dual Supply | 330 | 210 | 120 | mA |
| | +12 V Single Supply | 240 | 160 | 100 | mA |
| | ±5 V Dual Supply | 240 | 160 | 100 | mA |
| | +5 V Single Supply | 180 | 120 | 80 | mA |

(1) Specified for nominal supply voltage only.

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## 6.6 ±15 V Dual Supply: Electrical Characteristics

$V_{DD}$ = +15 V ± 10%, $V_{SS}$ = – 15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +15 V, $V_{SS}$ = – 15 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = – 10 V to +10 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 2.1 | 2.9 | Ω |
| | | | – 40°C to +85°C | | | 3.8 | Ω |
| | | | – 40°C to +125°C | | | 4.5 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = – 10 V to +10 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 0.05 | 0.25 | Ω |
| | | | – 40°C to +85°C | | | 0.3 | Ω |
| | | | – 40°C to +125°C | | | 0.35 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = – 10 V to +10 V<br>$I_S$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 0.5 | 0.6 | Ω |
| | | | – 40°C to +85°C | | | 0.7 | Ω |
| | | | – 40°C to +125°C | | | 0.85 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0 V, $I_S$ = – 10 mA<br>Refer to On-Resistance | – 40°C to +125°C | | 0.009 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Switch state is off<br>$V_S$ = +10 V / – 10 V<br>$V_D$ = – 10 V / + 10 V<br>Refer to Off-Leakage Current | 25°C | – 1 | 0.1 | 1 | nA |
| | | | – 40°C to +85°C | – 3 | | 3 | nA |
| | | | – 40°C to +125°C | – 15 | | 15 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Switch state is off<br>$V_S$ = +10 V / – 10 V<br>$V_D$ = – 10 V / + 10 V<br>Refer to Off-Leakage Current | 25°C | – 1.8 | 0.08 | 1.8 | nA |
| | | | – 40°C to +85°C | – 5 | | 5 | nA |
| | | | – 40°C to +125°C | – 26 | | 26 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Switch state is on<br>$V_S$ = $V_D$ = ±10 V<br>Refer to On-Leakage Current | 25°C | – 1.5 | 0.05 | 1.5 | nA |
| | | | – 40°C to +85°C | – 3.5 | | 3.5 | nA |
| | | | – 40°C to +125°C | – 18 | | 18 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | – 40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Logic voltage low | | – 40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | – 40°C to +125°C | | 0.005 | 1.2 | µA |
| $I_{IL}$ | Input leakage current | | – 40°C to +125°C | – 0.95 | – 0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | – 40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 25 | 40 | µA |
| | | | – 40°C to +85°C | | | 50 | µA |
| | | | – 40°C to +125°C | | | 80 | µA |
| $I_{SS}$ | $V_{SS}$ supply current | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 3 | 10 | µA |
| | | | – 40°C to +85°C | | | 20 | µA |
| | | | – 40°C to +125°C | | | 40 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

## 6.7 ±15 V Dual Supply: Switching Characteristics

$V_{DD}$ = +15 V ± 10%, $V_{SS}$ = – 15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +15 V, $V_{SS}$ = – 15 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 120 | 175 | ns |
| | | | – 40°C to +85°C | | | 190 | ns |
| | | | – 40°C to +125°C | | | 210 | ns |
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 80 | 170 | ns |
| | | | – 40°C to +85°C | | | 185 | ns |
| | | | – 40°C to +125°C | | | 200 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 110 | 180 | ns |
| | | | – 40°C to +85°C | | | 195 | ns |
| | | | – 40°C to +125°C | | | 210 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 10 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 50 | | ns |
| | | | – 40°C to +85°C | 1 | | | ns |
| | | | – 40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35 pF | 25°C | | 0.15 | | ms |
| | | | – 40°C to +85°C | | | 1 | ms |
| | | | – 40°C to +125°C | | | 1 | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 140 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 0 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | – 11 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 100 kHz<br>Refer to Off Isolation | 25°C | | – 75 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | – 55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | – 92 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | – 75 | | dB |
| BW | – 3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V<br>Refer to Bandwidth | 25°C | | 40 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1 MHz | 25°C | | – 0.2 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 10 MΩ, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to AC PSRR | 25°C | | – 40 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 15 V, $V_{BIAS}$ = 0 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0005 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 36 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 49 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 150 | | pF |

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## 6.8 ±20 V Dual Supply: Electrical Characteristics

$V_{DD}$ = +20 V ± 10%, $V_{SS}$ = – 20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +20 V, $V_{SS}$ = – 20 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = – 15 V to +15 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 1.9 | 2.7 | Ω |
| | | | – 40°C to +85°C | | | 3.7 | Ω |
| | | | – 40°C to +125°C | | | 4.4 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = – 15 V to +15 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 0.04 | 0.22 | Ω |
| | | | – 40°C to +85°C | | | 0.28 | Ω |
| | | | – 40°C to +125°C | | | 0.28 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = – 15 V to +15 V<br>$I_S$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 0.3 | 0.75 | Ω |
| | | | – 40°C to +85°C | | | 0.9 | Ω |
| | | | – 40°C to +125°C | | | 1.2 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0 V, $I_S$ = – 10 mA<br>Refer to On-Resistance | – 40°C to +125°C | | 0.008 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 22 V, $V_{SS}$ = – 22 V<br>Switch state is off<br>$V_S$ = +15 V / – 15 V<br>$V_D$ = – 15 V / + 15 V<br>Refer to Off-Leakage Current | 25°C | – 2 | 0.05 | 2 | nA |
| | | | – 40°C to +85°C | – 4 | | 4 | nA |
| | | | – 40°C to +125°C | – 24 | | 24 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 22 V, $V_{SS}$ = – 22 V<br>Switch state is off<br>$V_S$ = +15 V / – 15 V<br>$V_D$ = – 15 V / + 15 V<br>Refer to Off-Leakage Current | 25°C | – 2.5 | 0.1 | 2.5 | nA |
| | | | – 40°C to +85°C | – 8 | | 8 | nA |
| | | | – 40°C to +125°C | – 44 | | 44 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 22 V, $V_{SS}$ = – 22 V<br>Switch state is on<br>$V_S$ = $V_D$ = ±15 V<br>Refer to On-Leakage Current | 25°C | – 2 | 0.1 | 2 | nA |
| | | | – 40°C to +85°C | – 5 | | 5 | nA |
| | | | – 40°C to +125°C | – 29 | | 29 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | – 40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Logic voltage low | | – 40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | – 40°C to +125°C | | 0.4 | 1.2 | µA |
| $I_{IL}$ | Input leakage current | | – 40°C to +125°C | – 0.98 | – 0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | – 40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 22 V, $V_{SS}$ = – 22 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 26 | 39 | µA |
| | | | – 40°C to +85°C | | | 43 | µA |
| | | | – 40°C to +125°C | | | 48 | µA |
| $I_{SS}$ | $V_{SS}$ supply current | $V_{DD}$ = 22 V, $V_{SS}$ = – 22 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 4 | 6 | µA |
| | | | – 40°C to +85°C | | | 7 | µA |
| | | | – 40°C to +125°C | | | 8 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

## 6.9 ±20 V Dual Supply: Switching Characteristics

$V_{DD}$ = +20 V ± 10%, $V_{SS}$ = – 20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +20 V, $V_{SS}$ = – 20 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 100 | 190 | ns |
| | | | – 40°C to +85°C | | | 200 | ns |
| | | | – 40°C to +125°C | | | 220 | ns |
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 80 | 180 | ns |
| | | | – 40°C to +85°C | | | 200 | ns |
| | | | – 40°C to +125°C | | | 220 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 90 | 180 | ns |
| | | | – 40°C to +85°C | | | 200 | ns |
| | | | – 40°C to +125°C | | | 220 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 10 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 60 | | ns |
| | | | – 40°C to +85°C | 1 | | | ns |
| | | | – 40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35 pF | 25°C | | 0.17 | | ms |
| | | | – 40°C to +85°C | | | 1 | ms |
| | | | – 40°C to +125°C | | | 1 | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 122 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 0 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | – 14.8 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 100 kHz<br>Refer to Off Isolation | 25°C | | – 75 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | – 55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | – 92 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | – 74 | | dB |
| BW | – 3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V,<br>Refer to Bandwidth | 25°C | | 38 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1 MHz | 25°C | | – 0.16 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 10 MΩ, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to AC PSRR | 25°C | | – 38 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 20 V, $V_{BIAS}$ = 0 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0005 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 33 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 44 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 148 | | pF |

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## 6.10 44 V Single Supply: Electrical Characteristics

$V_{DD}$ = +44 V, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +44 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to 40 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 2.3 | 2.8 | Ω |
| | | | –40°C to +85°C | | | 3.6 | Ω |
| | | | –40°C to +125°C | | | 4.3 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0 V to 40 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 0.1 | 0.2 | Ω |
| | | | –40°C to +85°C | | | 0.3 | Ω |
| | | | –40°C to +125°C | | | 0.35 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to 40 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 0.2 | 1 | Ω |
| | | | –40°C to +85°C | | | 1.3 | Ω |
| | | | –40°C to +125°C | | | 1.5 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 22 V, $I_S$ = –10 mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.02 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 44 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 40 V / 1 V<br>$V_D$ = 1 V / 40 V<br>Refer to Off-Leakage Current | 25°C | –5 | 0.05 | 5 | nA |
| | | | –40°C to +85°C | –10 | | 10 | nA |
| | | | –40°C to +125°C | –35 | | 35 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 44 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 40 V / 1 V<br>$V_D$ = 1 V / 40 V<br>Refer to Off-Leakage Current | 25°C | –8 | 0.05 | 8 | nA |
| | | | –40°C to +85°C | –12 | | 12 | nA |
| | | | –40°C to +125°C | –70 | | 70 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 44 V, $V_{SS}$ = 0 V<br>Switch state is on<br>$V_S$ = $V_D$ = 40 V or 1 V<br>Refer to On-Leakage Current | 25°C | –8 | 0.05 | 8 | nA |
| | | | –40°C to +85°C | –10 | | 10 | nA |
| | | | –40°C to +125°C | –45 | | 45 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 0.005 | 1.2 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –0.95 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 44 V, $V_{SS}$ = 0 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 17 | 50 | µA |
| | | | –40°C to +85°C | | | 60 | µA |
| | | | –40°C to +125°C | | | 75 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

## 6.11 44 V Single Supply: Switching Characteristics

$V_{DD}$ = +44 V, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +44 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 100 | 185 | ns |
| | | | –40°C to +85°C | | | 200 | ns |
| | | | –40°C to +125°C | | | 220 | ns |

## 6.11 44 V Single Supply: Switching Characteristics (continued)

$V_{DD}$ = +44 V, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +44 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 80 | 180 | ns |
| | | | –40°C to +85°C | | | 200 | ns |
| | | | –40°C to +125°C | | | 220 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 90 | 180 | ns |
| | | | –40°C to +85°C | | | 200 | ns |
| | | | –40°C to +125°C | | | 220 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 18 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 45 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35 pF | 25°C | | 0.14 | | ms |
| | | | –40°C to +85°C | | | 1 | ms |
| | | | –40°C to +125°C | | | 1 | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 185 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 22 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | –16.5 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Off Isolation | 25°C | | –75 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | –55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | –92 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | –75 | | dB |
| BW | –3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V<br>Refer to Bandwidth | 25°C | | 37 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz | 25°C | | –0.18 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 10 MΩ, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to AC PSRR | 25°C | | –39 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 22 V, $V_{BIAS}$ = 22 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0003 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 22 V, f = 1 MHz | 25°C | | 33 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 22 V, f = 1 MHz | 25°C | | 45 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 22 V, f = 1 MHz | 25°C | | 148 | | pF |

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## 6.12 36 V Single Supply: Electrical Characteristics

$V_{DD}$ = +36 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +36 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $V_A$ | Analog signal range | | –40°C to +125°C | $V_{SS}$ | | $V_{DD}$ | V |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to 30 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 2.5 | 3.5 | Ω |
| | | | –40°C to +85°C | | | 4.5 | Ω |
| | | | –40°C to +125°C | | | 5 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0 V to 30 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 0.1 | 0.2 | Ω |
| | | | –40°C to +85°C | | | 0.25 | Ω |
| | | | –40°C to +125°C | | | 0.3 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to 30 V<br>$I_S$ = –10 mA<br>Refer to On-Resistance | 25°C | | 0.3 | 1 | Ω |
| | | | –40°C to +85°C | | | 1.5 | Ω |
| | | | –40°C to +125°C | | | 2 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 18 V, $I_S$ = –10 mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.02 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 39.6 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 30 V / 1 V<br>$V_D$ = 1 V / 30 V<br>Refer to Off-Leakage Current | 25°C | –0.25 | 0.05 | 0.25 | nA |
| | | | –40°C to +85°C | –3 | | 3 | nA |
| | | | –40°C to +125°C | –26 | | 26 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 39.6 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 30 V / 1 V<br>$V_D$ = 1 V / 30 V<br>Refer to Off-Leakage Current | 25°C | –1 | 0.05 | 1 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –50 | | 50 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 39.6 V, $V_{SS}$ = 0 V<br>Switch state is on<br>$V_S$ = $V_D$ = 30 V or 1 V<br>Refer to On-Leakage Current | 25°C | –0.4 | 0.05 | 0.4 | nA |
| | | | –40°C to +85°C | –4.5 | | 4.5 | nA |
| | | | –40°C to +125°C | –32 | | 32 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 0.4 | 1.2 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –0.98 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 39.6 V, $V_{SS}$ = 0 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 28 | 50 | µA |
| | | | –40°C to +85°C | | | 60 | µA |
| | | | –40°C to +125°C | | | 70 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

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## 6.13 36 V Single Supply: Switching Characteristics

$V_{DD}$ = +36 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +36 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 100 | 170 | ns |
| | | | – 40°C to +85°C | | | 185 | ns |
| | | | – 40°C to +125°C | | | 200 | ns |
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 80 | 180 | ns |
| | | | – 40°C to +85°C | | | 190 | ns |
| | | | – 40°C to +125°C | | | 200 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 90 | 180 | ns |
| | | | – 40°C to +85°C | | | 195 | ns |
| | | | – 40°C to +125°C | | | 200 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 18 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 60 | | ns |
| | | | – 40°C to +85°C | 1 | | | ns |
| | | | – 40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35 pF | 25°C | | 0.14 | | ms |
| | | | – 40°C to +85°C | | | 1 | ms |
| | | | – 40°C to +125°C | | | 1 | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 200 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 18 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | – 13 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Off Isolation | 25°C | | – 75 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | – 55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | – 95 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | – 70 | | dB |
| BW | – 3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V,<br>Refer to Bandwidth | 25°C | | 38 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz | 25°C | | – 0.19 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 10 MΩ, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to AC PSRR | 25°C | | – 38 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ =18 V, $V_{BIAS}$ = 18 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0004 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 18 V, f = 1 MHz | 25°C | | 34 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 18 V, f = 1 MHz | 25°C | | 47 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 18 V, f = 1 MHz | 25°C | | 148 | | pF |

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## 6.14 12 V Single Supply: Electrical Characteristics

$V_{DD}$ = +12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to 10 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 4.6 | 6 | Ω |
| | | | –40°C to +85°C | | | 7.5 | Ω |
| | | | –40°C to +125°C | | | 8.6 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0 V to 10 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 0.08 | 0.25 | Ω |
| | | | –40°C to +85°C | | | 0.35 | Ω |
| | | | –40°C to +125°C | | | 0.4 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to 10 V<br>$I_S$ = –10 mA<br>Refer to On-Resistance | 25°C | | 1.2 | 1.9 | Ω |
| | | | –40°C to +85°C | | | 2.2 | Ω |
| | | | –40°C to +125°C | | | 2.5 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 6 V, $I_S$ = –10 mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.02 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 10 V / 1 V<br>$V_D$ = 1 V / 10 V<br>Refer to Off-Leakage Current | 25°C | –1 | 0.05 | 1 | nA |
| | | | –40°C to +85°C | –2 | | 2 | nA |
| | | | –40°C to +125°C | –12 | | 12 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 10 V / 1 V<br>$V_D$ = 1 V / 10 V<br>Refer to Off-Leakage Current | 25°C | –1.5 | 0.05 | 1.5 | nA |
| | | | –40°C to +85°C | –3 | | 3 | nA |
| | | | –40°C to +125°C | –23 | | 23 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V<br>Switch state is on<br>$V_S$ = $V_D$ = 10 V or 1 V<br>Refer to On-Leakage Current | 25°C | –1 | 0.05 | 1 | nA |
| | | | –40°C to +85°C | –3 | | 3 | nA |
| | | | –40°C to +125°C | –15 | | 15 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 0.005 | 1.2 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –0.96 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 10 | 35 | µA |
| | | | –40°C to +85°C | | | 45 | µA |
| | | | –40°C to +125°C | | | 55 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

## 6.15 12 V Single Supply: Switching Characteristics

$V_{DD}$ = +12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 8 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 180 | 200 | ns |
| | | | –40°C to +85°C | | | 220 | ns |
| | | | –40°C to +125°C | | | 250 | ns |

## 6.15 12 V Single Supply: Switching Characteristics (continued)

$V_{DD}$ = +12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 8 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 120 | 200 | ns |
| | | | –40°C to +85°C | | | 220 | ns |
| | | | –40°C to +125°C | | | 250 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 8 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 130 | 220 | ns |
| | | | –40°C to +85°C | | | 250 | ns |
| | | | –40°C to +125°C | | | 280 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 8 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 60 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35 pF | 25°C | | 0.17 | | ms |
| | | | –40°C to +85°C | | | 1 | ms |
| | | | –40°C to +125°C | | | 1 | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 250 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 6 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | –6 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Charge Injection | 25°C | | –75 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | –55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | –92 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | –85 | | dB |
| BW | –3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V<br>Refer to Bandwidth | 25°C | | 42 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz | 25°C | | –0.3 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 10 MΩ, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to AC PSRR | 25°C | | –42 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 6 V, $V_{BIAS}$ = 6 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0009 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 44 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 62 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 155 | | pF |

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## 6.16 Typical Characteristics

at $T_A$ = 25°C

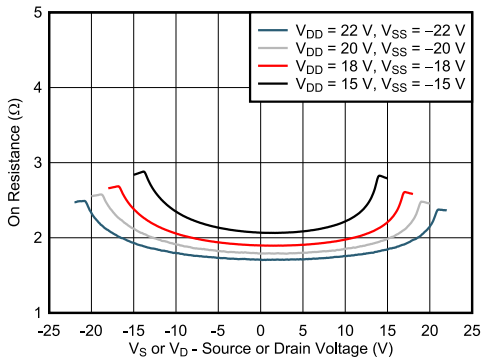



图 6-1. On-Resistance vs Source or Drain Voltage – Dual Supply

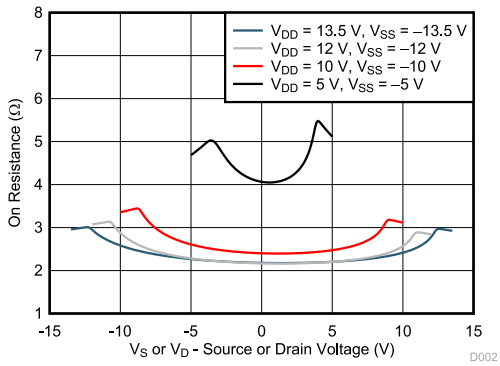



图 6-2. On-Resistance vs Source or Drain Voltage – Dual Supply

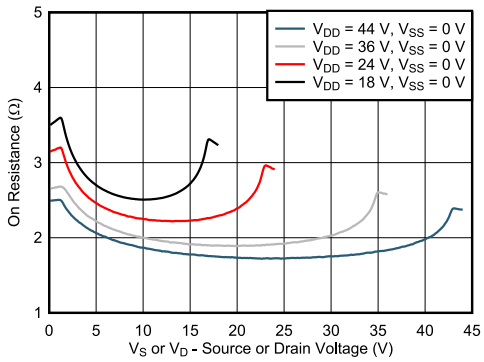



图 6-3. On-Resistance vs Source or Drain Voltage – Single Supply

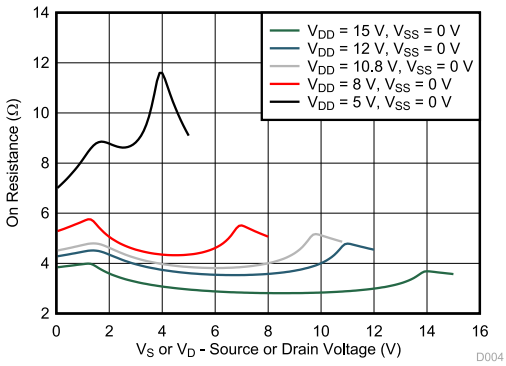
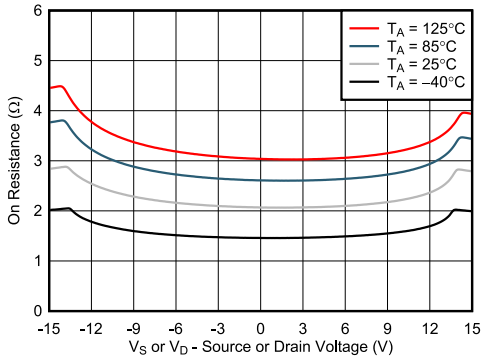
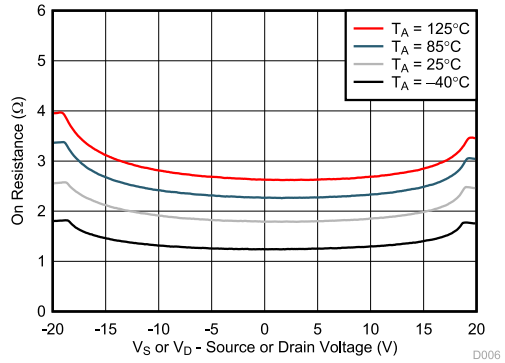



图 6-4. On-Resistance vs Source or Drain Voltage – Single Supply




$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

图 6-5. On-Resistance vs Temperature

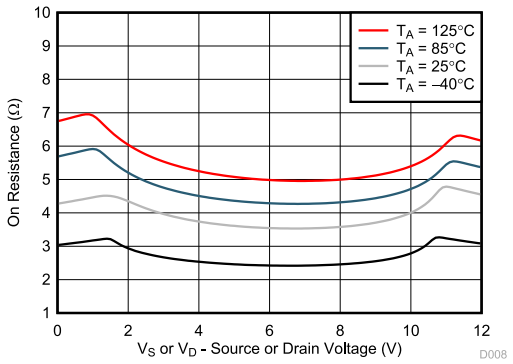



$V_{DD}$ = 20 V, $V_{SS}$ = -20V

图 6-6. On-Resistance vs Temperature

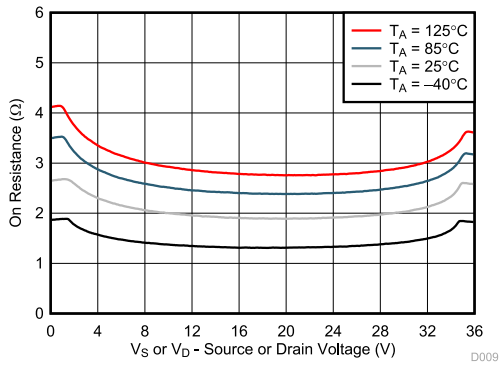
## 6.16 Typical Characteristics (continued)

at $T_A$ = 25°C



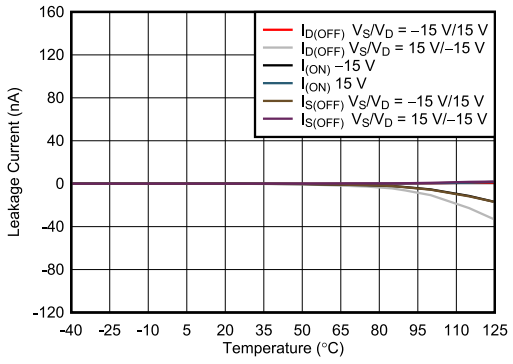

$V_{DD}$ = 12 V, $V_{SS}$ = 0 V

**图 6-7. On-Resistance vs Temperature**



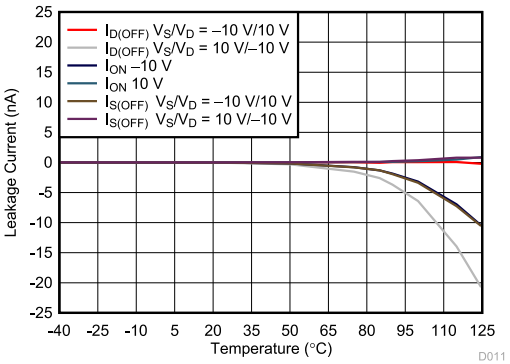

$V_{DD}$ = 36 V, $V_{SS}$ = 0 V

**图 6-8. On-Resistance vs Temperature**



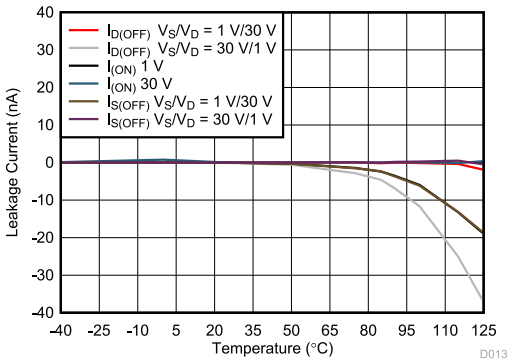

$V_{DD}$ = 20 V, $V_{SS}$ = -20V

**图 6-9. Leakage Current vs Temperature**



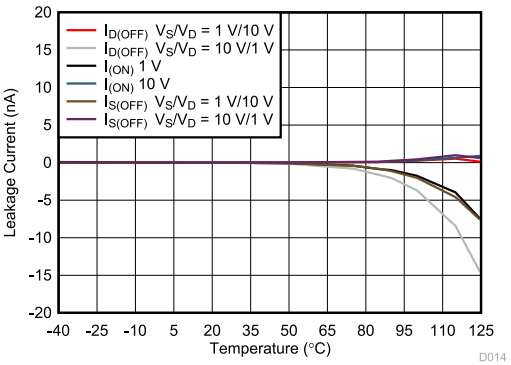

$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

**图 6-10. Leakage Current vs Temperature**




$V_{DD}$ = 36 V, $V_{SS}$ = 0 V

**图 6-11. Leakage Current vs Temperature**




$V_{DD}$ = 12 V, $V_{SS}$ = 0 V

**图 6-12. Leakage Current vs Temperature**

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## 6.16 Typical Characteristics (continued)

at $T_A$ = 25°C

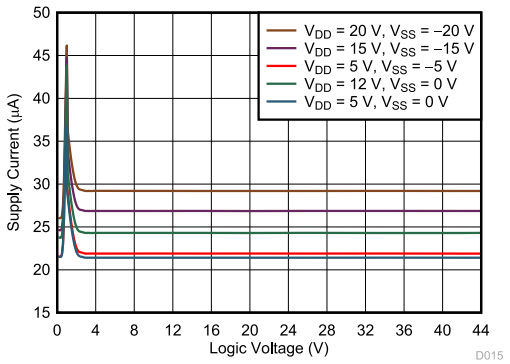



图 6-13. Supply Current vs Logic Voltage

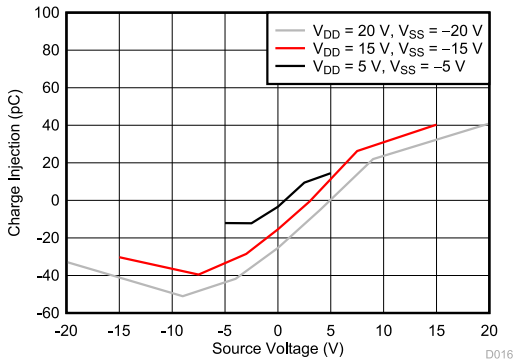



图 6-14. Charge Injection vs Source Voltage – Dual Supplies (Drain side)

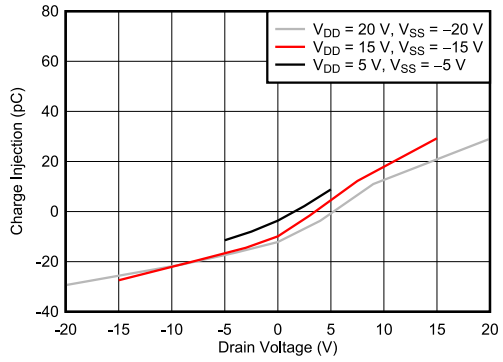



图 6-15. Charge Injection vs Source Voltage – Dual Supplies (Source Side)

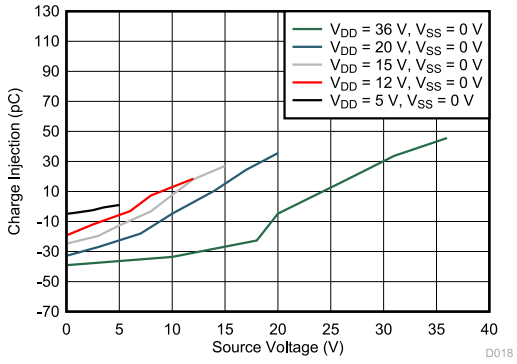



图 6-16. Charge Injection vs Source Voltage – Single Supplies (Drain side)

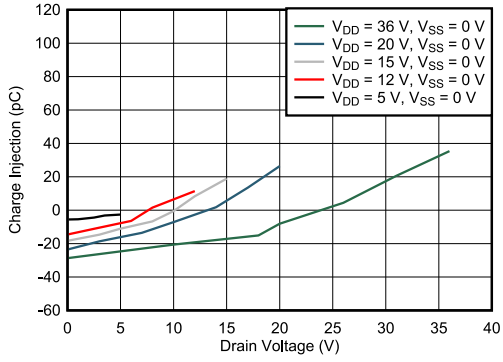
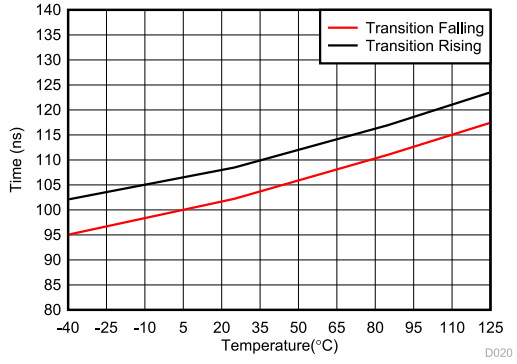



图 6-17. Charge Injection vs Source Voltage – Single Supplies (Source Side)



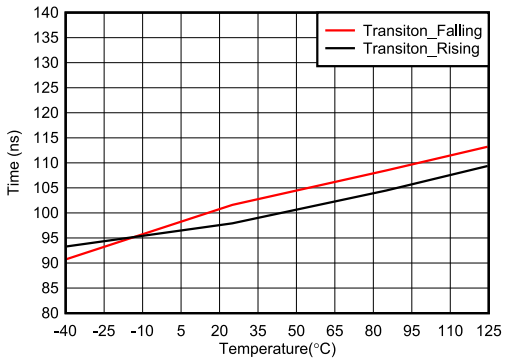

$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

图 6-18. $T_{TRANSITION}$ vs Temperature

ADVANCE INFORMATION

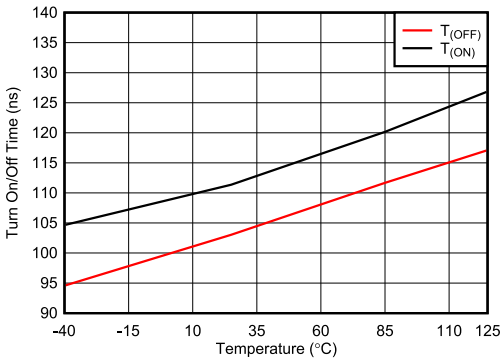
## 6.16 Typical Characteristics (continued)

at $T_A$ = 25°C



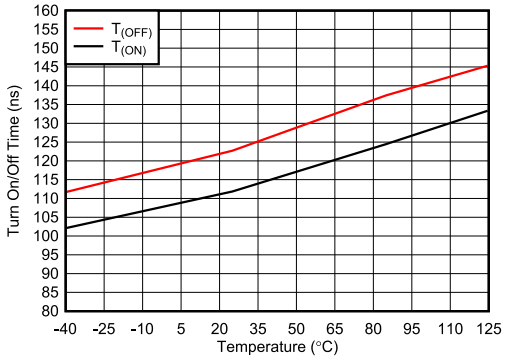

$V_{DD}$ = 44 V, $V_{SS}$ = 0 V

**图 6-19. $T_{TRANSITION}$ vs Temperature**




$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

**图 6-20. $T_{ON}$ and $T_{OFF}$ vs Temperature**




$V_{DD}$ = 44 V, $V_{SS}$ = 0 V

**图 6-21. $T_{ON}$ and $T_{OFF}$ vs Temperature**

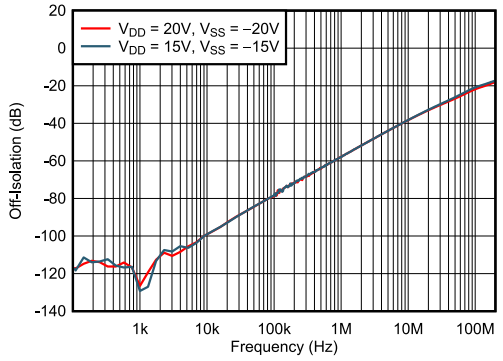



**图 6-22. Off-Isolation vs Frequency**

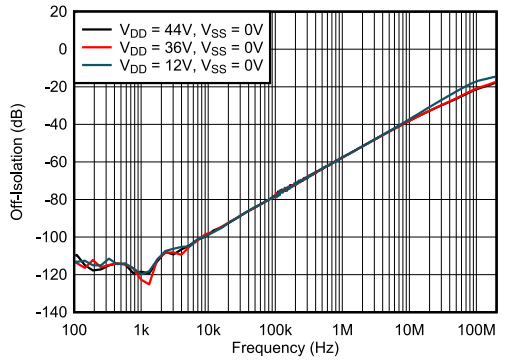



**图 6-23. Off-Isolation vs Frequency**

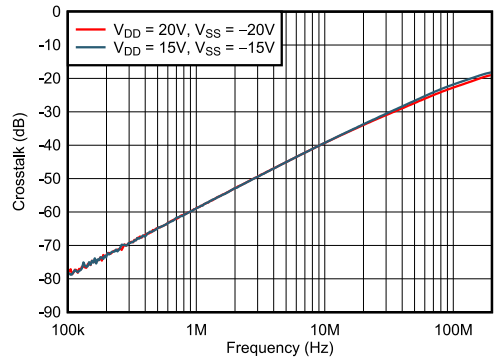



**图 6-24. Crosstalk vs Frequency**

ADVANCE INFORMATION

## 6.16 Typical Characteristics (continued)

at $T_A$ = 25°C

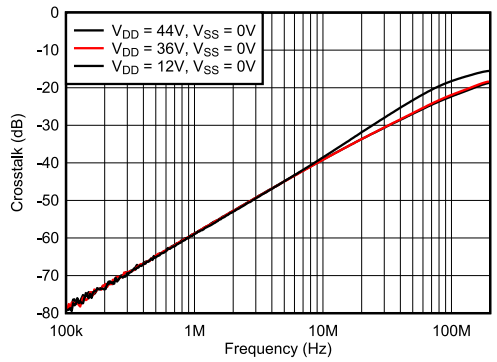



**图 6-25. Crosstalk vs Frequency**

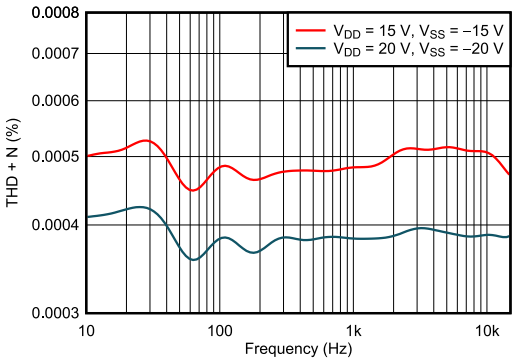



**图 6-26. THD+N vs Frequency (Dual Supplies)**

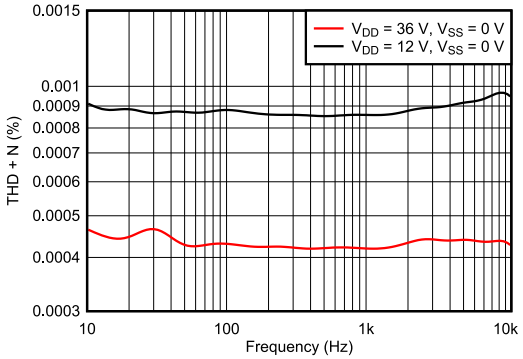



**图 6-27. THD+N vs Frequency (Single Supplies)**

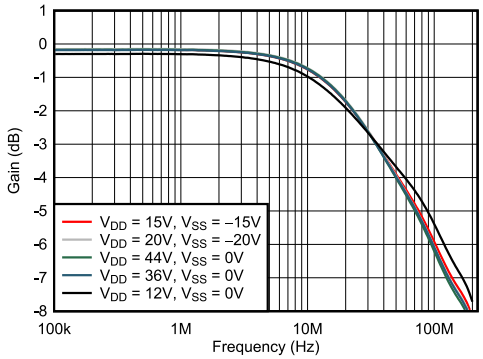
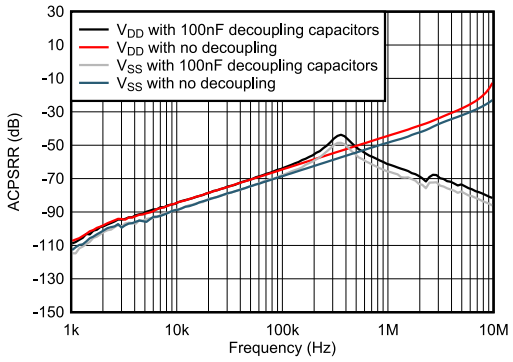
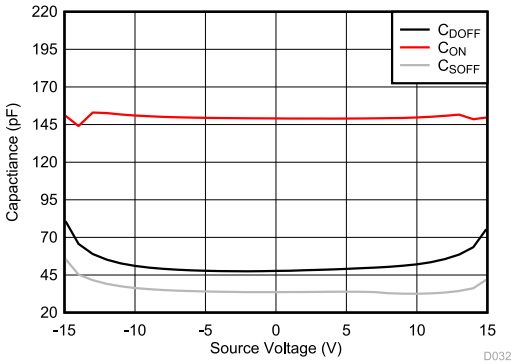



**图 6-28. On Response vs Frequency**




$V_{DD}$ = +15 V, $V_{SS}$ = -15 V

**图 6-29. ACPSRR vs Frequency**




$V_{DD}$ = +15 V, $V_{SS}$ = -15 V

**图 6-30. Capacitance vs Source Voltage or Drain Voltage**

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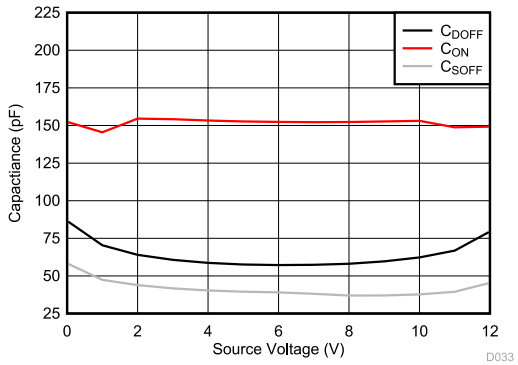
## 6.16 Typical Characteristics (continued)

at $T_A$ = 25°C




$V_{DD}$ = 12 V, $V_{SS}$ = 0 V

**图 6-31. Capacitance vs Source Voltage or Drain Voltage**

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# 7 Parameter Measurement Information

## 7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote on-resistance. 图 7-1 shows the measurement setup used to measure $R_{ON}$. Voltage (V) and current ($I_{SD}$) are measured using the following setup, where $R_{ON}$ is computed as $R_{ON} = V / I_{SD}$:

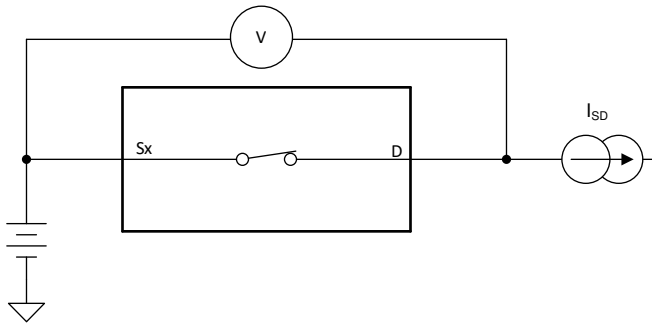


**图 7-1. On-Resistance**

## 7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

图 7-2 shows the setup used to measure both off-leakage currents.

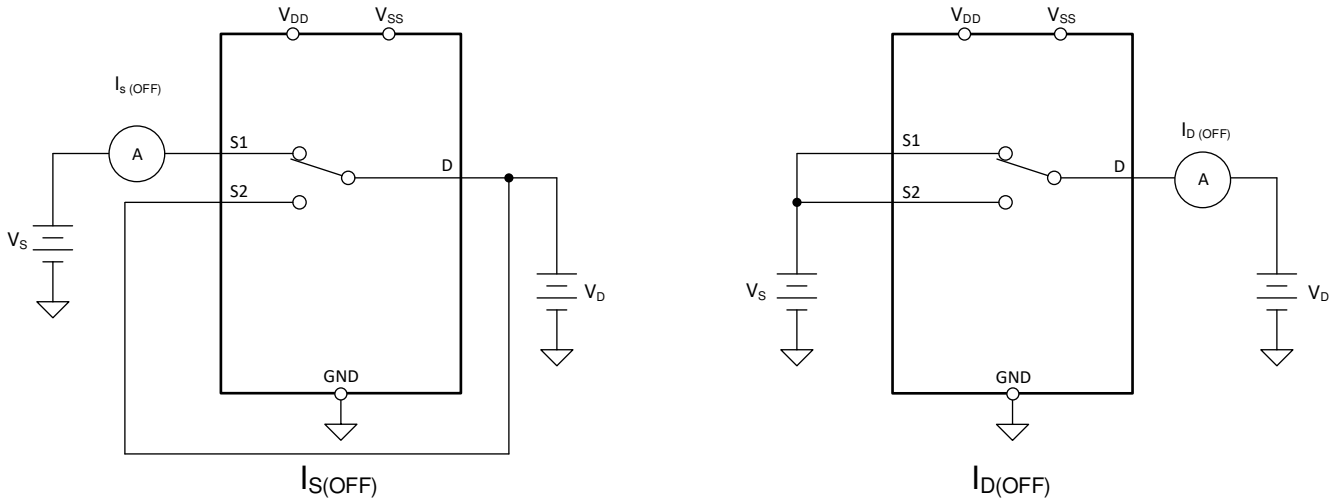


**图 7-2. Off-Leakage Measurement Setup**

## 7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

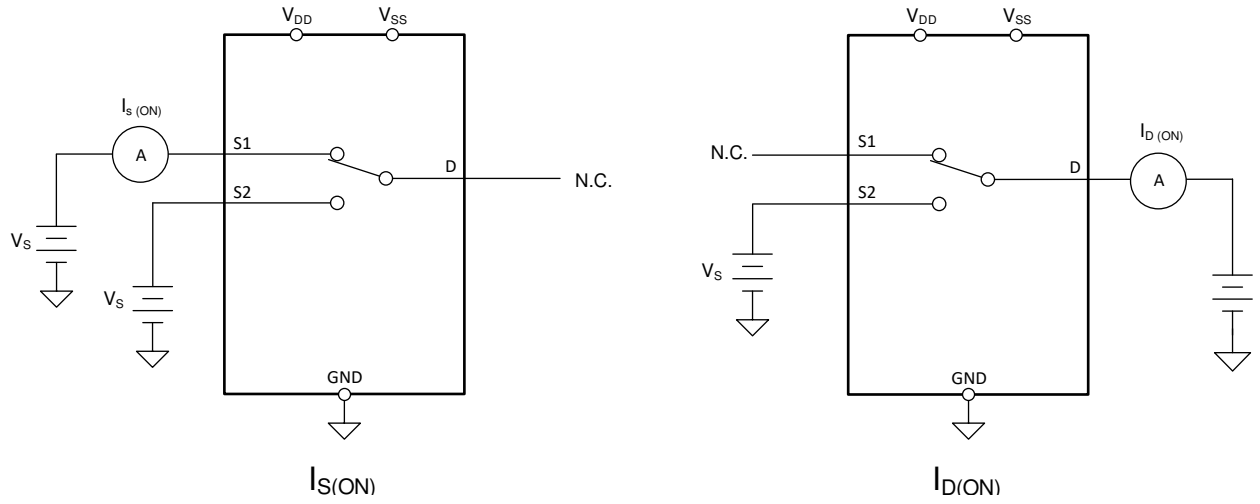


图 7-3. On-Leakage Measurement Setup

## 7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

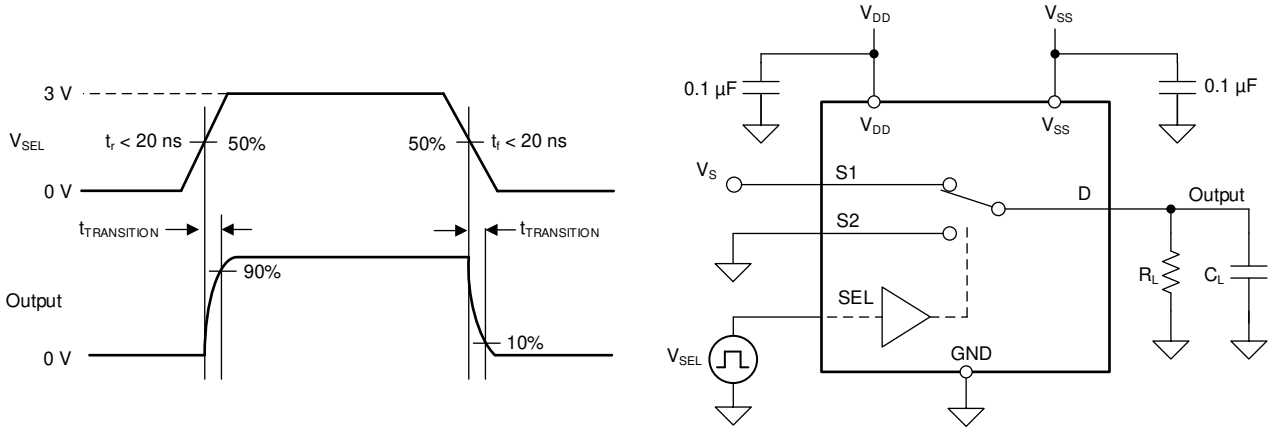


图 7-4. Transition-Time Measurement Setup

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## 7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

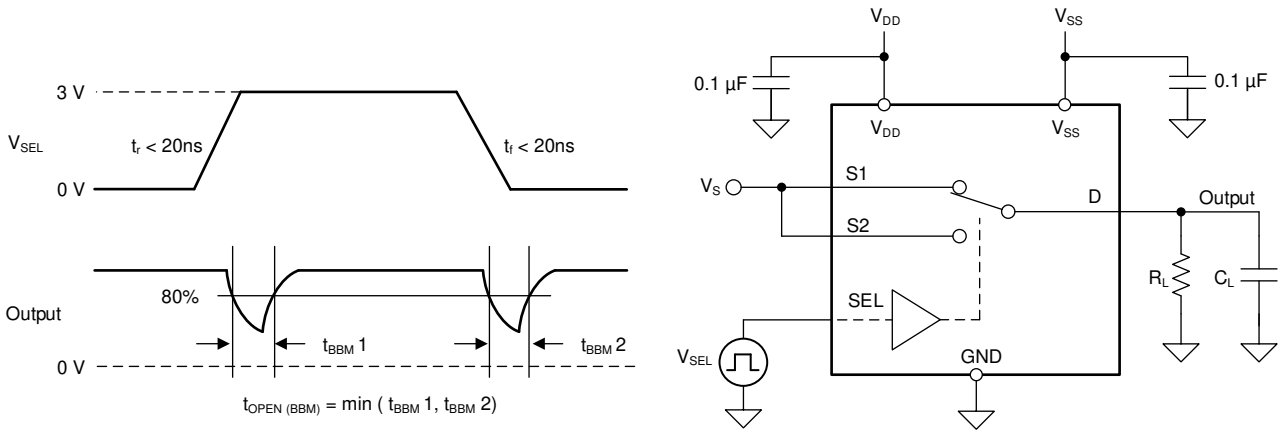



图 7-5. Break-Before-Make Delay Measurement Setup

## 7.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-6 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-6 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

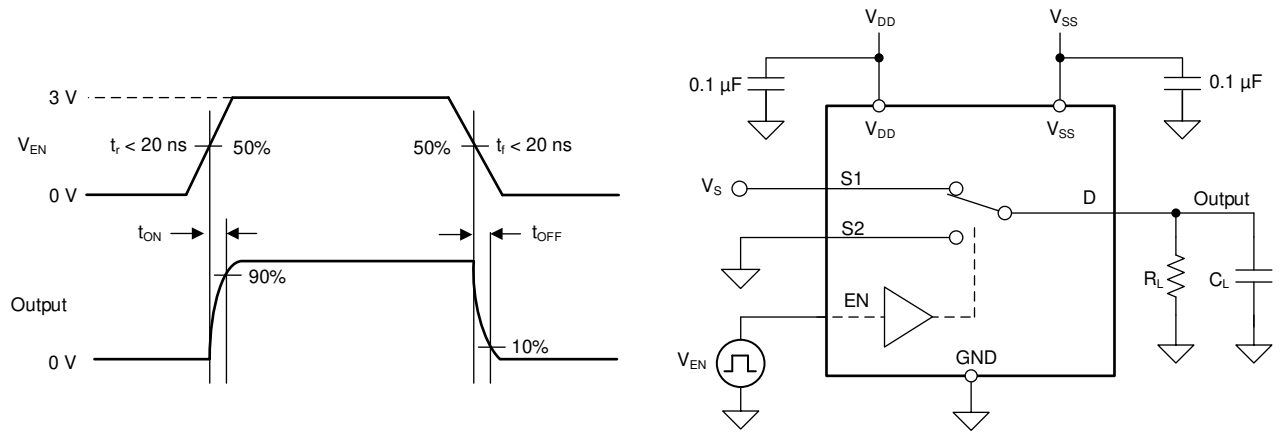



图 7-6. Turn-On and Turn-Off Time Measurement Setup

## 7.7 Charge Injection

The TMUX7219 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is

denoted by the symbol $Q_C$. 图 7-7 shows the setup used to measure charge injection from source (Sx) to drain (D).

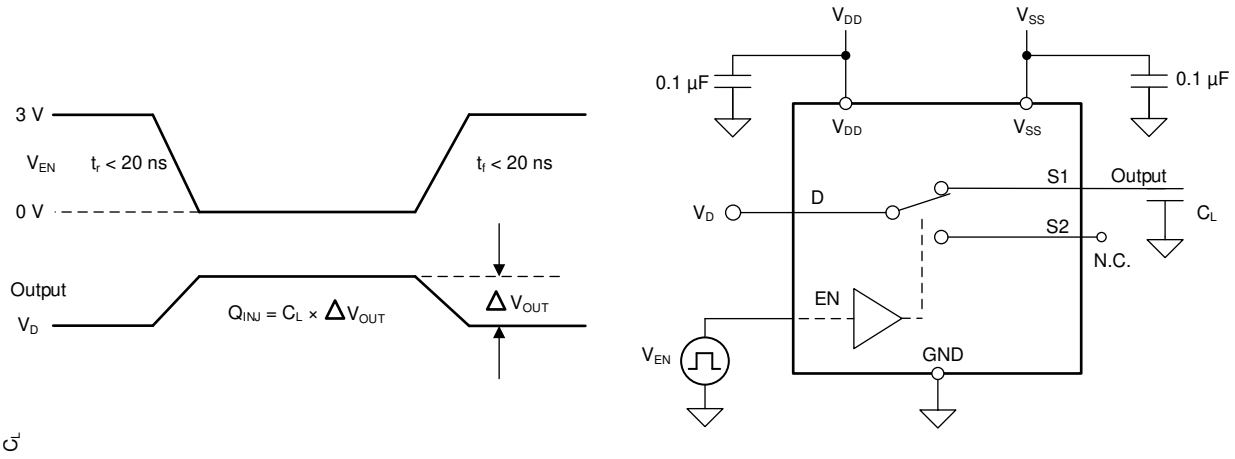
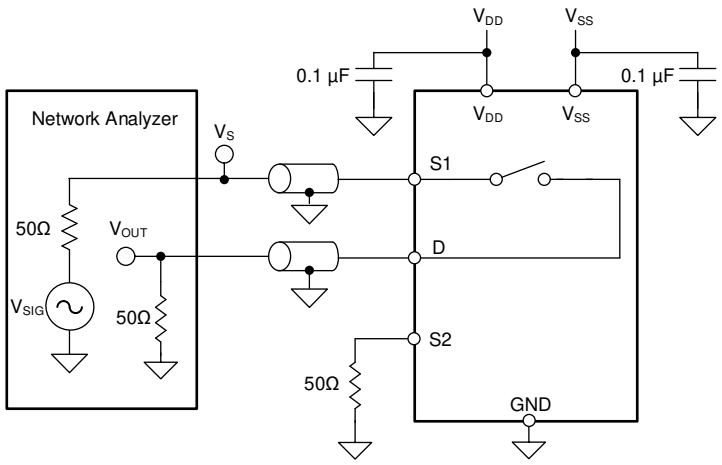



**图 7-7. Charge-Injection Measurement Setup**

## 7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 7-8 shows the setup used to measure, and the equation used to calculate off isolation.




$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

**图 7-8. Off Isolation Measurement Setup**

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

## 7.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 7-9 shows the setup used to measure, and the equation used to calculate crosstalk.

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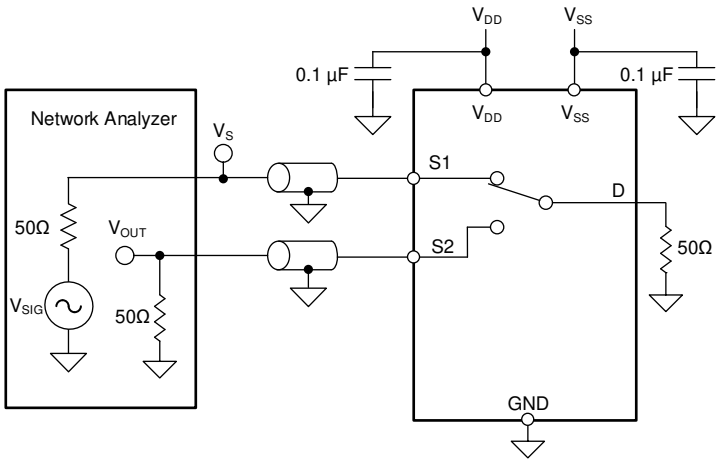
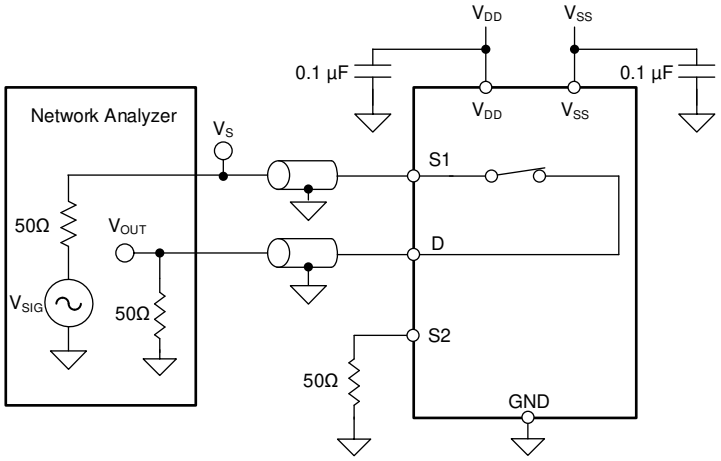



$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

**图 7-9. Crosstalk Measurement Setup**

## 7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 7-10 shows the setup used to measure bandwidth.




$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

**图 7-10. Bandwidth Measurement Setup**

## 7.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N.

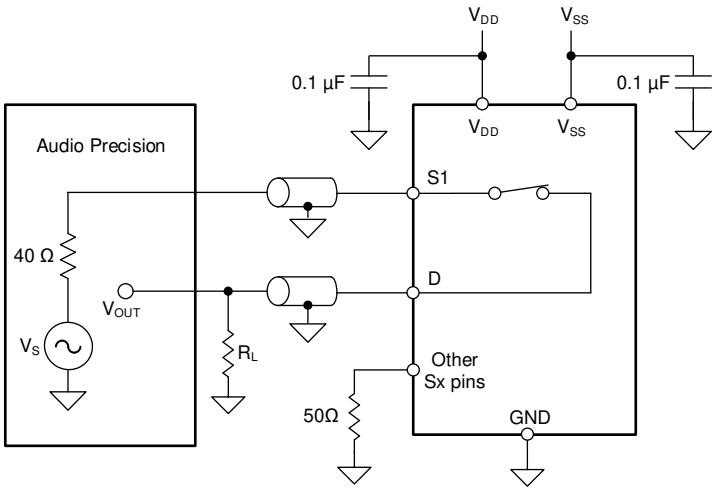
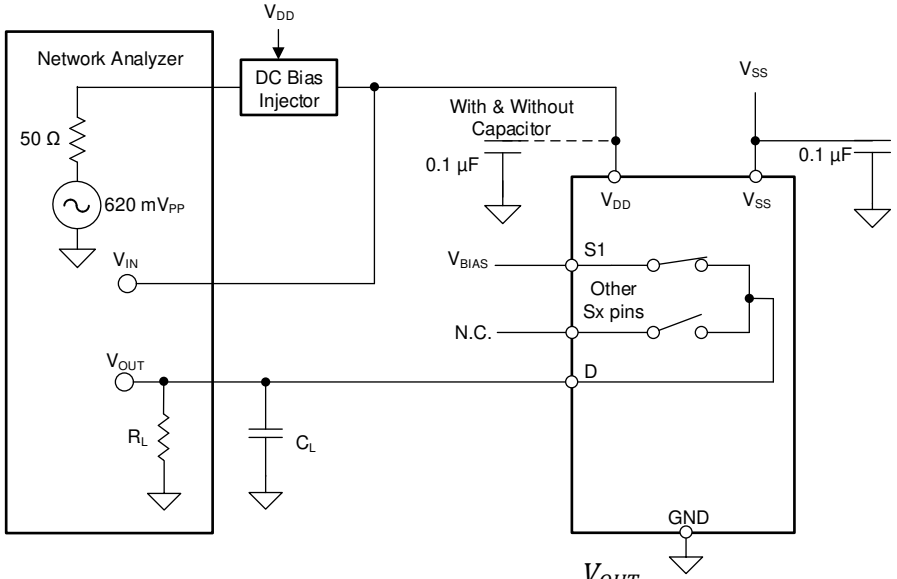



**图 7-11. THD+N Measurement Setup**

## 7.12 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 $mV_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR. A high ratio represents a high degree of tolerance to supply rail variation.

图 6-29 shows how the de-coupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.




$$V_{BIAS} = 1\,V, PSRR = 20 \times Log\frac{V_{OUT}}{V_{IN}}$$

**图 7-12. AC PSRR Measurement Setup**

ADVANCE INFORMATION

# 8 Detailed Description

## 8.1 Overview

The TMUX6219 is an 2:1, 1-channel switch. Each input is turned on or turned off based on the state of the select line and enable pin.

## 8.2 Functional Block Diagram

The TMUX7219 is an 2:1, 1-channel switch. Each input is turned on or turned off based on the state of the select line and enable pin.

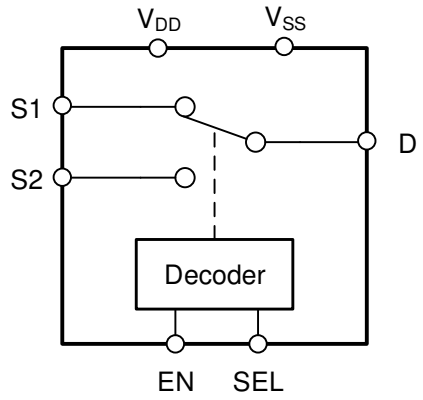



**图 8-1. TMUX7219 Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Bidirectional Operation

The TMUX7219 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

### 8.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX7219 ranges from $V_{SS}$ to $V_{DD}$.

### 8.3.3 1.8 V Logic Compatible Inputs

The TMUX7219 has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the device to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

### 8.3.4 Fail-Safe Logic

The TMUX7219 supports Fail-Safe Logic on the control input pins (EN, SEL) allowing for operation up to 44 V above $V_{SS}$, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX7219 to be ramped to +44 V while $V_{DD}$ and $V_{SS}$ = 0 V. The logic control inputs are protected against positive faults of up to +44 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

### 8.3.5 Latch-Up Immune

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX72xx family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX72xx family of switches and multiplexers to be used in harsh environments.

## 8.4 Device Functional Modes

When the EN pin of the TMUX7219 is pulled high, one of the switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both of the switches are in an open state regardless of the state of the SEL pin. The control pins can be as high as 44 V.

The TMUX7219 can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins must be tied to GND or $V_{DD}$ in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (S1, S2, or D) should be connected to GND.

## 8.5 Truth Tables

表 8-1 show the truth tables for the TMUX7219.

**表 8-1. TMUX7219 Truth Table**

| EN | SEL | Selected Source Connected To Drain (D) Pin |
|---|---|---|
| 0 | X(1) | All sources are off (HI-Z) |
| 1 | 0 | S1 |
| 1 | 1 | S2 |

(1) X denotes *don't care*.

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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

TMUX7219 is part of the precision switches and multiplexers family of devices. TMUX7219 offers low RON, low on and off leakage currents and ultra-low charge injection performance. These properties make TMUX7219 ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

## 9.2 Typical Application

### 9.2.1 Power Amplifier Gate Driver

One application of the TMUX7219 is for input control of a power amplifier gate driver. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate to $V_{SS}$. The wide dual supply range of ±4.5 V to ±18 V allows the switch to work with GaN power amplifiers and the wide single supply range 4.5 V to 36 V works well with LDMOS power amplifiers.

图 9-1 shows the TMUX7219 configured for control of the power amplifier gate driver in GaN application.

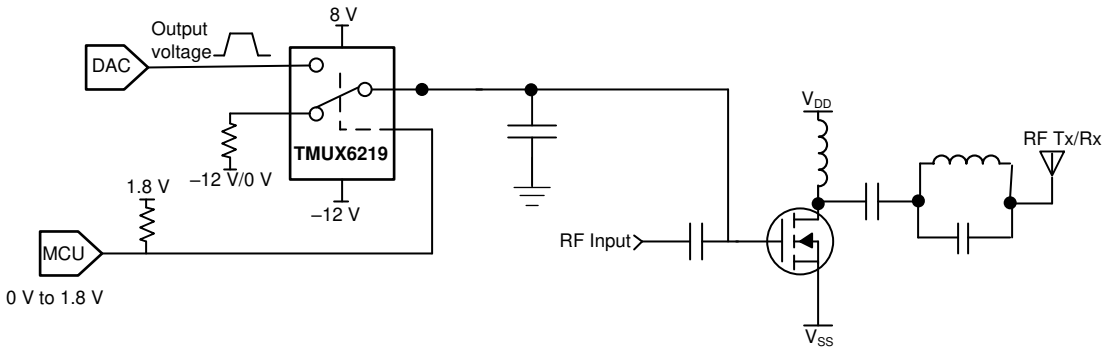


**图 9-1. Power Amplifier Gate Driver**

#### *9.2.1.1 Design Requirements*

For this design example, use the parameters listed in 表 9-1.

**表 9-1. Design Parameters**

| PARAMETERS | VALUES | |
|---|---|---|
| | GAN application | LDMOS application |
| Supply ($V_{DD}$) | 8 V | 5 V |
| Supply ($V_{SS}$) | -12 V | 0 V |
| MUX I/O signal range | -12 V to 8 V (Rail-to-Rail) | 0 V to 5 V (Rail-to-Rail) |
| Control logic thresholds | 1.8 V compatiable (up to $V_{DD}$) | 1.8 V compatiable (up to $V_{DD}$) |
| EN | EN pulled high to enable the switch | EN pulled high to enable the switch |

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#### 9.2.1.2 Detailed Design Procedure

The application shown in 图 9-1 demonstrates how to toggle between the DAC output and low signal voltage for control of a GaN power amplifier using a single control input. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pin of the switch. The TMUX7219 can support 1.8 V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX7219 can be operated without any external components except for the supply decoupling capacitors. The select pin has an internal pull-down resistor to prevent floating input logic. All inputs to the switch must fall within the recommend operating conditions of the TMUX7219 including signal range and continuous current. For this design with a positive supply of 8 V on $V_{DD}$, and negative supply of -12 V on $V_{SS}$, the signal range can be 8 V to -12 V. The max continuous current ($I_{DC}$) can be up to 330 mA as shown in 节 6.4 for wide-range current measurement.

## 10 Power Supply Recommendations

The TMUX7219 operates across a wide supply range of of ±4.5 V to ±22 V (4.5 V to 44 V in single-supply mode). The device also perform well with asymmetrical supplies such as $V_{DD}$ = 12 V and $V_{SS}$= – 5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF at both the $V_{DD}$ and $V_{SS}$ pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Always ensure the ground (GND) connection is established before supplies are ramped.

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# 11 Layout

## 11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self – inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

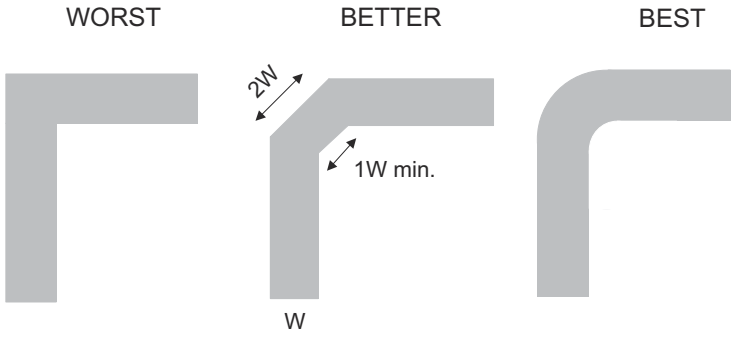


**图 11-1. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 11-2 illustrates an example of a PCB layout with the TMUX7219. Some key considerations are:

- Decouple the supply pins with a 0.1-µF and 1 µF capacitor, placed lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

## 11.2 Layout Example

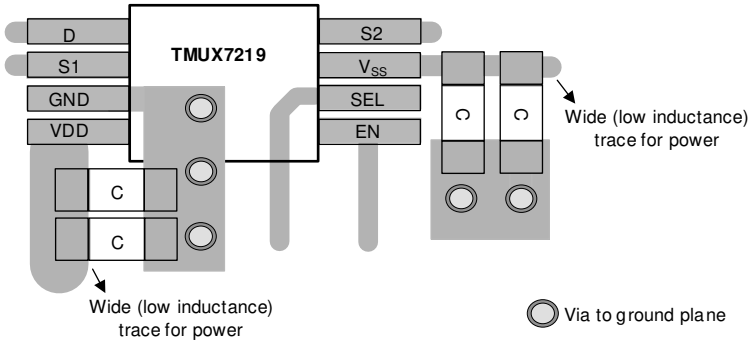


**图 11-2. TMUX7219 Layout Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.

Texas Instruments, *QFN/SON PCB Attachment*.

Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.

Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*.

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

# 重要声明和免责声明

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX7219DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | X219 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

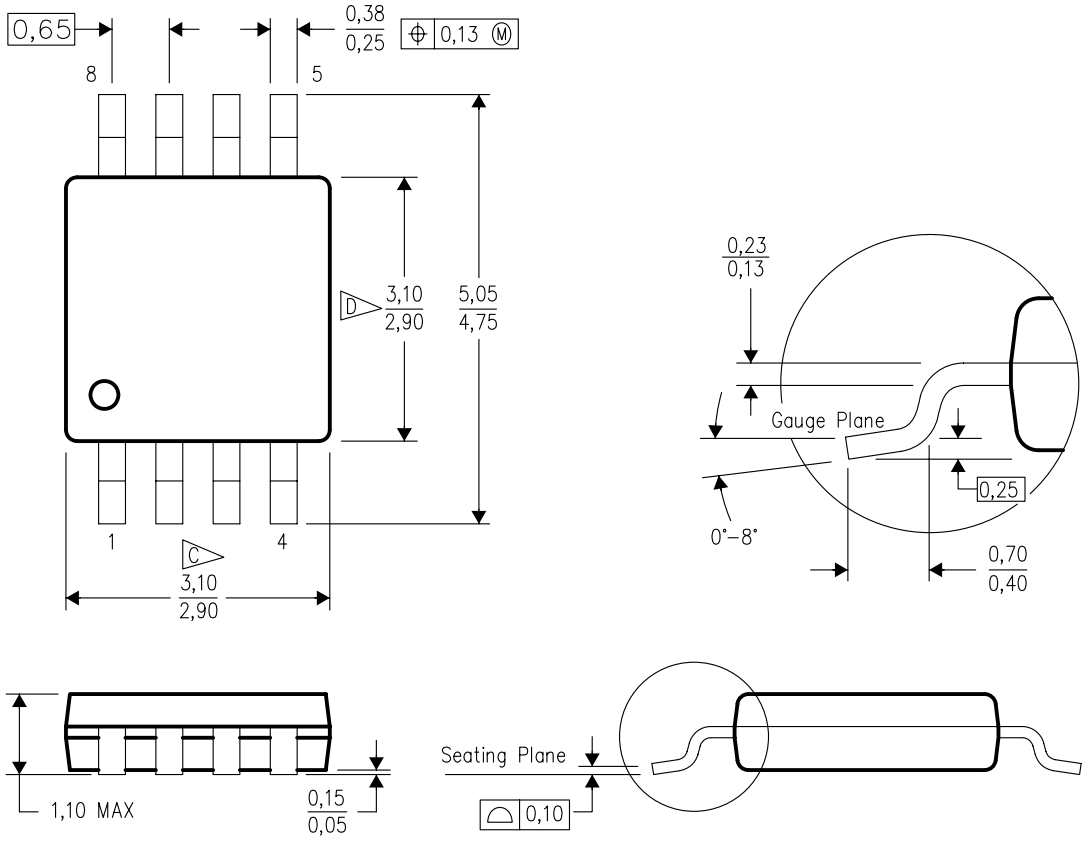
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

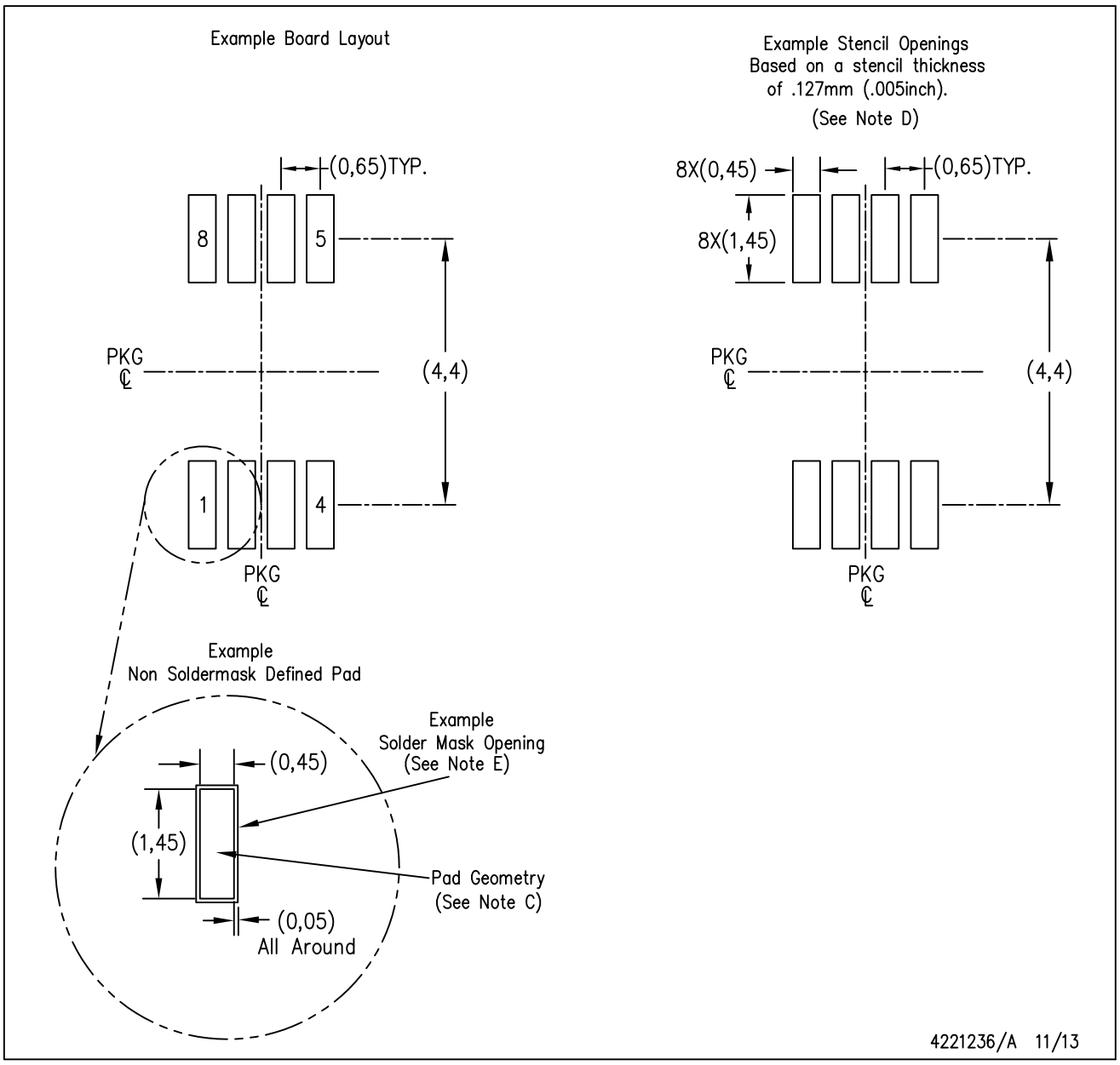
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122