TMAG5170-Q1 3-Axis Linear Hall Effect Sensor With SPI Interface

1 Features

- AEC-Q100 Qualified With the Following Result:
  - Temperature Grade 0: –40 °C to 150 °C
- High Precision with <±2% Sensitivity Error
- Integrated Temperature Compensation for Multiple Magnet Types
- Individually Selectable Linear Magnetic Sensitivity Range at X, Y, or Z Axis:
  - TMAG5170A1-Q1: ±25, ±50, ±100 mT
  - TMAG5170A2-Q1: ±133, ±200, ±300 mT
- 10-MHz Serial Peripheral Interface (SPI)
- Maximum 40-Ksps Conversion Rate per Axis
- 2.3-V to 5.5-V Primary Supply Range
- Designed for Functional Safety Applications According to ISO 26262
- Integrated Angle CORDIC calculation with Gain and Offset Adjustment

2 Applications

- Electric Power Steering
- Steering Wheel Control
- Shifter System
- Multi-function Knobs
- Door Open/ Close Sensor
- Joystick
- Brake System
- Wiper Module
- Robotic Arm Sensor
- E-Bikes
- Ambient Current Sensor

3 Description

The TMAG5170-Q1 is a 3-axis linear Hall effect sensor designed for automotive and industrial applications. This device integrates 3 independent Hall sensors in X, Y, and Z axes. A precision analog signal-chain along with integrated 12-bit ADC digitizes the measured analog magnetic field values. The SPI interface can be used by an external micro-controller to configure the device, start a conversion, or to read back the device register data. On-chip integrated temperature sensor data is available for multiple system functions such as safety check and temperature compensation for a given magnetic field measurement.

The TMAG5170-Q1 can be configured through the SPI to enable any number of magnetic axes and temperature measurements for a particular application. Dedicated $\overline{ALERT}$ pin enables low-power system operation, and can be used by a micro-controller to trigger a new conversion.

The device is offered in two different orderables for separate magnetic field ranges. Each orderable part can be configured further to select one of three magnetic field ranges that suits the magnet strength and component placements during system calibration. The high level of integration provides flexibility and cost effectiveness in a wide array of sensing system implementations.

The device performs consistently across a wide ambient temperature range of –40 °C to +150 °C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMAG5170-Q1	VSSOP (8)(2)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

(2) TMAG5170A1-Q1 is Advanced Information. TMAG5170A2-Q1 is Preview only.

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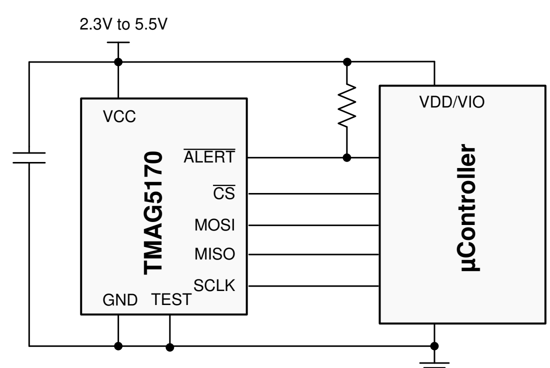
Application Block Diagram



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4 Revision History

DATE	REVISION	NOTES
June 2020	*	Initial release.

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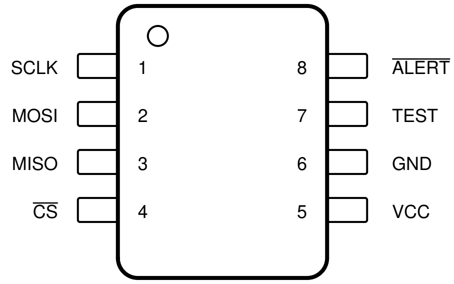
5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	SCLK	I	Serial clock
2	MOSI	I	Master output slave input
3	MISO	O	Master input slave output
4	$\overline{\text{CS}}$	I	Chip select
5	VCC	P	Main power supply. Handles 2.3-V to 5.5-V power supply input
6	GND	G	Ground reference
7	TEST	P	TI Test pin. Should be grounded in application
8	$\overline{\text{ALERT}}$	I/O	Status output/Trigger

(1) I = input, O = output, I/O = input and output, G = ground, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{VCC}	Main supply voltage	–0.3	7	V
I_{OUT}	Output current, MISO, $\overline{\text{ALERT}}$	–10	10	mA
V_{OUT}	Output voltage, MISO, $\overline{\text{ALERT}}$	–0.3	7	V
V_{IN}	Input voltage, MOSI, $\overline{\text{CS}}$, SCLK	–0.3	V_{VCC}+ 0.3	V
B_{MAX}	Magnetic flux density		Unlimited	T
T_J	Junction temperature	–40	170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Thermal Information

THERMAL METRIC[1]		TMAG5170-Q1 DGK (8-MSOP) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VCC}	Main supply voltage	2.3		5.5	V
I_{OUT}	Output current, MISO	–2		2	mA
I_{OUT}	Output current, $\overline{\text{ALERT}}$	0		2	mA
V_{IH}	Input HIGH voltage, MOSI, $\overline{\text{CS}}$, SCLK	0.8			V_{VCC}
V_{IL}	Input LOW voltage, MOSI, $\overline{\text{CS}}$, SCLK			0.2	V_{VCC}
T_A	Operating free air temperature	-40		150	C

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MISO, $\overline{\text{ALERT}}$						
V_{OH}	Output HIGH voltage, MISO pin	I_{OUT} = -2mA	V_{CC} –0.4		V_{CC}	V
V_{OL}	Output LOW voltage, MISO pin	I_{OUT} = 2mA	0		0.4	V
V_{OL}	Output LOW voltage, $\overline{\text{ALERT}}$ pin	I_{OUT} = 2mA	0		0.4	V
$t_{FALL\_\overline{ALERT}}$	$\overline{\text{ALERT}}$ output fall time	R_{PU} =10KΩ, C_L =20pF, V_{CC} =2.3V to 5.5V		50		ns
$t_{\overline{ALERT}}$	$\overline{\text{ALERT}}$ output pulse width with conversion complete or threshold cross interrupt event	ALERT_MODE =0b, Interrupt & Trigger Mode		5		µs
$t_{\overline{ALERT}}$	$\overline{\text{ALERT}}$ output pulse width with other interrupt events	ALERT_MODE =0b, Interrupt & Trigger Mode		31		µs
I_{OZ}	Output Leakage current, $\overline{\text{ALERT}}$ pin	ALERT pin disabled, V_{OZ} = 5.5V	0		100	nA
DC Power						
V_{VCC_UV}	Under voltage threshold at VCC			2.1		V
V_{VCC_OV}	Over voltage threshold at VCC			5.9		V
I_{ACT}	Active mode current from VCC	$\overline{\text{CS}}$ high, VCC = 5.5V		3.4		mA
I_{STDBY}	Stand-by mode current from VCC	$\overline{\text{CS}}$ high, VCC = 5.5V		840		µA
I_{CFG}	Configuration mode current from VCC	$\overline{\text{CS}}$ high, VCC = 5.5V		60		µA
I_{SLP}	Sleep mode current from V_{CC}	$\overline{\text{CS}}$ high, VCC = 5.5V		1.5		µA
I_{DEEP_SLP}	Deep sleep mode current from VCC	$\overline{\text{CS}}$ high, VCC = 5.5V		5		nA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Power						
$I_{VCC\ DCM}$	Duty-cycle mode current consumption, one channel enabled, CONV_AVG = 000	Data active rate 1000Hz, V_{VCC} = 5V		245		µA
		Data active rate 100Hz, V_{VCC} = 5V		32		µA
		Data active rate 10Hz, V_{VCC} = 5V		4.5		µA
		Data active rate 1Hz, V_{VCC} = 5V		1.5		µA
	Duty-cycle mode current consumption, two channels enabled, CONV_AVG = 000	Data active rate 1000Hz, V_{VCC} = 5V		292		µA
		Data active rate 100Hz, V_{VCC} = 5V		39		µA
		Data active rate 10Hz, V_{VCC} = 5V		5		µA
		Data active rate 1Hz, V_{VCC} = 5V		1.6		µA
Operating Speed						
$t_{measure}$	Conversion time (1)	CONV_AVG = 000, OPERATING_MODE =010, only one channel enabled (2)		45		µs
		CONV_AVG = 101, OPERATING_MODE =010, only one channel enabled (3)		820		µs
f_{HFOSC}	Internal high-frequency oscillator speed			3.2		MHz
f_{LFOSC}	Internal low-frequency oscillator speed			16		KHz
Temperature Sensing						
T_{SENS_RANGE}	Temperature sensing range		–40		170	C
T_{SENS_T0}	Reference temperature for $TADC_{T0}$			25		C
$TADC_{T0}$	TEMP_RESULT decimal value @ T_{SENS_T0}			17508		
$TADC_{RES}$	Temp sensing resolution			60.1		LSB/C
NRMS (T)	RMS (1 Sigma) temperature noise	CONV_AVG = 101		0.14		C
NRMS (T)	RMS (1 Sigma) temperature noise	CONV_AVG = 000		0.35		C

(1) To calculate the time between conversion request and the availibility of the conversion result, add the initialization time to the $t_{measure}$ as explained in INITIALIZATION TIME TO START CONVERSION. For continuous conversion, the initialization time is applicable only for the first conversion.
(2) Add 25µs for each additional channel enabled for conversion with CONV_AVG =000.
(3) For conversion with CONV_AVG =101, each axis data is collected 32 times. If an additional channel is enabled with CONV_AVG =101, add 32×25µs = 800µs to the $t_{measure}$ to calculate the conversion time for two axes.

6.6 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TMAG5170A1						
B_{IN_A1}	Linear magnetic range	x_RANGE =00b		±50		mT
		x_RANGE =01b		±25		mT
		x_RANGE =10b		±100		mT
$SENS_{50\_A1}$	Sensitivity, X, Y, or Z axis	x_RANGE =00b		654		LSB/mT
$SENS_{25\_A1}$		x_RANGE =01b		1308		LSB/mT
$SENS_{100\_A1}$		x_RANGE =10b		326		LSB/mT
$SENS_{ER\_25C\_A1}$	Sensitivity error, X, Y, Z axis	T_A = 25℃	–1.1%	±0.1%	1.1%	
$SENS_{LER\_XY\_A1}$	Sensitivity Linearity Error, X, Y-axis	T_A = 25℃		±0.1%		
$SENS_{LER\_Z\_A1}$	Sensitivity Linearity Error, Z axis			±0.05%		

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Magnetic Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$SENS_{MS\_XY\_A1}$	Sensitivity mismatch among X-Y axes	T_A = 25℃	–1.1%	±0.15%	1.1%	
$SENS_{MS\_Z\_A1}$	Sensitivity mismatch among Y-Z, or X-Z axes	T_A = 25℃		±0.15%		
$SENS_{MS\_DR\_XY\_A1}$	Sensitivity mismatch drift X-Y axes	T_A =-40℃ to 150℃		±0.2%		
$SENS_{MS\_DR\_Z\_A1}$	Sensitivity mismatch drift Y-Z, or X-Z axes			±0.2%		
B_{off_A1}	Offset	x_RANGE - 00, T_A = 25℃		±0.15		mT
$B_{off\_TC\_A1}$	Offset drift from value at T_A = 25℃	T_A =-40℃ to 150℃		-2		µT/°C
$N_{RMS\_XY\_FAST\_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	CONV_AVG = 000, T_A = 25℃		±0.140		mT
$N_{RMS\_XY\_SLOW\_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	CONV_AVG = 101, T_A = 25℃		±0.025		mT
$N_{RMS\_Z\_FAST\_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	CONV_AVG = 000, T_A = 25℃		±0.064		mT
$N_{RMS\_Z\_SLOW\_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	CONV_AVG = 101, T_A = 25℃		±0.011		mT
TMAG5170A2						
B_{IN_A2}	Linear magnetic range	x_RANGE =00b		±200		mT
		x_RANGE =01b		±133		mT
		x_RANGE =10b		±300		mT
$SENS_{50\_A2}$	Sensitivity, X, Y, or Z axis	x_RANGE =00b		162		LSB/mT
$SENS_{25\_A2}$		x_RANGE =01b		246		LSB/mT
$SENS_{100\_A2}$		x_RANGE =10b		108		LSB/mT
$SENS_{ER\_25C\_A2}$	Sensitivity error, X, Y, Z axis	T_A = 25℃		±0.5%		
$SENS_{LER\_XY\_A2}$	Sensitivity Linearity Error, X, Y-axis	T_A = 25℃		±0.1%		
$SENS_{LER\_Z\_A2}$	Sensitivity Linearity Error, Z axis	T_A = 25℃		±0.1%		
$SENS_{MS\_XY\_A2}$	Sensitivity mismatch among X-Y axes	T_A = 25℃		±0.15%		
$SENS_{MS\_Z\_A2}$	Sensitivity mismatch among Y-Z, or X-Z axes	T_A = 25℃		±0.15%		
$SENS_{MS\_DR\_XY\_A2}$	Sensitivity mismatch drift X-Y axes	T_A =-40℃ to 150℃		±0.2%		
$SENS_{MS\_DR\_Z\_A2}$	Sensitivity mismatch drift Y-Z, or X-Z axes	T_A =-40℃ to 150℃		±0.2%		
B_{off_A2}	Offset	x_RANGE - 00, T_A = 25℃		±0.15		mT
$N_{RMS\ (X,\ Y)}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	CONV_AVG = 000, T_A = 25℃		±0.150		mT
$N_{RMS\ (X,\ Y)}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	CONV_AVG = 101, T_A = 25℃		±0.026		mT
$N_{RMS\ (Z)}$	RMS (1 Sigma) magnetic noise (Z axis)	CONV_AVG = 000, T_A = 25℃		±0.075		mT
$N_{RMS\ (Z)}$	RMS (1 Sigma) magnetic noise (Z axis)	CONV_AVG = 101, T_A = 25℃		±0.014		mT

Magnetic Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE COMPENSATION						
TC	Temperature compensation (X or Y-axis)	TEMPCO =00		0		%/°C
	Temperature compensation (Z-axis)			0		
	Temperature compensation (X or Y-axis)	TEMPCO =01		0.12		
	Temperature compensation (Z-axis)			0.12		
	Temperature compensation (X or Y-axis)	TEMPCO =11		0.2		
	Temperature compensation (Z-axis)			0.2		

6.7 Power up Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} = 5.5V						
$t_{start\_power\_up}$	Time to start up after V_{VCC} supply voltage crossing V_{VCC_MIN}			100	240	µs
t_{start_sleep}	Time to activate from sleep mode (master controlled or duty cycled)			90	200	µs
$t_{start\_deep\_sleep}$	Time to start up from deep sleep mode			100	240	µs
t_{stand_by}	Time to go to Stand-by mode from Configuration mode			90	213	µs
t_{spi_sleep}	Setup time between $\overline{CS}$ going low and SCLK start during sleep mode			8	10	µs
V_{CC} =2.3V						
$t_{start\_power\_up}$	Time to start up after V_{CC} supply voltage crossing V_{CC_MIN}			180	420	µs
t_{start_sleep}	Time to activate from sleep mode (master controlled or duty cycled)			120	250	µs
$t_{start\_deep\_sleep}$	Time to start up from deep sleep mode			180	420	µs
t_{stand_by}	Time to go to Stand-by mode from Configuration mode			90	213	µs
t_{spi_sleep}	Delay time between $\overline{CS}$ going low and SCLK start during sleep mode			8	10	µs

6.8 SPI Interface Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI Interface						
f_{SPI}	SPI clock (SCLK) frequency	LOAD = 25 pF			10	MHz
t_{whigh}	High time: SCLK logic high time duration		45			ns
t_{wlow}	Low time: SCLK logic low time duration		45			ns
t_{su_cs}	$\overline{CS}$ setup time: Time delay between falling edge of $\overline{CS}$ and rising edge of SCLK		45			ns
t_{h_cs}	Hold time: Time between the falling edge of SCLK and rising edge of $\overline{CS}$		45			ns
t_{pd_soen}	Delay time: Time delay from falling edge of $\overline{CS}$ to data valid at MISO				45	ns
t_{pd_sodis}	Delay time: Time delay from rising edge of $\overline{CS}$ to MISO transition to tristate				55	ns
t_{su_si}	MOSI setup time: Setup time of MOSI before the rising edge of SCLK		25			ns

SPI Interface Timing (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{h_si}	Hold time: Time between the rising edge of SCLK to MOSI valid		25			ns
t_{pd_so}	Propagation delay from falling edge of SCLK to MISO				45	ns
t_{w_cs}	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high.	LOAD = 25 pF	100			ns
t_{spi_sleep}	Setup time between $\overline{CS}$ going low and SCLK start during sleep mode			8	10	µs

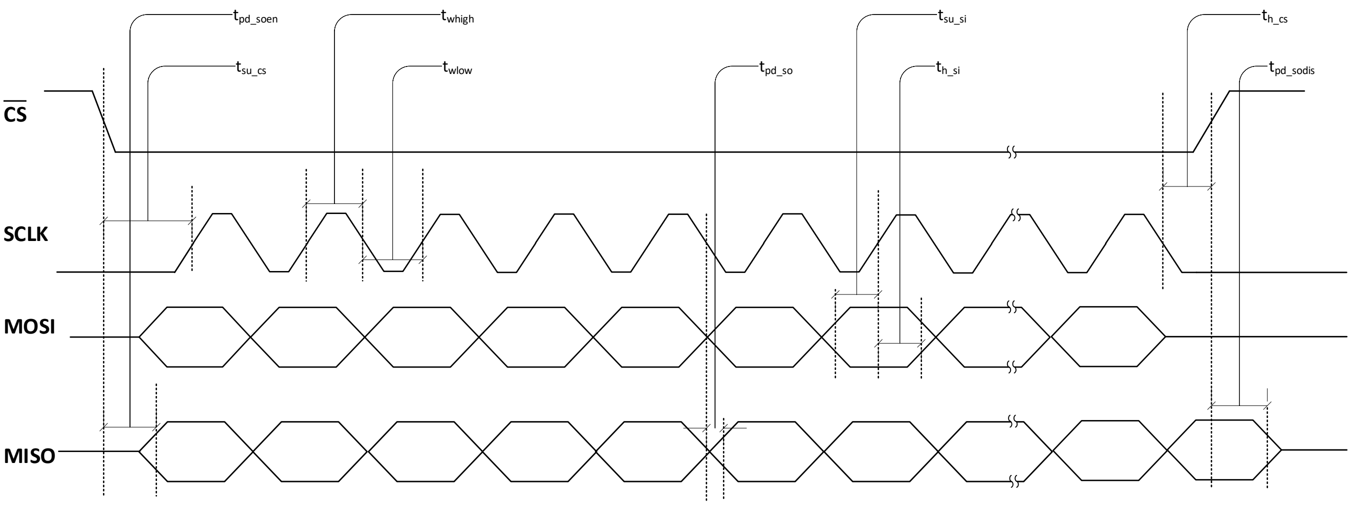


Figure 1. SPI Timing Parameters

7 Detailed Description

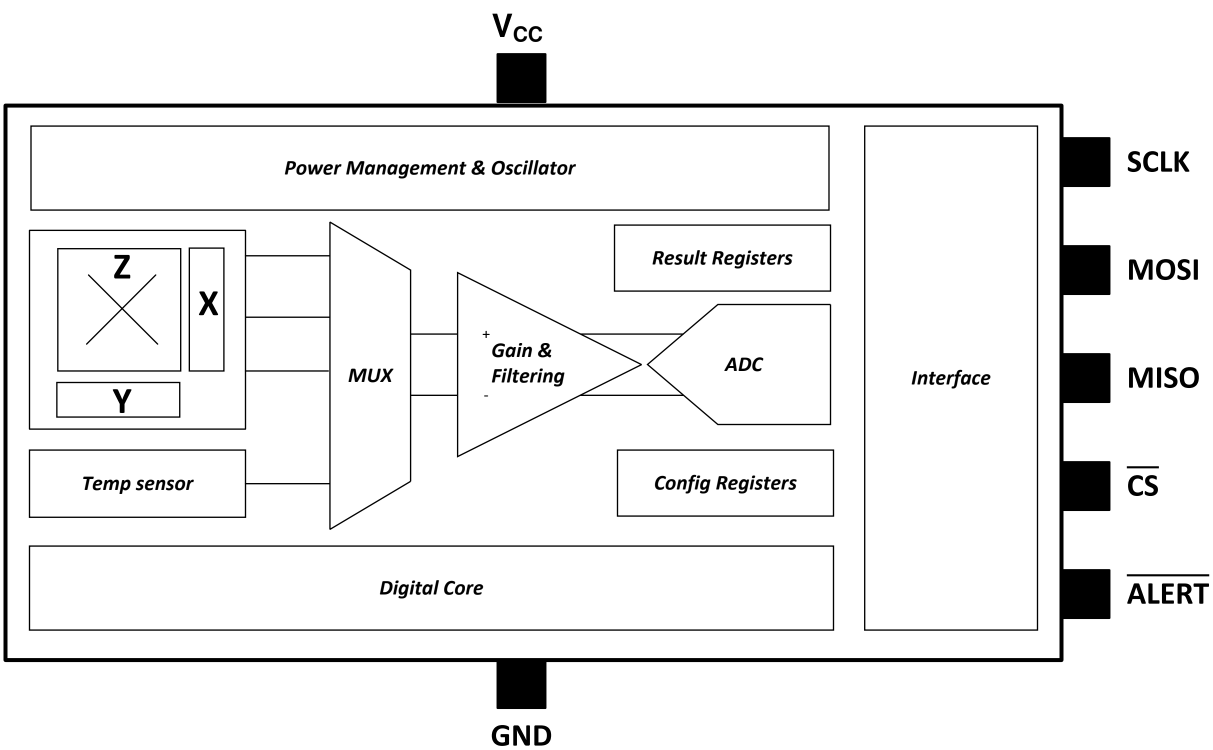
7.1 Overview

The TMAG5170-Q1 IC is based on the Hall effect technology and precision mixed signal circuitry from Texas Instruments. The output signals (raw X, Y, Z Magnetic data and Die temperature data) is provided through the SPI interface. The device can be configured in multiple settings through user access registers through the SPI interface.

The IC consists of the following functional and building blocks:

- The power mode control system supports one VCC rail, containing a low-power oscillator, basic biasing, accurate reset, undervoltage, overvoltage detection, and a fast oscillator.
- The sensing and temperature measurement block contains the HALL biasing, HALL probes with multiplexers, noise filters, temperature sensor, and ADC. The Hall sensor data and temperature data are multiplexed through the same ADC
- The SPI interface, containing the register files and I/O pads. The TMAG5170-Q1 supports SPI interface along with integrated cyclic redundancy check (CRC).
- The safety block is embedded in the circuitry to enable mandatory and user enabled safety checks.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Magnetic Flux Direction

The TMAG5170-Q1 is sensitive to the magnetic field component in X, Y, and Z directions. The X and Y fields are in plane with the package. The Z filed is perpendicular to the top of the package. The device is sensitive to both magnetic north and south poles in each axis. As shown in Figure 2, the device will generate positive ADC codes in response to a magnetic south pole in the proximity. Similarly, the device will generate negative ADC codes if magnetic north poles approach from the same directions.

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Feature Description (continued)

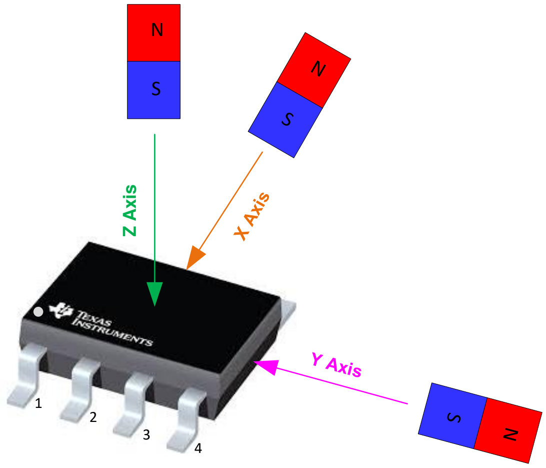

Figure 2. Direction of Applied Magnetic South Pole to Generate Positive ADC Codes

7.3.2 Sensor Location

Figure 3 shows the location of X, Y, Z hall elements inside the TMAG5170-Q1.

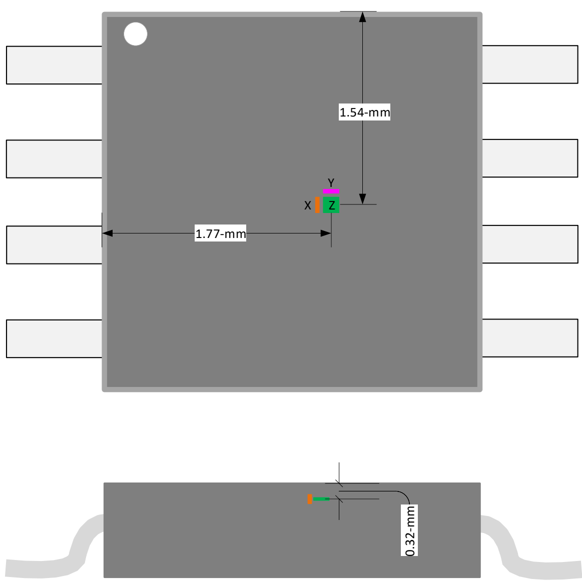

Figure 3. Location of X, Y, Z Hall Elements

Feature Description (continued)

7.3.3 Magnetic Range Selection

Table 1 shows the magnetic range selection for the TMAG5170-Q1 device. Each axis range can be independently selected irrespective of the others.

Table 1. Magnetic Range Selection

	RANGE REGISTER SETTING	TMAG5170A1-Q1	TMAG5170A2-Q1	COMMENT
X Axis Field	X_RANGE = 00b	±50 mT	±200 mT	
	X_RANGE = 01b	±25 mT	±133 mT	Best resolution case
	X_ RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case
Y Axis Field	Y_RANGE = 00b	±50 mT	±200 mT	
	Y_RANGE = 01b	±25 mT	±133 mT	Best resolution case
	Y_RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case
Z Axis Field	Z_RANGE = 00b	±50 mT	±200 mT	
	Z_RANGE = 01b	±25 mT	±133 mT	Best resolution case
	Z_RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case

7.3.4 Update Rate Settings

The TMAG5170-Q1 offers multiple update rates for system design flexibility. Figure 5 shows the different update rate settings for the TMAG5170-Q1.

Table 2. Update Rate Settings

OPERATING MODE	REGISTER SETTING	UPDATE RATE			COMMENT
		SINGLE AXIS	TWO AXIS	THREE AXIS	
X, Y, Z Axis	CONV_AVG = 000b	40Ksps	20Ksps	13.3Ksps	Fastest update rate
X, Y, Z Axis	CONV_AVG = 001b	20Ksps	10Ksps	6.65Ksps	
X, Y, Z Axis	CONV_AVG = 010b	10Ksps	5Ksps	3.33Ksps	
X, Y, Z Axis	CONV_AVG = 011b	5Ksps	2.5Ksps	1.66Ksps	
X, Y, Z Axis	CONV_AVG = 100b	2.5Ksps	1.25Ksps	0.833Ksps	
X, Y, Z Axis	CONV_AVG = 101b	1.25Ksps	0.625Ksps	0.417Ksps	Best SNR case

7.3.5 ALERT Function

The ALERT pin of the TMAG5170-Q1 supports multiple operating modes targeting different applications.

7.3.5.1 Interrupt and Trigger Mode

With ALERT_MODE at default value of 0b, the ALERT output can be configured to generate an interrupt signal for microcontroller when a user defined event occurs. A user defined event can be a conversion completion, or an error from safety diagnostic tests. In this mode, the ALERT pin can also be used to trigger a conversion start using the TRIGGER_MODE register bit.

7.3.5.2 Magnetic Switch Mode

With ALERT_MODE set at 1b, the ALERT output is configured as a magnetic switch. One or multiple magnetic channels can be selected in the ALERT_CONFIG register. The magnetic switch thresholds are determined by the *_THRX_CONFIG register bits setting. If the measured magnetic field is greater than *_HI_THRESHOLD, or smaller than *_LO_THRESHOLD, the ALERT output will assert low. Figure 4 shows the magnetic switch function using the X-axis magnetic field as an example.

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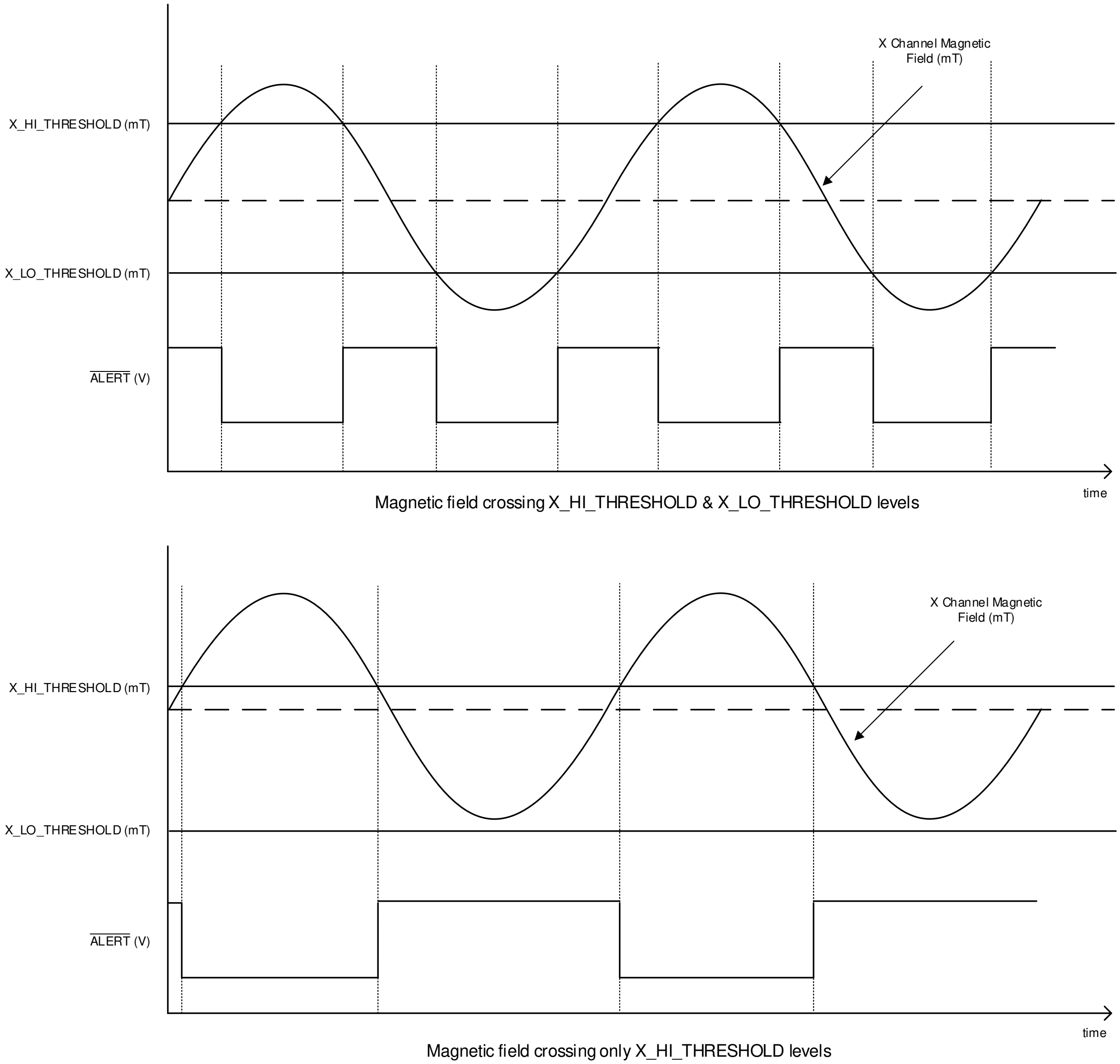

Figure 4. ALERT Pin Working as Magnetic Switch

7.3.6 Threshold Count

The THRX_COUNT bits in the ALERT_CONFIG register offer robust noise filtering and immunity against false tripping while the TMAG5170-Q1 implements the $\overline{\text{ALERT}}$ function for a specific magnetic or temperature threshold crossing. With THRX_COUNT at default 00b, only one measured value must cross the threshold to be considered a valid threshold crossing event. With THRX_COUNT at 11b, four successive measured values must cross the threshold to be considered a valid threshold crossing. An internal counter tracks and records the number of threshold crossing for a given sensor.

The counter resets if any of the below events occur:

- The device meets the threshold cross count for the specified number per the THRX_COUNT bits, the corresponding *CH_THX bit(s) are set, & the SPI read of the SYS_STATUS register has occurred
- If a measured result does not cross the threshold

When the $\overline{\text{ALERT}}$ pin is configured to work as a magnetic switch, the threshold count is active for both low-to-high and high-to-low transitions, offering noise immunity in both directions of the threshold cross.

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7.3.7 Diagnostics

The TMAG5170-Q1 supports several device and system level diagnostics features to detect, monitor, and report failures that either existed before the power up or occurred during device operation.

In the event of a failure, the TMAG5170-Q1 reports back to the master through one or multiple of the following mechanisms:

- ERROR_STAT bit during the MISO read frame
- Direct read of the status registers through the SPI
- ALERT pin response to indicate a failure, if enabled
- No response through MISO line, or CRC error during SPI communication

The TMAG5170-Q1 performs the following device level and system level checks:

7.3.7.1 Device Level Check

- Hall plate sensitivity, biasing and connectivity
- Signal-chain integrity including ADC
- Internal biasing and regulator operation
- Internal memory integrity
- SPI communication integrity
- Pin continuity

7.3.7.2 System Level Check

- Magnetic field outside range
- System temperature outside range
- External supply voltage outside range

7.4 Device Functional Modes

7.4.1 Operating Modes

The TMAG5170-Q1 supports multiple operating modes for wide array of applications as explained in Figure 5. The device starts powering up after the VCC supply crosses the minimum threshold as specified in the *Recommended Operating Conditions* table. Any particular operating mode can be selected by setting the corresponding OPERATING_MODE register bits.

7.4.1.1 Active Mode

The TMAG5170-Q1 coverts the magnetic sensor or temperature data during active mode. Active mode supports both continuous conversion and trigger mode conversion based off the OPERATING_MODE setting. Continuous operation at this mode is useful for applications where the fastest data conversion is required, and power budget is not stringent. In the Active trigger mode, a Master can trigger a conversion through one of several trigger mechanisms as described in the TRIGGER_MODE register bits. Once the conversion started, the time it takes to finish a conversion is denoted by $t_{measure}$. The conversion time can vary widely based off the MAG_CH_EN, CONV_AVG, DIAG_SEL, and DIAG_EN register bits setting. The average current consumption during the active conversion is I_{ACT}.

7.4.1.2 Standby Mode

In this mode, the TMAG5170-Q1 is ready to start sensor conversion with a Master controlled trigger. Several trigger mechanisms are supported per TRIGGER_MODE register bits. At this mode, all analog and digital support circuitry remains on to optimize the faster start of sensor conversion at the command from a Master. This mode offers optimization between system power consumption and fast conversion. The average current consumption at this mode is denoted by I_{STDBY}. The time it takes for the device to go to standby mode from configuration mode is denoted by t_{stand_by}.

Device Functional Modes (continued)

7.4.1.3 Configuration Mode (DEFAULT)

At power up, the TMAG5170-Q1 goes to the configuration mode as default option. In this mode, the SPI communication and user register access are enabled. A Master will configure the device user register bits to select the desired operating mode, sensor data conversion, enable/ disable diagnostic features, and so forth. The average current consumption at this mode is denoted by I_{CFG}. Like the standby mode, the configure mode also support sensor conversion start with a Master controlled trigger. The trigger mechanism is selected by the same TRIGGER_MODE register bits. While comparing with standby mode, the configure mode takes longer to start the sensor conversion while consuming approximately ten times less current.

7.4.1.4 Sleep Mode

The TMAG5170-Q1 supports a sleep mode where it retains the user configuration settings and previous conversion results. A Master can wake up the device from sleep mode through SPI communications, or $\overline{ALERT}$ line. The average power consumption in this mode is denoted by I_{SLP}. The time it takes for the device to go to the configuration mode from the sleep mode is denoted by t_{start_sleep}.

7.4.1.5 Wake-Up and Sleep Mode

The TMAG5170-Q1 supports a power down mode where it can be configured to wake up at a certain interval and measure sensor data per SENSOR_CONFIG register setting. When the data measurement is complete, an $\overline{ALERT}$ signal can be generated to notify the Master that the new conversion data is ready. It is possible to configure the $\overline{ALERT}$ signal generation only in the event a particular magnetic or temperature threshold is exceeded. Detail setting on $\overline{ALERT}$ pin is described in ALERT_CONFIG register. When the active conversion is complete, the TMAG5170-Q1 remains in standby mode for 5-µs before going back to sleep. A Master can wake up the TMAG5170-Q1 and access the data at any time. The average power consumption in the wake-up and sleep mode is denoted by I_{VCC_DCM}. The time it takes for the device to go to configuration mode from wake-up and sleep mode is denoted by t_{start_sleep}.

NOTE

For the ADVANCE INFORMATION device, the SPI read is not supported when the part is in sleep during the wake-up and sleep mode. To read conversion result, exit the wake-up and sleep mode by changing to configuration mode by setting the OPERATING_MODE register bits through a SPI write. For this SPI write, the device response on the MISO line should be ignored.

7.4.1.6 Deep-Sleep Mode

For ultra-low power system, the TMAG5170-Q1 supports a deep-sleep mode to conserve power. In this mode, the TMAG5170-Q1 does not retain the user configuration or previous result data. The device reverts back to factory setting in this mode. The average power consumption in this mode is I_{DEEP_SLP}. The time it takes for the device to go to the configuration mode from the deep-sleep mode is denoted by t_{start_sleep}.

Device Functional Modes (continued)

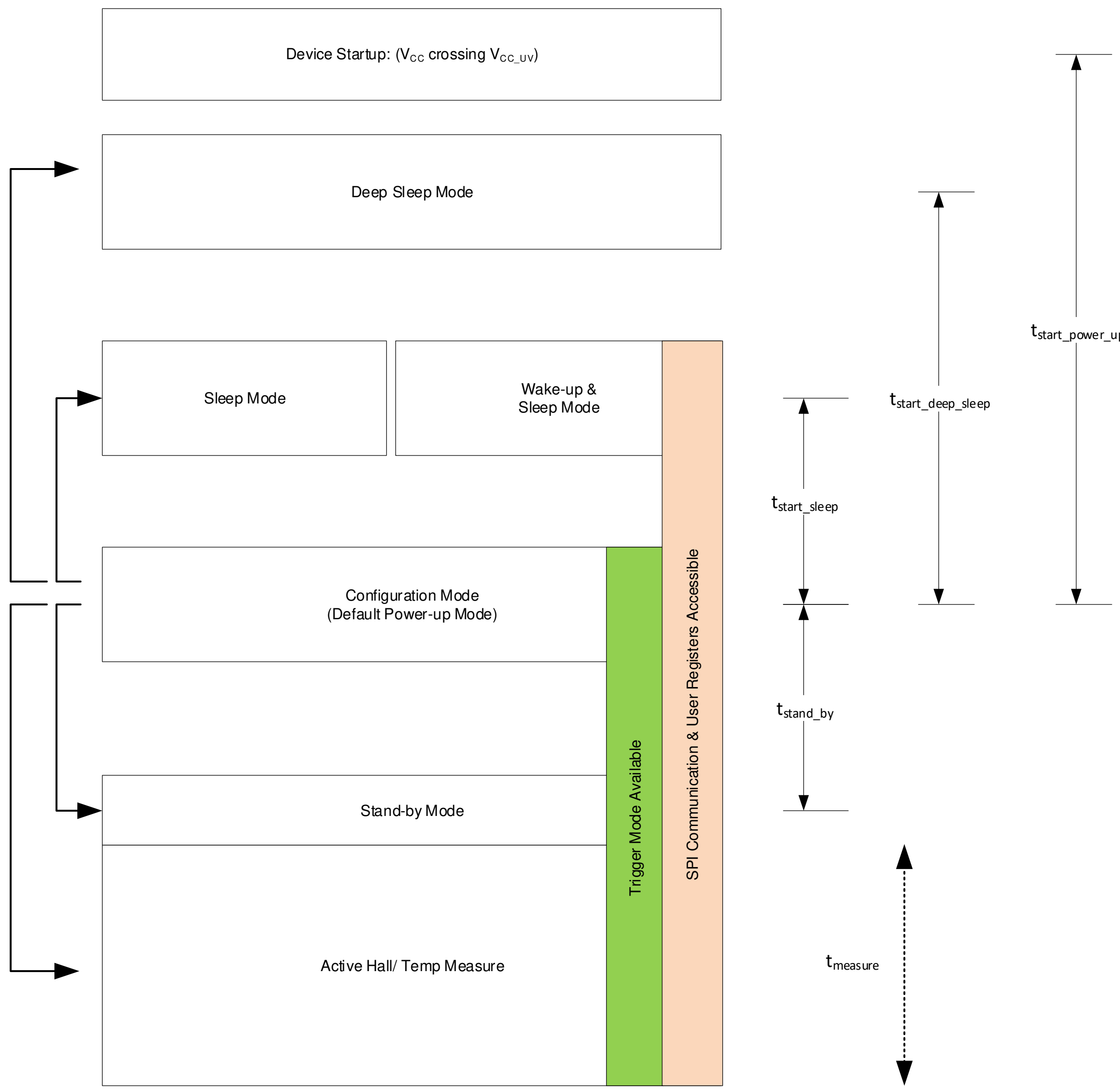


Figure 5. TMAG5170-Q1 Power-Up Sequence

Table 3 shows different power saving modes of the TMAG5170-Q1.

Table 3. Comparing Operating Modes

OPERATING MODE	DEVICE FUNCTION	INITIALIZATION TIME TO START CONVERSION (1)	DATA CONVERSION
Active Conversion	Continuously measuring X, Y, Z axis, or temperature data	10 µs	Supports continuous and trigger mode conversion
Standby Mode	Device is ready to accept SPI commands and start active conversion	35 µs	Supports trigger mode conversion
Configuration Mode	SPI and user configuration registers active	t_{stand_by} + 35 µs	Supports trigger mode conversion
Wake-up & Sleep Mode	Wakes up at a certain interval to measure the X, Y, Z axis, or temperature data	t_{start_sleep} + t_{stand_by} + 35 µs	1, 5, 10, 15, 20, 30, 100, 500, and 1000-ms intervals supported(1).

(1) The timing numbers are typical parameters. Their value may vary depending on the internal oscillator frequency.

Device Functional Modes (continued)

Table 3. Comparing Operating Modes (continued)

OPERATING MODE	DEVICE FUNCTION	INITIALIZATION TIME TO START CONVERSION(1)	DATA CONVERSION
Sleep Mode	Device retains key configuration settings, and last measurement data	t_{start_sleep} + t_{stand_by} + 35 µs	The microcontroller can use sleep mode to implement other power saving intervals not supported by wake-up and sleep mode.
Deep-sleep Mode	Device does not retain key configuration settings, and last measurement data	$t_{start\_deep\_sleep}$ + t_{stand_by} + 35 µs	No conversion start is supported during deep-sleep mode

7.5 Programming

7.5.1 Data Definition

7.5.1.1 Magnetic Sensor Data

The X, Y, and Z magnetic sensor data are stored in the X_CH_RESULT, Y_CH_RESULT, and Z_CH_RESULT registers, respectively. The 12-bit ADC output is stored in 16-bit result registers in 2's complement format as shown in Figure 6. With fastest conversion (CONV_AVG = 000b), the ADC output loads the 12 MSB bits of the 16-bit result register along with 4 LSB bits as zeros. With CONV_AVG ≠ 000b, all the 16 bits are used to store the results. With DATA_TYPE = 00b, the 16-bit magnetic sensor data can be accessed through regular 32-bit SPI read. The measured magnetic field can be calculated using Equation 1.

$$B = \frac{-(D_{15} \times 2^{15}) + \sum_{i=0}^{14} D_i \times 2^i}{2^{16}} \times 2|B_R|$$

where

- B is magnetic field in mT.
- D_i is the data bit as shown in Figure 6.
- B_R is the magnetic range in mT for the corresponding channel. (1)

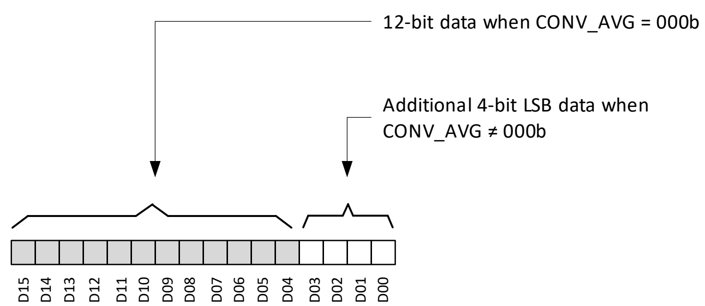


Figure 6. Magnetic Sensor Data Definition

With DATA_TYPE ≠ 00b, the 12 MSB bits from the magnetic result registers can be accessed. In this mode, the measured magnetic field can be calculated using Equation 2.

$$B = \frac{-\left(D_{15} \times 2^{i}\right) + \sum_{i=4}^{14} D_i \times 2^i}{2^{12}} \times 2|B_R| \quad (2)$$

7.5.1.2 Temperature Sensor Data

The TMAG5170-Q1 temperature sensor will measure temperature from –40 °C to 170 °C. The temperature is stored in 16-bit TEMP_RESULT register as shown in Figure 7. With DATA_TYPE = 00b, the 16-bit temperature data can be accessed through regular 32-bit SPI read. The temperature can be calculated using Equation 3.

$$T = T_{SENS\_T0} + \frac{TADC_T - TADC_{T0}}{TADC_{RES}}$$

Programming (continued)

where

- T is the measured temperature in degree celsius.
- T_{SENS_T0} as listed in the *Electrical Characteristics* table.
- $TADC_{RES}$ is the change in ADC code per degree celsius.
- $TADC_{T0}$ as listed in the *Electrical Characteristics* table.
- $TADC_T$ is the measured ADC code for temperature T. (3)

With DATA_TYPE ≠ 00b, the 12 MSB bits from the TEMP_RESULT register can be accessed. In this mode, the temperature can be calculated using Equation 4.

$$T = T_{SENS\_T0} + \frac{16 \times \left(TADC_T - \frac{TADC_{T0}}{16}\right)}{TADC_{RES}} \tag{4}$$

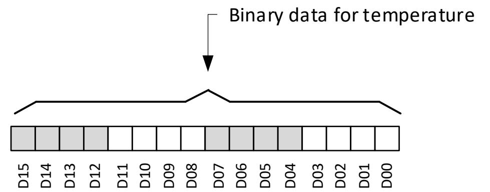


Figure 7. Temperature Sensor Data Definition

7.5.1.3 Angle and Magnitude Data Definition

The TMAG5170-Q1 calculates the angle based off the ANGLE_EN register bit settings. The ANGLE_RESULT register stores the angle information in the 13-LSB bits as shown in Figure 8. Bits D04-D12 store angle integer value from 0 to 360 degree. Bits D00-D03 store fractional angle value with a resolution of 1/16 degree. The 3-MSB bits are always populated as b000. The angle can be calculated using Equation 5.

$$A = \sum_{i=4}^{12} D_i \times 2^i + \frac{\sum_{i=0}^{3} D_i \times 2^i}{16}$$

where

- A is the angle measured in degree.
- D_i is the data bit as shown in Figure 8. (5)

For example: a 354.50 degree is populated as 0001 0110 0010 1000b and a 17.25 degree is populated as 000 0001 0001 0100b.

With DATA_TYPE ≠ 00b, the D01-D12 bits from the ANGLE_RESULT register can be accessed. In this mode, the angle fractional value is represented by 3 bit with resolution of 1/8 degree. The angle in degree can be calculated using Equation 6.

$$A = \sum_{i=4}^{12} D_i \times 2^i + \frac{\sum_{i=1}^{3} D_i \times 2^i}{8} \tag{6}$$

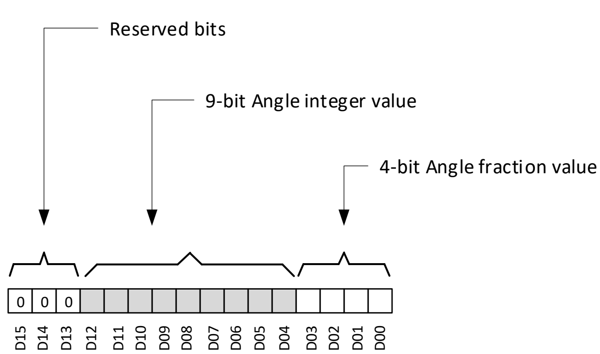


Figure 8. Angle Data Definition

Programming (continued)

During the angle calculation, use Equation 7 to calculate the resultant vector magnitude.

$$M = \sqrt{MADC_{Ch1}{}^2 + MADC_{Ch2}{}^2} \quad (7)$$

where

- $MADC_{Ch1}$, $MADC_{Ch2}$ are the ADC codes of the two magnetic channels selected for the angle calculation.

The magnitude value is stored in the MAGNITUDE_RESULT register as shown in Figure 9. This value should be constant during 360 degree angle measurements.

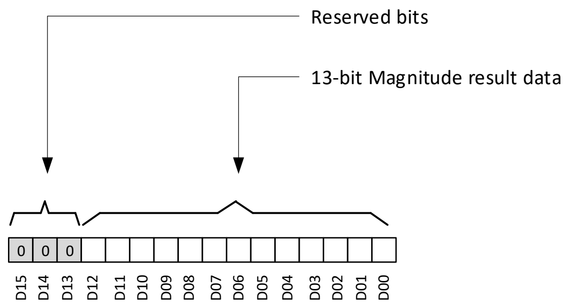


Figure 9. Magnitude Result Data Definition

Magnitude result can be accessed through SPI in 16-bit or 12-bit formats. In the 12-bit format, bit D01 to bit D12 are sent through the SPI.

7.5.2 SPI Interface

The serial peripheral interface (SPI) is a synchronous serial communication interface used for short distance communication, usually between devices on a printed-circuit board assembly. The TMAG5170-Q1 supports a 4-wire SPI interface. The primary communication between the IC and the external microcontroller is through an SPI bus that provides full-duplex communications in a master-slave configuration. The external microcontroller is always an SPI master that sends command requests on the MOSI pin, and receives device responses on the MISO pin. The TMAG5170-Q1 device is always an SPI slave device that receives command requests and sends responses (such as status and measured values) to the external microcontroller over the MISO line. The TMAG5170-Q1 supports a fixed 32-bit frame size to communicate with a master device. However, the 32-bit frame can be configured through DATA_TYPE register bits to support a regular single register read data packet, or a special packet to read two-channel data simultaneously.

7.5.2.1 SCLK

The Serial Clock (SCLK) represents the master clock signal. This clock determines the speed of data transfer and all receiving and sending are done synchronously to this clock. The output data on the MISO pin transitions on the falling edge of the SCLK and input data on the MOSI pin is latched on the rising edge of the SCLK.

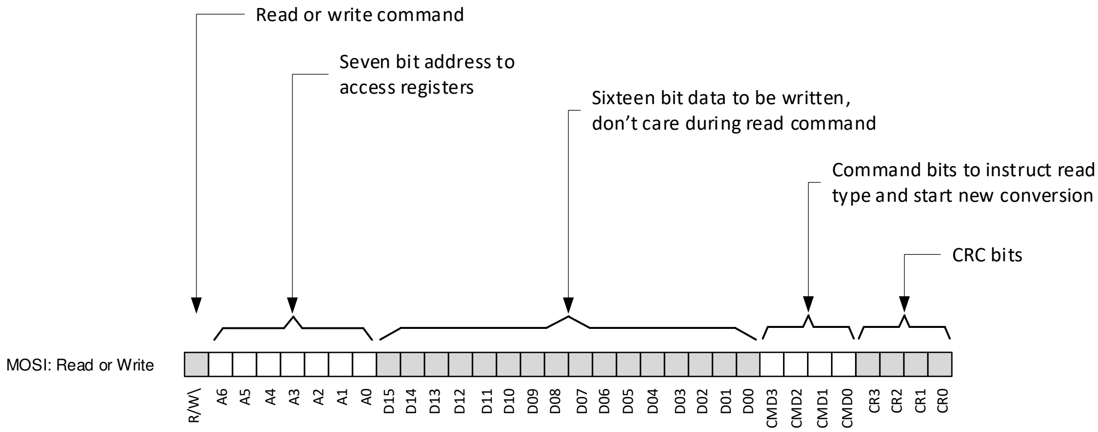
7.5.2.2 $\overline{CS}$

The $\overline{CS}$ activates the SPI interface at the SPI. As long as the $\overline{CS}$ signal is at high level, the TMAG5170-Q1 will not accept the SCLK signal or the Master-Out-Slave-In input (MOSI), and the Master-In-Slave-Out output (MISO) is in high impedance. Hold $\overline{CS}$ low for the duration of a communication frame without toggling to ensure proper communication. The SPI interface is disabled each time $\overline{CS}$ is brought from low to high.

7.5.2.3 MOSI

The 'master out, slave in' (MOSI) line is used by the master to configure the user access registers, start a new conversion, or send a read command. The MOSI bits are transmitted with each SCLK rising edge when the $\overline{CS}$ pin is low. Figure 10 explains the MOSI frame details. There are 4 command bits in the MOSI line to select the status bit for the next frame or start a new conversion.

Programming (continued)



CMD0	CMD0 = 0	No conversion start through command bits
	CMD0 = 1	Start of conversion at the CS going high
CMD1	CMD1 = 0	Display SET_COUNT [2:0] in STAT [2:0] bits at MISO next frame
	CMD1 = 1	Display DATA_TYPE [2:0] in STAT [2:0] bits at MISO next frame

* CMD2 & CMD3 are reserved bits
** SET_COUNT register bits indicate the rolling count of the conversion data set. The counter is reset after 111b.
*** DATA_TYPE register bits indicate the type of data being read through the MISO line

Figure 10. 32-Bit Frame Definition of the MOSI Line

7.5.2.4 MISO

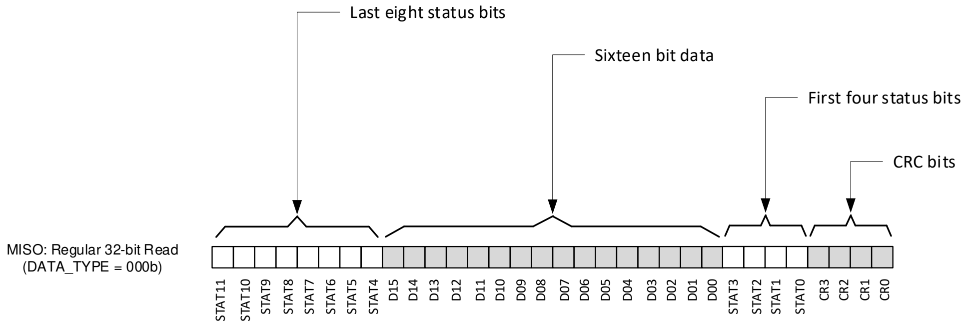
The 'master in, slave out' (MISO) line is used by the master to read the data from the TMAG5170-Q1. The TMAG5170-Q1 will shift out command responses and ADC conversion data serially with each rising SCLK edge when the CS pin is low. This pin assumes a high-impedance state when CS is high. Based off the DATA_TYPE bit setting, the TMAG5170-Q1 supports two different MISO frames:

- *Regular 32-Bit MISO Read*
- *Special 32-Bit MISO Read*

7.5.2.4.1 Regular 32-Bit MISO Read

With DATA_TYPE = 000b, the TMAG5170-Q1 supports a regular 16-bit register read during the 32-bit MISO frame as explained in Figure 11. In this read mode, 12-bit status bits are displayed. All the status bits except for the ERROR_STAT bit are directly read from the status registers. The ERROR_STAT bit indicates if any error bit set in the device. The status bits STAT[2:0] can be changed based off CMD1 value in the previous frame as described in Figure 11.

Programming (continued)



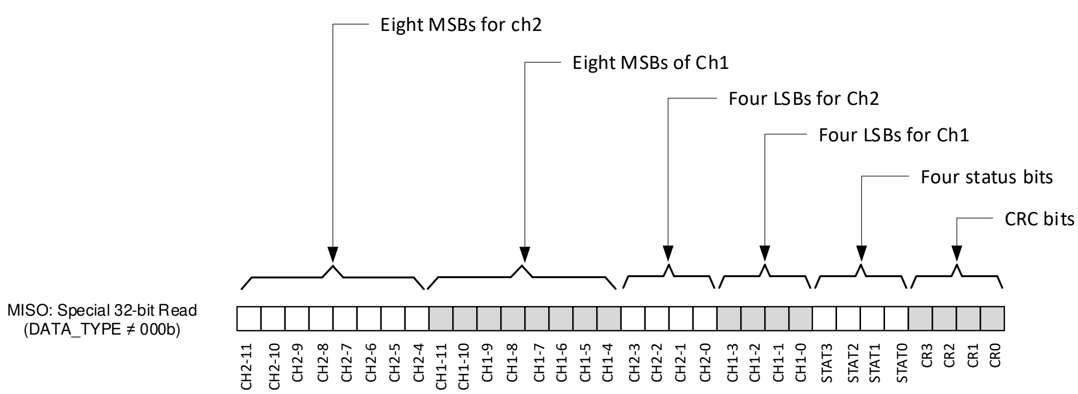
STAT11	STAT10	STAT9	STAT8	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
PREV_CRC_STAT	CFG_RESET	ALRT_STATUS1	ALRT_STATUS0	X	Y	Z	T	ERROR_STAT	Follows CMD1 instruction from previous frame		

* PREV_CRC_STAT indicates if there is any CRC error in the immediate past frame
** ERROR_STAT indicates if there is any error bit flipped in the part
*** STAT10 to STAT4 indicate select status bits from the CONV_STATUS and AFE_STATUS registers

Figure 11. Regular 32-Bit MISO Read

7.5.2.4.2 Special 32-Bit MISO Read

With DATA_TYPE > 000b, the TMAG5170-Q1 supports a special 32-bit MISO frame for two-channel simultaneous data read. Each channel data is limited to 12 bits. This feature is useful for systems requiring faster data throughput while performing multi-axis measurements. Figure 12 explains the detail construction of the special 32-bit MISO frame. When the device is in set to special 32-bit read, it will continue to deliver the 2-channel data set through the MISO line during consecutive read or write cycles. DATA_TYPE bits must be reset to get back to a regular read cycle. Only 4 status bits are transmitted in this mode. All the status bits except for the ERROR_STAT bit are directly read from the status registers. The ERROR_STAT bit indicates if any error bit set in the device. The status bits, STAT[2:0] can be changed based off CMD1 value in the previous frame.



STAT3	STAT2	STAT1	STAT0
ERROR_STAT	Follows CMD1 instruction from previous frame		

* ERROR_STAT indicates if there is any error bit set in the device

Figure 12. Special 32-Bit MISO Read

Programming (continued)

7.5.2.5 SPI CRC

The TMAG5170-Q1 performs mandatory CRC for SPI communication. The Data integrity is maintained in both directions by a 4-bit CRC covering the content of the incoming and outgoing 32-bit messages. The four LSB bits of each 32-bit SPI frame are dedicated for the CRC. The CRC code is generated by the polynomial $x^4 + x + 1$. Initialize the CRC bits with b1111.

During the MOSI write frame, the TMAG5170-Q1 reads for the CRC data before executing a write instruction. The write instruction from the master is ignored if there is any CRC error present in the frame. During the MOSI regular read frame the TMAG5170-Q1 starts to deliver the requested data through MISO line in the same frame, and notify master of any error occurrence through the ERROR_STAT bit. A master can determine the presence of a CRC error in the MOSI frame by checking the Status11 bit in the next regular read frame.

7.5.2.6 SPI Frame

With the flexible definition of the 32-bit frames, the TMAG5170-Q1 supports a wide array of application requirements catering to multiple user-specific data throughout. Two different frame examples are shown in this section to illustrate the complete SPI bus communication:

- *32-Bit Read Frame*
- *32-Bit Write Frame*

7.5.2.6.1 32-Bit Read Frame

Figure 13 shows both regular and special MISO frames during MOSI read command. The TMAG5170-Q1 implements in-frame communication. When master sends a register read command during a regular read cycle, the corresponding 16-bit register data is sent through the MISO line in the same frame. During the special read cycle, the TMAG5170-Q1 ignores the address and data bits of the MOSI line and sends the two channel data set through the MISO line as defined in the DATA_TYPE register bits.

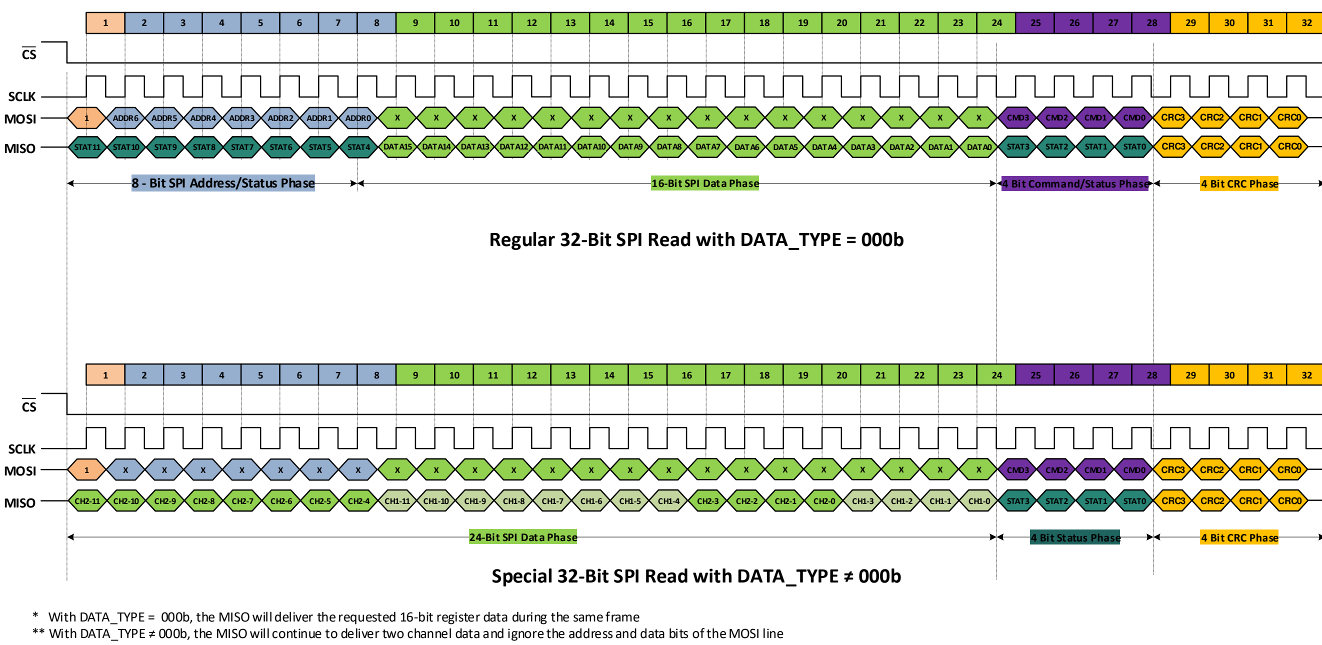
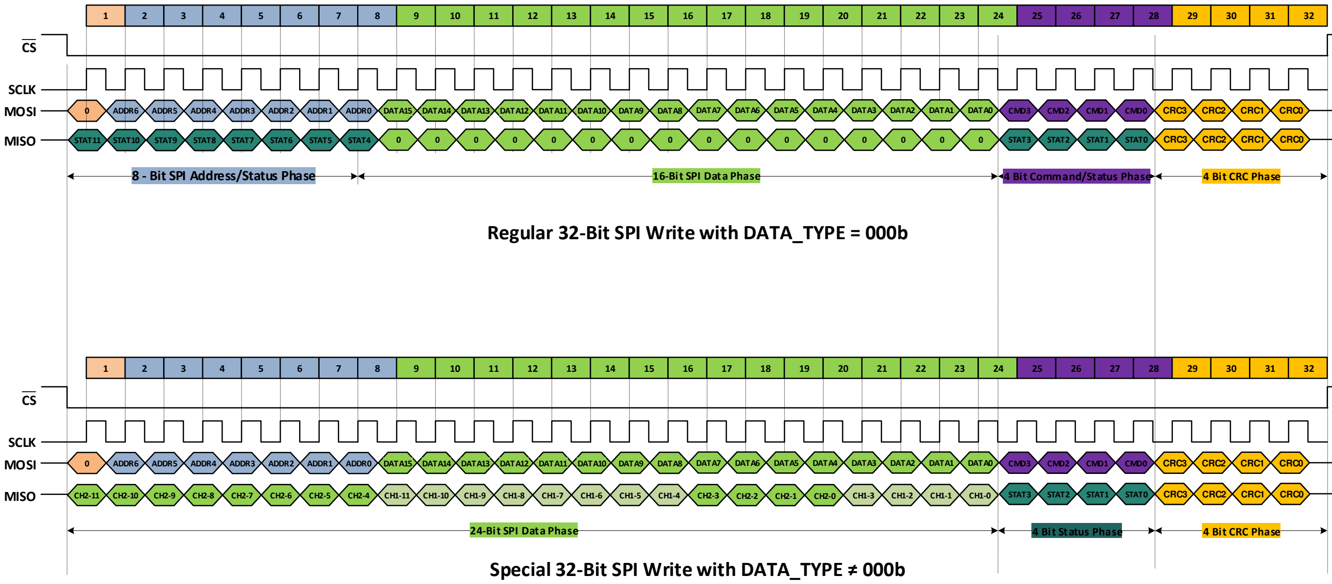


Figure 13. 32-Bit SPI Read

7.5.2.6.2 32-Bit Write Frame

Figure 14 shows both regular and special MISO frames during MOSI write command. During a regular 32-bit frame write command through MOSI, the MISO delivers '0's in place of 16-bit data placeholders. During the special frame write cycle through MOSI line, the TMAG5170-Q1 will continue to send the two channel data through MISO line as defined by the DATA_TYPE register bits.

Programming (continued)



* With DATA_TYPE = 000b, the MISO will deliver '0's in the 16-bit data space during write frame
** With DATA_TYPE ≠ 000b, the MISO will continue to deliver two channel data during either read or write frames.

Figure 14. 32-BIT WRITE FRAME

7.6 Register Map

7.6.1 TMAG5170 Registers

Table 4 lists the TMAG5170 registers. All register offset addresses not listed in Table 4 should be considered as reserved locations and the register contents should not be modified.

Table 4. TMAG5170 Registers

Offset	Acronym	Register Name	Section
0x0	DEVICE_CONFIG	Configure Device Operation Modes	Go
0x1	SENSOR_CONFIG	Configure Device Operation Modes	Go
0x2	SYSTEM_CONFIG	Configure Device Operation Modes	Go
0x3	ALERT_CONFIG	Configure Device Operation Modes	Go
0x4	X_THRX_CONFIG	Configure Device Operation Modes	Go
0x5	Y_THRX_CONFIG	Configure Device Operation Modes	Go
0x6	Z_THRX_CONFIG	Configure Device Operation Modes	Go
0x7	T_THRX_CONFIG	Configure Device Operation Modes	Go
0x8	CONV_STATUS	Conversion Satus Register	Go
0x9	X_CH_RESULT	Conversion Result Register	Go
0xA	Y_CH_RESULT	Conversion Result Register	Go
0xB	Z_CH_RESULT	Conversion Result Register	Go
0xC	TEMP_RESULT	Conversion Result Register	Go
0xD	AFE_STATUS	Safety Check Satus Register	Go
0xE	SYS_STATUS	Safety Check Satus Register	Go
0xF	TEST_CONFIG	Test Configuration Register	Go
0x10	OSC_MONITOR	Conversion Result Register	Go
0x11	MAG_GAIN_CONFIG	Configure Device Operation Modes	Go
0x13	ANGLE_RESULT	Conversion Result Register	Go

Table 4. TMAG5170 Registers (continued)

Offset	Acronym	Register Name	Section
0x14	MAGNITUDE_RESULT	Conversion Result Register	Go

Complex bit access types are encoded to fit into small table cells. Table 5 shows the codes that are used for access types in this section.

Table 5. TMAG5170 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 DEVICE_CONFIG Register (Offset = 0x0) [reset = 0x0]

DEVICE_CONFIG is shown in Table 6.

Return to the Summary Table.

Table 6. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14-12	CONV_AVG	R/W	0x0	Enables additional sampling of the sensor data to reduce the noise effect (or to increase resolution) 0x0 = 1x - 13.33Kbps (3-axes) or 40Kpbs (1 axis) 0x1 = 2x - 6.65Kbps (3-axes) or 20Kpbs (1 axis) 0x2 = 4x - 3.33Kbps (3-axes) or 10Kpbs (1 axis) 0x3 = 8x - 1.66Kbps (3-axes) or 5Kpbs (1 axis) 0x4 = 16x - 0.833Kbps (3-axes) or 2.5Kpbs (1 axis) 0x5 = 32x - 0.417Kbps (3-axes) or 1.25Kpbs (1 axis) 0x6 = Code not used, defaults to 000b if selected 0x7 = Code not used, defaults to000b if selected
11-10	RESERVED	R	0x0	Reserved
9-8	MAG_TEMPCO	R/W	0x0	Temperature Coefficient of Sense Magnet 0x0 = 0% (Current sensor applications) 0x1 = 0.12%/°C (NdBFe) 0x2 = Reserved 0x3 = 0.2%/°C (Ceramic)
7	RESERVED	R	0x0	Reserved

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Table 6. DEVICE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	OPERATING_MODE	R/W	0x0	Selects Operating Mode 0x0 = Configuration mode, DEFAULT (TRIGGER_MODE Active) 0x1 = Stand-by mode (TRIGGER_MODE Active) 0x2 = Active Measure mode (Continuous conversion) 0x3 = Active Trigger Mode (TRIGGER_MODE Active) 0x4 = Wake-up and Sleep mode (duty-cycled mode) 0x5 = Sleep mode 0x6 = Deep sleep mode (wakes up at CS signal from Master) 0x7 = Code not used, defaults to 000b if selected
3	T_CH_EN	R/W	0x0	Enables data acquisition of the temperature channel 0x0 = Temp channel disabled, DEFAULT 0x1 = Temp channel enabled
2	T_RATE	R/W	0x0	Temperature Conversion Rate. It is linked to the CONV_AVG field 0x0 = Same as other sensors per CONV_AVG, DEFAULT 0x1 = Once per conversion set
1	T_HLT_EN	R/W	0x0	Enables temperature limit check 0x0 = Temperature limit check off, DEFAULT 0x1 = Temperature limit check on
0	TEMP_COMP_EN	R/W	0x0	Enables device on-chip temp sensor to improve linearization of magnetic sensor output: 1) device takes one temp conversion data with each wake-up cycle during wake-up and sleep mode 2) Device takes one temp conversion data during each conversion set 0x0 = Temp compensation not enabled (default) 0x1 = Temp compensation enabled

7.6.1.2 SENSOR_CONFIG Register (Offset = 0x1) [reset = 0x0]

SENSOR_CONFIG is shown in Table 7.

Return to the Summary Table.

Table 7. SENSOR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	ANGLE_EN	R/W	0x0	Enable Angle calculation using two axis data 0x0 = No angle calculation (default) 0x1 = X-Y-angle calculation enabled 0x2 = Y-Z-angle calculation enabled 0x3 = Z-X-angle calculation enabled

Table 7. SENSOR_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-10	SLEEPTIME	R/W	0x0	Selects the time spent in low power mode between conversions when OPERATING_MODE =010b 0x0 = 1ms 0x1 = 5ms 0x2 = 10ms 0x3 = 15ms 0x4 = 20ms 0x5 = 30ms 0x6 = 50ms 0x7 = 100ms 0x8 = 500ms 0x9 = 1000ms 0xA = Code not used, defaults to 0000b if selected 0xB = Code not used, defaults to 0000b if selected 0xC = Code not used, defaults to 0000b if selected 0xD = Code not used, defaults to 0000b if selected 0xE = Code not used, defaults to 0000b if selected 0xF = Code not used, defaults to 0000b if selected
9-6	MAG_CH_EN	R/W	0x0	Enables data acquisition of the magnetic axis channel(s) 0x0 = All magnetic channels of OFF, DEFAUT 0x1 = X channel enabled 0x2 = Y channel enabled 0x3 = X, Y channel enabled 0x4 = Z channel enabled 0x5 = Z, X channel enabled 0x6 = Y, Z channel enabled 0x7 = X, Y, Z channel enabled 0x8 = XYX channel enabled 0x9 = YXY channel enabled 0xA = YZY channel enabled 0xB = ZYZ channel enabled 0xC = ZXZ channel enabled 0xD = XZX channel enabled 0xE = XYZYX channel enabled 0xF = XYZZYX channel enabled
5-4	Z_RANGE	R/W	0x0	Enables different magnetic ranges to support magnetic fields from ±25mT to ±300mT 0x0 = ±50mT (TMAG5170A1) / ±200mT(TMAG5170A2), DEFAULT 0x1 = ±25mT (TMAG5170A1) / ±133mT(TMAG5170A2) 0x2 = ±100mT (TMAG5170A1) / ±300mT(TMAG5170A2) 0x3 = Code not used, defaults to 00b if selected

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Table 7. SENSOR_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	Y_RANGE	R/W	0x0	Enables different magnetic ranges to support magnetic fields from ±25mT to ±300mT 0x0 = ±50mT (TMAG5170A1) / ±200mT(TMAG5170A2), DEFAULT 0x1 = ±25mT (TMAG5170A1) / ±133mT(TMAG5170A2) 0x2 = ±100mT (TMAG5170A1) / ±300mT(TMAG5170A2) 0x3 = Code not used, defaults to 00b if selected
1-0	X_RANGE	R/W	0x0	Enables different magnetic ranges to support magnetic fields from ±25mT to ±300mT 0x0 = ±50mT (TMAG5170A1) / ±200mT(TMAG5170A2), DEFAULT 0x1 = ±25mT (TMAG5170A1) / ±150mT(TMAG5170A2) 0x2 = ±100mT (TMAG5170A1) / ±300mT(TMAG5170A2) 0x3 = Code not used, defaults to 00b if selected

7.6.1.3 SYSTEM_CONFIG Register (Offset = 0x2) [reset = 0x0]

SYSTEM_CONFIG is shown in Table 8.

Return to the Summary Table.

Table 8. SYSTEM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-12	DIAG_SEL	R/W	0x0	Selects a safety diagnostic mode run 0x0 = Run all data path diagnostics all together -DEFAULT 0x1 = Run only enabled data path diagnostics all together 0x2 = Run all data path diagnostics in sequence 0x3 = Run only enabled data path diagnostics in sequence
11	RESERVED	R	0x0	Reserved
10-9	TRIGGER_MODE	R/W	0x0	Selects a condition which initiates a single conversion based off already configured registers. A running conversion completes before executing a trigger. Redundant triggers are ignored. TRIGGER_MODE is available only during the modes explicitly mentioned in OPERATING_MODE. 0x0 = Conversion Start at SPI Command Bits, DEFAULT 0x1 = nCS Sync Pulse 0x2 = ALERT Sync Pulse 0x3 = Code not used, defaults to 00b if selected
8-6	DATA_TYPE	R/W	0x0	Data Type to be accessed from results registers via SPI 0x0 = Default 32-bit Register Access 0x1 = 12-Bit XY Data Access 0x2 = 12-Bit XZ Data Access 0x3 = 12-Bit ZY Data Access 0x4 = 12-Bit XT Data Access 0x5 = 12-Bit YT Data Access 0x6 = 12-Bit ZT Data Access 0x7 = 12-Bit AM Data Access

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Table 8. SYSTEM_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DIAG_EN	R/W	0x0	Enables AFE Diagnostic Tests to be executed with respect to the diagnostics enabled in DEVICE_CFG and the settings of the B-Field and Temperature Conversions 0x0 = Execution of AFE Diagnostics is disabled, DEFAULT 0x1 = Execution of the diagnostics selected in DEVICE_CFG
4-3	RESERVED	R	0x0	Reserved
2	Z_HLT_EN	R/W	0x0	Enables magnetic field limit check on Z axis 0x0 = Z axis limit check off, DEFAULT 0x1 = Z axis limit check on
1	Y_HLT_EN	R/W	0x0	Enables magnetic field limit check on Y axis 0x0 = Y axis limit check off, DEFAULT 0x1 = Y axis limit check on
0	X_HLT_EN	R/W	0x0	Enables magnetic field limit check on X axis 0x0 = X axis limit check off, DEFAULT 0x1 = X axis limit check on

7.6.1.4 ALERT_CONFIG Register (Offset = 0x3) [reset = 0x0]

ALERT_CONFIG is shown in Table 9.

Return to the Summary Table.

Table 9. ALERT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	ALERT_LATCH	R/W	0x0	Latched ALERT Mode Select 0x0 = ALERT sources are not latched. ALERT is asserted only while the source of the ALERT response is present 0x1 = ALERT sources are latched. ALERT response is latched when the source of the ALERT is asserted until cleared on Read of the corresponding status register (AFE_STATUS, SYS_STATUS, or result registers)
12	ALERT_MODE	R/W	0x0	ALERT Mode Select 0x0 = Interrupt Mode 0x1 = Comparator Mode. This mode overrides any interrupt function (ALERT trigger is also disabled), and implements Hall switch function based off the *_THRX_ALRT settings.
11	STATUS_ALRT	R/W	0x0	Enable ALERT response when any flag in the AFE_STATUS or SYS_STATUS registers are set 0x0 = ALERT is not asserted when any of the AFE_STATUS or SYS_STATUS bit is set 0x1 = ALERT output is asserted when any of the AFE_STATUS or SYS_STATUS bit is set
10-9	RESERVED	R	0x0	Reserved

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Table 9. ALERT_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RSLT_ALRT	R/W	0x0	Enable ALERT response when the configured set of conversions is complete 0x0 = ALERT is not used to signal when the configured set of conversions are complete 0x1 = ALERT output is asserted when the configured set of conversions are complete
7-6	RESERVED	R	0x0	Reserved
5-4	THRX_COUNT	R/W	0x0	Number of conversions above the HIGH Threshold or below the LOW Threshold before the ALERT Response is initiated 0x0 = 1-Conversion Result 0x1 = 2-Conversion Results 0x2 = 3-Conversion Results 0x3 = 4-Conversion Results
3	T_THRX_ALRT	R/W	0x0	Temperature Threshold ALERT Enable 0x0 = ALERT is not used to signal when Temperature Thresholds are Crossed 0x1 = ALERT output is asserted when Temperature Thresholds are Crossed
2	Z_THRX_ALRT	R/W	0x0	Z-Channel Threshold ALERT Enable 0x0 = ALERT is not used to signal when Z-Axis Magnetic Thresholds are Crossed 0x1 = ALERT output is asserted when Z-Axis Magnetic Thresholds are Crossed
1	Y_THRX_ALRT	R/W	0x0	Y-Channel Threshold ALERT Enable 0x0 = ALERT is not used to signal when Y-Axis Magnetic Thresholds are Crossed 0x1 = ALERT output is asserted when Y-Axis Magnetic Thresholds are Crossed
0	X_THRX_ALRT	R/W	0x0	X-Channel Threshold ALERT Enable 0x0 = ALERT is not used to signal when X-Axis Magnetic Thresholds are Crossed 0x1 = ALERT output is asserted when X-Axis Magnetic Thresholds are Crossed

7.6.1.5 X_THRX_CONFIG Register (Offset = 0x4) [reset = 0x7D83]

X_THRX_CONFIG is shown in Table 10.

Return to the Summary Table.

Table 10. X_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X_HI_THRESHOLD	R/W	0x7D	X-Axis Maximum Magnetic Field Threshold as defined as: ±(X_RANGE/128)*X_HI_THRESHOLD. Default to 98% of the full-scale
7-0	X_LO_THRESHOLD	R/W	0x83	X-Axis Minimum Magnetic Field Threshold is defined as: ±(X_RANGE/128)*X_LO_THRESHOLD. Default to -98% of the full-scale

7.6.1.6 Y_THRX_CONFIG Register (Offset = 0x5) [reset = 0x7D83]

Y_THRX_CONFIG is shown in Table 11.

Return to the Summary Table.

Table 11. Y_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Y_HI_THRESHOLD	R/W	0x7D	Y-Axis Maximum Magnetic Field Threshold is defined as: ±(Y_RANGE/128)*Y_HI_THRESHOLD. Default to 98% of the full-scale.
7-0	Y_LO_THRESHOLD	R/W	0x83	Y-Axis Minimum Magnetic Field Threshold is defined as: ±(Y_RANGE/128)*Y_LO_THRESHOLD. Default to -98% of the full-scale.

7.6.1.7 Z_THRX_CONFIG Register (Offset = 0x6) [reset = 0x7D83]

Z_THRX_CONFIG is shown in Table 12.

Return to the Summary Table.

Table 12. Z_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Z_HI_THRESHOLD	R/W	0x7D	Z-Axis Maximum Magnetic Field Threshold is defined as: ±(Z_RANGE/128)*Z_HI_THRESHOLD. Default to 98% of the full-scale
7-0	Z_LO_THRESHOLD	R/W	0x83	Z-Axis Minimum Magnetic Field Threshold is defined as: ±(Z_RANGE/128)*X_LO_THRESHOLD. Default to -98% of the full-scale

7.6.1.8 T_THRX_CONFIG Register (Offset = 0x7) [reset = 0x6732]

T_THRX_CONFIG is shown in Table 13.

Return to the Summary Table.

Table 13. T_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	T_HI_THRESHOLD	R/W	0x67	TEMP Maximum Threshold is defined as: ±(170/128)*T_HI_THRESHOLD. Default to 170C
7-0	T_LO_THRESHOLD	R/W	0x32	TEMP Minimum Threshold is defined as: ±(170/128)*T_LO_THRESHOLD. Default to -40C

7.6.1.9 CONV_STATUS Register (Offset = 0x8) [reset = 0x0]

CONV_STATUS is shown in Table 14.

Return to the Summary Table.

Table 14. CONV_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	RDY	R	0x0	Conversion Data Buffer is Ready to be Read 0x0 = Conversion Data Buffer Valid 0x1 = Conversion Data Buffer Not Valid

Table 14. CONV_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	A	R	0x0	Angle/Magnitude Data from Current Conversion 0x0 = Data is not Current 0x1 = Data is Current
11	T	R	0x0	Temperature Data from Current Conversion 0x0 = Temperature Data is not Current 0x1 = Temperature Data is Current
10	Z	R	0x0	Z-Channel Data from Current Conversion 0x0 = Z-Channel Data is not Current 0x1 = Z-Channel Data is Current
9	Y	R	0x0	Y-Channel Data from Current Conversion 0x0 = Y-Channel Data is not Current 0x1 = Y-Channel Data is Current
8	X	R	0x0	X-Channel Data from Current Conversion 0x0 = X-Channel Data is not Current 0x1 = X-Channel Data is Current
7	RESERVED	R	0x0	Reserved
6-4	SET_COUNT	R	0x0	Rolling Count of Conversion Data Sets
3-2	RESERVED	R	0x0	Reserved
1-0	ALRT_STATUS	R	0x0	State of ALERT Response 0x0 = No ALERT Conditions 0x1 = AFE Status Flag Set 0x2 = SYS Status Flag Set 0x3 = Flags Set in both AFE and SYS Status Registers

7.6.1.10 X_CH_RESULT Register (Offset = 0x9) [reset = 0x0]

X_CH_RESULT is shown in Table 15.

Return to the Summary Table.

Table 15. X_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	X_CH_RESULT	R	0x0	X-Channel Data Conversion Results

7.6.1.11 Y_CH_RESULT Register (Offset = 0xA) [reset = 0x0]

Y_CH_RESULT is shown in Table 16.

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Table 16. Y_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Y_CH_RESULT	R	0x0	Y-Channel Data Conversion Results

7.6.1.12 Z_CH_RESULT Register (Offset = 0xB) [reset = 0x0]

Z_CH_RESULT is shown in Table 17.

Return to the Summary Table.

Table 17. Z_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Z_CH_RESULT	R	0x0	Z-Channel Data Conversion Results

7.6.1.13 TEMP_RESULT Register (Offset = 0xC) [reset = 0x0]

TEMP_RESULT is shown in Table 18.

Return to the Summary Table.

Table 18. TEMP_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEMP_RESULT	R	0x0	Temperature Sensor Data Conversion Results

7.6.1.14 AFE_STATUS Register (Offset = 0xD) [reset = 0x8000]

AFE_STATUS is shown in Table 19.

Return to the Summary Table.

Table 19. AFE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CFG_RESET	RC	0x1	Device Power up Status. This bit is reset when microcontroller reads the AFE_STATUS register. 0x0 = DEVICE_RESET has been acknowledged and cleared 0x1 = Device has experienced a hardware reset after a power down or brown-out
14-13	RESERVED	R	0x0	Reserved
12	SENS_STAT	RC	0x0	Analog Front End Sensor Diagnostic Status 0x0 = No Error Detected 0x1 = Analog Front End Sensor Diagnostic Test Failed
11	TEMP_STAT	RC	0x0	Temperature Sensor Diagnostic Status 0x0 = No Error Detected 0x1 = Analog Front End Temperature Sensor Diagnostic Test Failed
10	ZHS_STAT	RC	0x0	Z-Axis Hall Sensor Diagnostic Status 0x0 = No Error Detected 0x1 = Z-Axis Hall Sensor Diagnostic Test Failed
9	YHS_STAT	RC	0x0	Y-Axis Hall Sensor Diagnostic Status 0x0 = No Error Detected 0x1 = Y-Axis Hall Sensor Diagnostic Test Failed
8	XHS_STAT	RC	0x0	X-Axis Hall Sensor Diagnostic Status 0x0 = No Error Detected 0x1 = X-Axis Hall Sensor Diagnostic Test Failed
7-2	RESERVED	R	0x0	Reserved

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Table 19. AFE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TRIM_STAT	RC	0x0	Trim Data Error 0x0 = No Trim Data Errors were detected 0x1 = Trim Data Error was detected
0	LDO_STAT	RC	0x0	LDO Error 0x0 = No faults in the internal LDO supplied power were detected 0x1 = A fault in the internal LDO supplied power was detected

7.6.1.15 SYS_STATUS Register (Offset = 0xE) [reset = 0x0]

SYS_STATUS is shown in Table 20.

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Table 20. SYS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALRT_LVL	RC	0x0	Reflects the current state of the ALERT Pin Feed-Back path 0x0 = The input ALERT Logic Level is Low 0x1 = The input ALERT Logic Level is High
14	ALRT_DRV	RC	0x0	Each time the open drain ALERT signal is driven, the feedback circuit checks if the ALERT output goes Low. An error flag is generated at the ALRT_DRV bit if the output doesn't go Low. 0x0 = No ALERT Drive Error Detected 0x1 = ALERT Drive Error Detected
13	MISO_DRV	RC	0x0	The Logic value driven output on MISO was not the value of the MISO Pin Feed-back path when MISO is being driven by the device 0x0 = No MISO Drive Error Detected 0x1 = MISO Drive Error Detected
12	CRC_STAT	RC	0x0	Cyclic Redundancy Check Error 0x0 = No Cyclic Redundancy Check Error was Detected 0x1 = Cyclic Redundancy Check Error was Detected for a SPI transaction
11	FRAME_STAT	RC	0x0	Incorrect number of clocks in SPI frame 0x0 = No Frame Error was Detected 0x1 = Incorrect number of clocks detected for a SPI transaction
10-8	OPERATING_STAT	R	0x0	Reports the status of Operating Mode 0x0 = Config state 0x1 = Standby state 0x2 = Active Measure (Continuous Mode) state 0x3 = - Active Triggered Mode state 0x4 = DCM Active State 0x5 = DCM Sleep State 0x6 = Sleep State
7-6	RESERVED	R	0x0	Reserved
5	VCC_OV	RC	0x0	VCC Over-Voltage Detection in Active or Stand-by mode 0x0 = No Over-Voltage Detected on VCC 0x1 = VCC was detected to be over-voltage

Table 20. SYS_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	VCC_UV	RC	0x0	VCC Under Voltage Detection in Active or Stand-by mode 0x0 = No Under-Voltage was Detected on VCC 0x1 = VCC was detected to be under-voltage
3	TEMP_THX	RC	0x0	Temperature Threshold Crossing Detected 0x0 = No Temperature Threshold Crossing Detected 0x1 = Temperature Threshold Crossing Detected
2	ZCH_THX	RC	0x0	Z-Channel Threshold Crossing Detected 0x0 = No Z-Axis Magnetic Field Threshold Crossing Detected 0x1 = Z-Axis Magnetic Field Threshold Threshold Crossing Detected
1	YCH_THX	RC	0x0	Y-Channel Threshold Crossing Detected 0x0 = No Y-Axis Magnetic Field Threshold Crossing Detected 0x1 = Y-Axis Magnetic Field Threshold Crossing Detected
0	XCH_THX	RC	0x0	X-Channel Threshold Crossing Detected 0x0 = No X-Axis Magnetic Feild Threshold Crossing Detected 0x1 = X-Axis Magnetic Feild Threshold Crossing Detected

7.6.1.16 TEST_CONFIG Register (Offset = 0xF) [reset = 0x0]

TEST_CONFIG is shown in Table 21.

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Table 21. TEST_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0x0	Reserved
5-4	VER	R	0x0	Indicates the version of the device 0x0 = A1 Rev (Default) 0x1 = A2 0x2 = reserved 0x3 = reserved
3	RESERVED	R	0x0	Reserved
2	CRC_DIS	R/W	0x0	Enables CRC to be included in SPI Protocol 0x0 = CRC Enabled SPI Portocol (Default) 0x1 = CRC Disabled in SPI Protocol
1-0	OSC_CNT_CTL	R/W	0x0	Oscillator Count Control - Starts, Stops, and Resets the counter driven by the HFOSC or LFOSC oscillator to facilitate oscillator frequency and integety checks 0x0 = Reset Counters (default) 0x1 = Start Osc Counter driven by HFOSC 0x2 = Start Osc Counter driven by LFOSC 0x3 = Stop Counter

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7.6.1.17 OSC_MONITOR Register (Offset = 0x10) [reset = 0x0]

OSC_MONITOR is shown in Table 22.

Return to the Summary Table.

Table 22. OSC_MONITOR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	OSC_COUNT	R	0x0	Oscillator Counter. The number of selected oscillator clock cycles that have been counted since Oscillator Counter was started. The HFOSC and LFOSC clock roll-over the 16-bit counter once reaching the max value.

7.6.1.18 MAG_GAIN_CONFIG Register (Offset = 0x11) [reset = 0x0]

MAG_GAIN_CONFIG is shown in Table 23.

Return to the Summary Table.

Table 23. MAG_GAIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	GAIN_SELECTION	R/W	0x0	Enables the selection of a particular Hall axis for amplitude correction to get accurate angle measurement 0x0 = No axis is selected (default) 0x1 = X-axis is selected 0x2 = Y-axis is selected 0x3 = Z-axis is selected
13-11	RESERVED	R	0x0	Reserved
10-0	GAIN_VALUE	R/W	0x0	11-bit gain value determined by Master to adjust the a particular Hall axis value. The gain value is anywhere between 0 and 1. Gain is calculated as 'user entered value/1024'.

7.6.1.19 ANGLE_RESULT Register (Offset = 0x13) [reset = 0x0]

ANGLE_RESULT is shown in Table 24.

Return to the Summary Table.

Table 24. ANGLE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ANGLE_RESULT	R	0x0	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

7.6.1.20 MAGNITUDE_RESULT Register (Offset = 0x14) [reset = 0x0]

MAGNITUDE_RESULT is shown in Table 25.

Return to the Summary Table.

Table 25. MAGNITUDE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MAGNITUDE_RESULT	R	0x0	Resultant vector magnitude (during angle measurement) result. This value should be constant during 360 degree measurements

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Selecting the Sensitivity Option

Select the highest TMAG5170-Q1 sensitivity option that can measure the required range of magnetic flux density so that the ADC output range is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations under the DRV5055 product folder on ti.com.

8.1.2 Temperature Compensation for Magnets

The TMAG5170-Q1 temperature compensation is designed to directly compensate the average temperature drift of several magnets as specified in the MAG_TEMPCO register bits. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite magnets as the temperature increases. Set the MAG_TEMPCO bit to default 00b if the device temperature compensation is not needed.

8.1.3 Sensor Conversion

Multiple conversion schemes can be adopted based off the MAG_CH_EN, CONV_AVG, DIAG_SEL, and DIAG_EN register bits setting.

8.1.3.1 Continuous Conversion

The TMAG5170-Q1 can be set in continuous conversion mode when OPERATING_MODE is set to 010b. An example of continuous conversion is shown Figure 15 where only X-axis is selected for conversion. The input magnetic field is processed in two steps. In the first step the device spins the hall sensor elements, and integrates the sampled data. In the second step the ADC block coverts the analog signal into digital bits and stores in the corresponding result register. While the ADC starts processing the first magnetic sample, the spin block can start processing the second magnetic sample. In this mode, the maximum sampling rate is determined by the update interval, not by the conversion time.

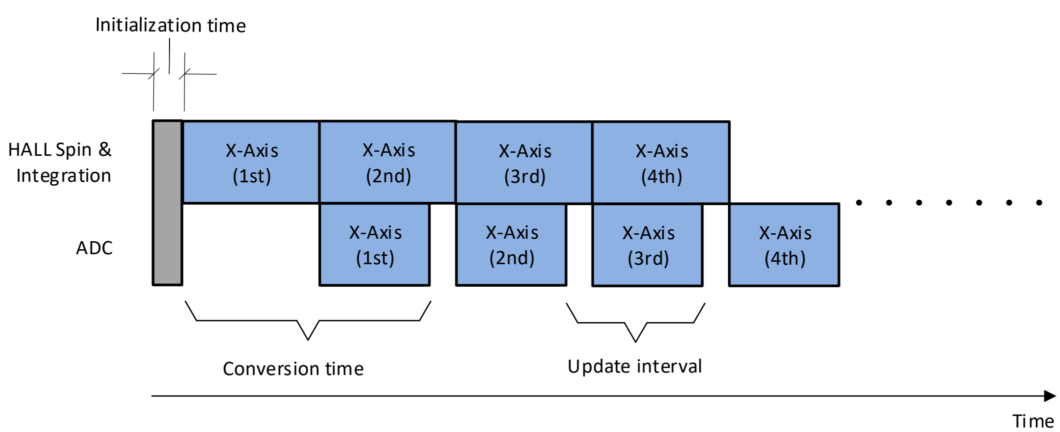

Figure 15. Continuous Conversion selecting X Axis

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Application Information (continued)

8.1.3.2 Trigger Conversion

The TMAG5170-Q1 supports trigger conversion with OPERATING_MODE set to 00b, 001b, or 011b. During trigger conversion, the initialization time can vary depending on the operating mode as shown in Table 3. The trigger event can be initiated through SPI command, ALERT, or CS signal. Figure 16 shows an example of trigger conversion with X, Y, Z, and temperature sensors activated.

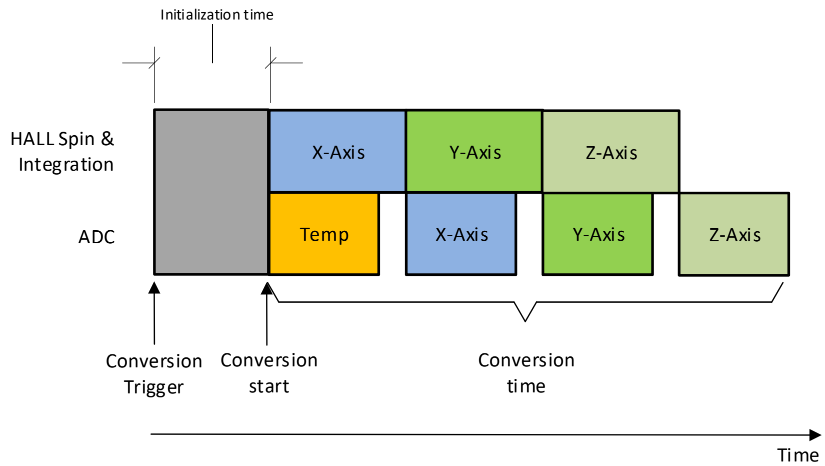

Figure 16. Trigger Conversion for X, Y, Z, & Temperature Sensors

8.1.3.3 Pseudo-Simultaneous Sampling

In absolute angle measurement, application sensor data from multiple axes are required to calculate an accurate angle. The magnetic field data collected at different times through the same signal chain introduces error in angle calculation. The TMAG5170-Q1 offers pseudo-simultaneous sampling data collection modes to eliminate this error. Figure 17 shows an example where MAG_CH_EN is set at 1101b to collect XZX data. The time stamps for X and Z sensor data are the same as shown in Equation 8.

$$t_Z = \frac{t_{X1} + t_{X2}}{2} \quad (8)$$

where

- t_{X1}, t_Z, t_{X2} are time stamps for X, Z, X sensor data completion as defined in Figure 17.

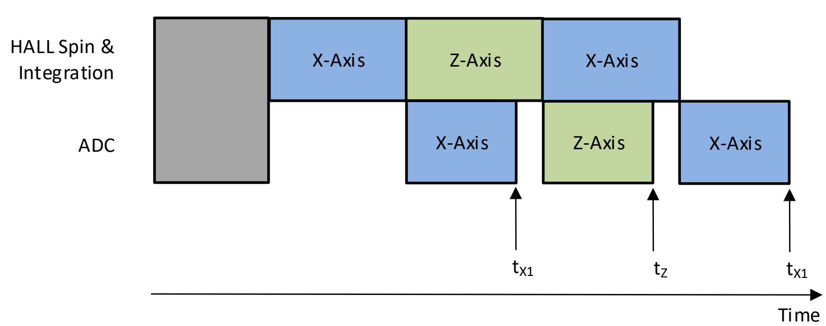

Figure 17. XZX Magnetic Field Conversion

The vertical X, Y sensors of the TMAG5170-Q1 exhibit more noise than the horizontal Z sensor. The pseudo-simultaneous sampling can be used to equalize the noise floor when two set of vertical sensor data are collected against one set of horizontal sensor data, as in examples of XZX or YZY modes.

8.2 Do's and Don'ts

The TMAG5170-Q1 updates the result registers at the end of a conversion. SPI read of the result register needs to be synchronized with the conversion update time to avoid reading a result data while the result register is being updated. The conversion update time, $t_{measure}$ is defined in the electrical characteristics table. Figure 18 shows examples of correct and incorrect SPI timings for a single axis conversion. For applications with tight timing budget use the $\overline{ALERT}$ signal to notify the master when a conversion is complete.

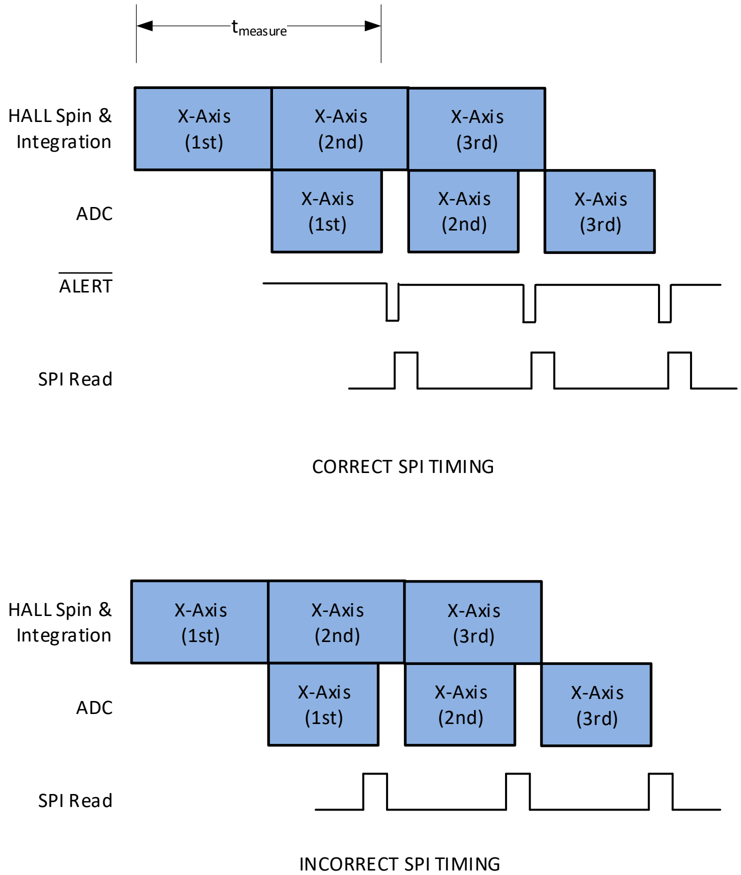

Figure 18. SPI Read Timing During Conversion

8.3 Typical Application

Magnetic angle sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5170-Q1 offers an on-chip angle calculator providing angular measurement based off any two of the magnetic axes. The two axes of interest can be selected in the ANGLE_EN register bits. The device offers angle output in complete 360 degree scale. Take several error sources into account for angle calculation, including sensitivity error, offset error, linearity error, noise, mechanical vibration, temperature drift, and so forth.

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Typical Application (continued)

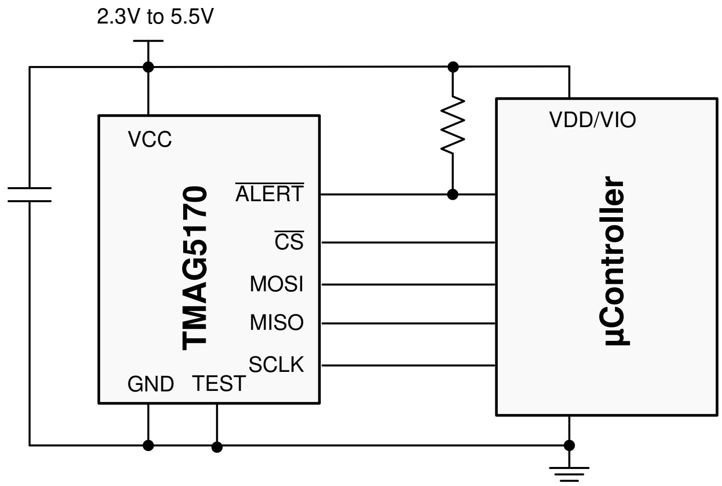

Figure 19. TMAG5170-Q1 Application Diagram

8.3.1 Design Requirements

Use the parameters listed in Table 26 for this design example

Table 26. Design Parameters

DESIGN PARAMETERS	ON-AXIS MEASUREMENT	OFF-AXIS MEASUREMENT
Device	TMAG5170-A1	TMAG5170-A1
VCC	5 V	5 V
Magnet	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480
Magnetic Range Selection	Select the same range for both axes based off the highest possible magnetic field seen by the sensor	Select the same range for both axes based off the highest possible magnetic field seen by the sensor
RPM	<600	<600
Desired Accuracy	<1 °C for 360° rotation	<1 C for 360° rotation

8.3.1.1 Gain Adjustment for Angle Measurement

Common measurement topology include angular position measurements in on-axis or off-axis angular measurements shown in Figure 20. Select the on-axis measurement topology whenever possible as this offers the best optimization of magnetic field and the device measurement ranges. The TMAG5170-Q1 offers on-chip gain adjustment option to account for mechanical position misalignments.

ADVANCE INFORMATION

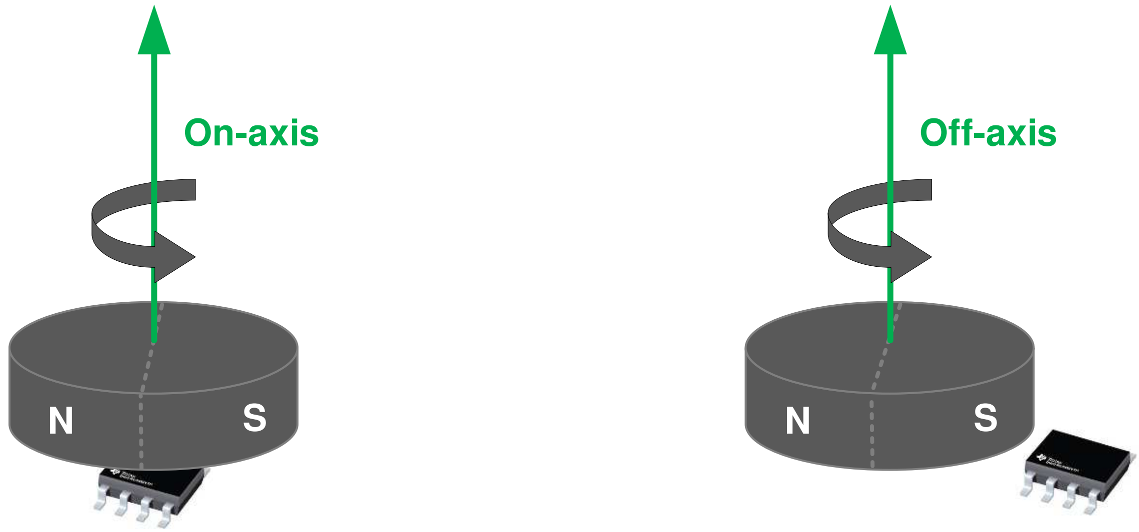

Figure 20. On-Axis vs Off-Axis Angle Measurements

8.3.2 Detailed Design Procedure

For accurate angle measurement, the two axes amplitudes must be normalized by selecting the proper gain adjustment value in the MAG_GAN_CONFIG register. The gain adjustment value is a fractional decimal number between 0 and 1. The following steps must be followed to calculate this fractional value:

- Set the device at 32x average mode and rotate the shaft full 360 degree.
- Record the two axes sensor ADC codes for the full 360 degree rotation.
- Measure the maximum peak-peak ADC code delta for each axis, Ax and Ay as shown in Figure 21 or Figure 22.
- Calculate the gain adjustment value for X axis: $G_X = \frac{A_Y}{A_X}$
- If G_X>1 apply the gain adjustment value to Y axis: $G_Y = \frac{1}{G_X}$
- The target binary gain setting at the GAIN_VALUE register bits are calculated from the equation, G_X or G_Y = $GAIN\_VALUE_{decimal}$/ 1024.

Example 1: If A_X = A_Y = 60,000, the GAIN_SELECTION resister bits can be set as 00b. The GAIN_VALUE register bits are don't care bits in this case.

Example 2: If A_X= 60,000, A_Y = 45,000, the G_X = 45,000/60,000 =0.75. Select 01b for the GAIN_SELECTION register bits.

Example 3: If A_X= 45,000, A_Y = 60,000, the G_X = (60,000/45,000) =1.33. Since G_X >1, the gain adjustment needs to be applied to Y axis with G_Y =1/G_X. Select 10b for the GAIN_SELECTION register bits.

ADVANCE INFORMATION

8.3.3 Application Curves

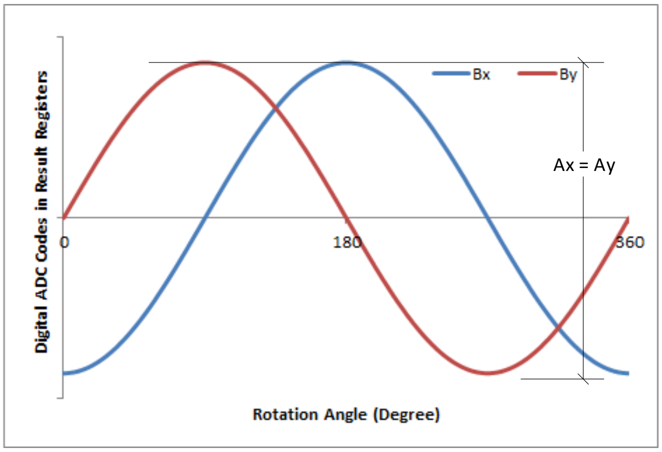

Figure 21. X and Y Sensor Data for Full 360 Degree Rotation for On-Axis Measurement

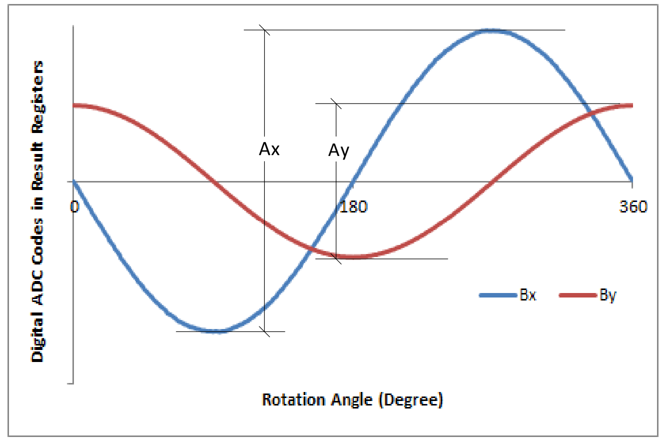

Figure 22. X and Y Sensor Data for Full 360 Degree Rotation for Off-Axis Measurement

9 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 µF. Connect the TEST pin to ground.

10 Layout

10.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed-circuit boards (PCBs), which makes placing the magnet on the opposite side of the PCB possible.

10.2 Layout Example

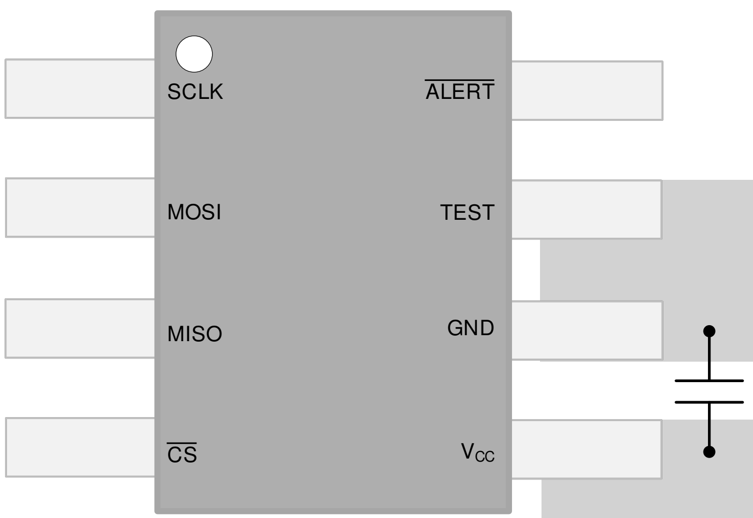

Figure 23. Layout Example With TMAG5170-Q1

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

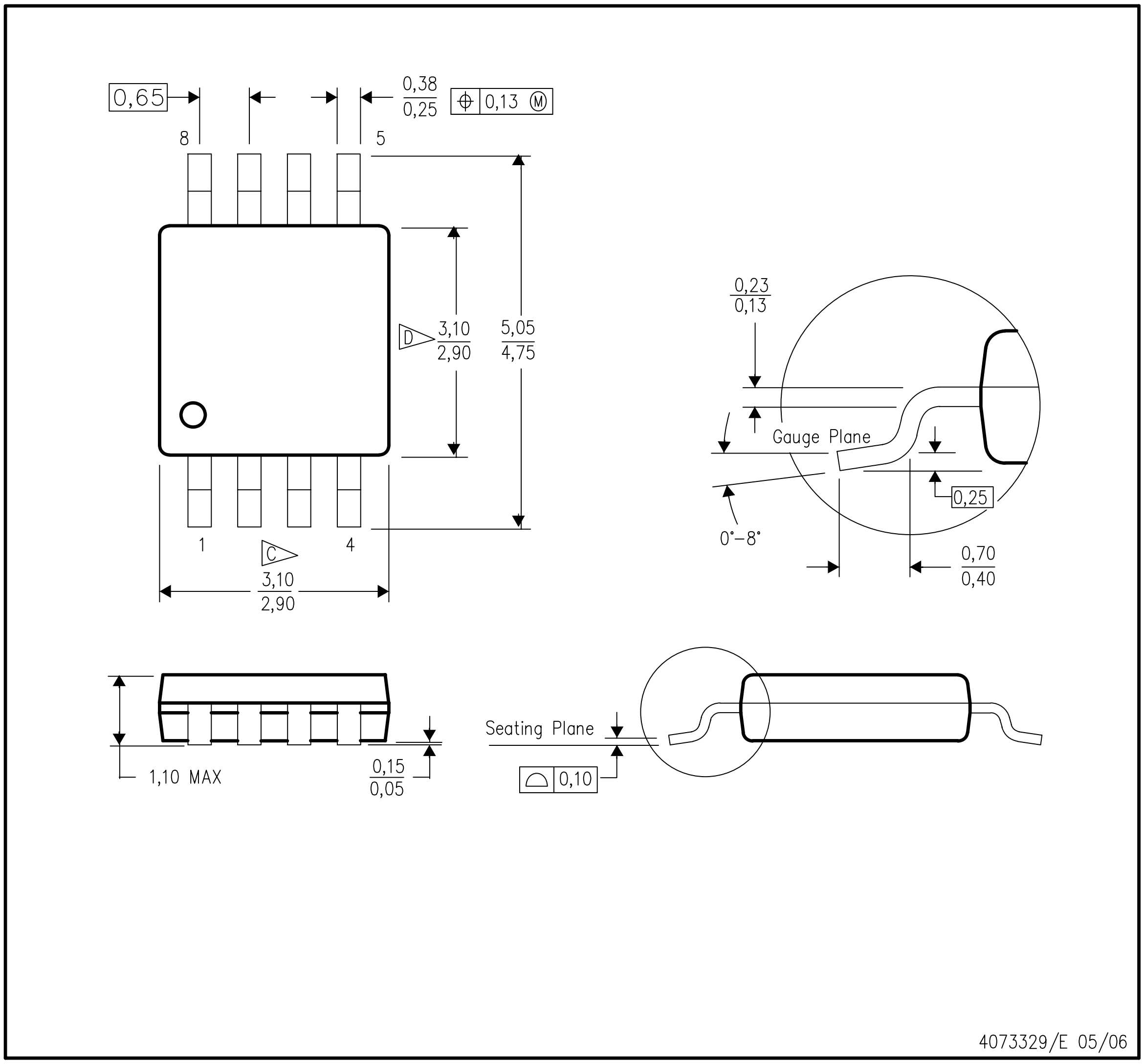
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

MECHANICAL DATA

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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Figure 24. DGK Package Drawing

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMAG5170A1EDGKQ1	ACTIVE	VSSOP	DGK	8	80	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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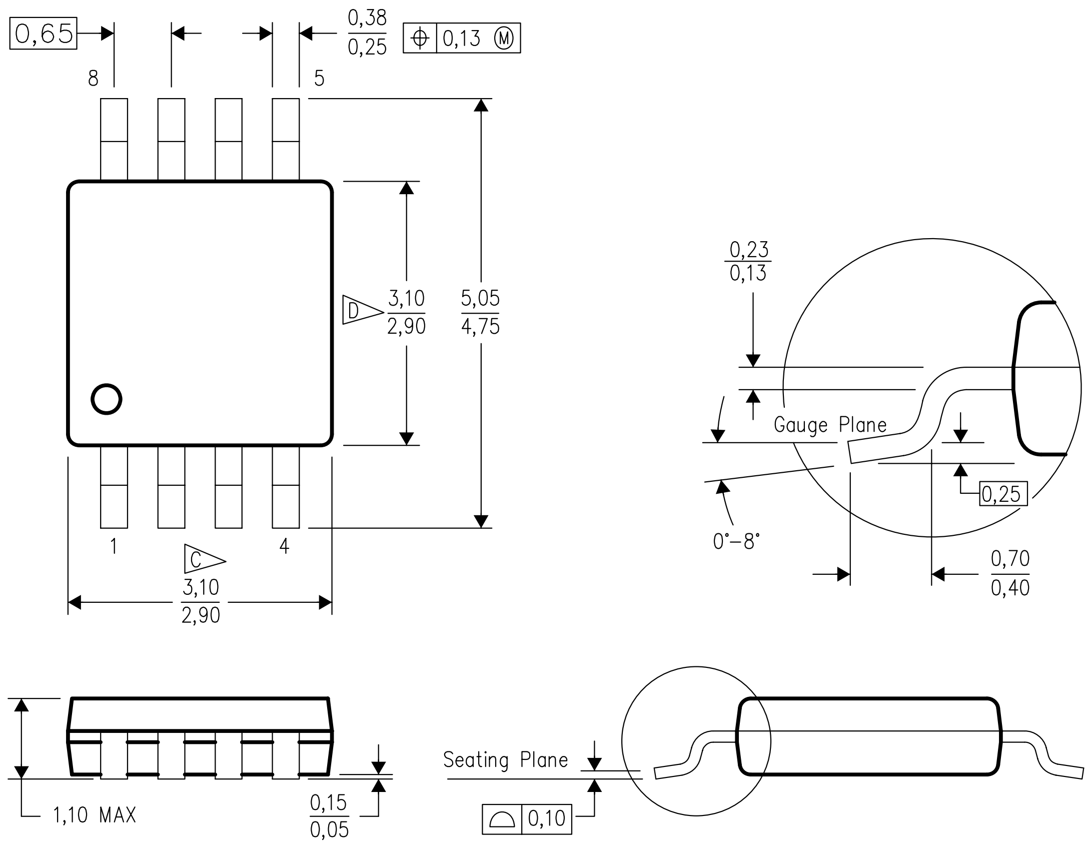
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES:
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- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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